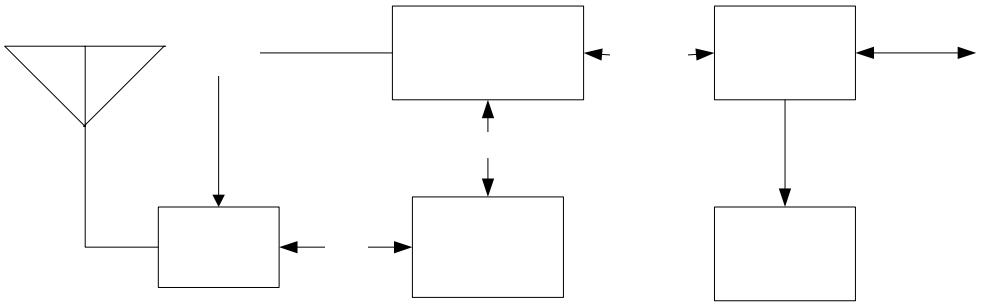
RF Remote Transmitter Block Diagram and Operational Description 06/05/18

Introduction

This document describes the operation of the major blocks within the RF Remote Transmitter. The following diagram shows the major blocks (one for each major IC) for the RF Remote Transmitter.

RF Remote Transmitter Block Diagram



Operation

The RF Remote Transmitter consists of two circuit boards, one being the RF board and the other being the Remote Radio Interface. The RF board consists of the Transceiver, Message Protocol, Bit Protocol, and Power regulation blocks. The RF Board is used in the RF Remote Transmitter in a transmit only mode and is used in the terminal device in a receive only mode.

RS422 Interface

The RF Remote Transmitter interfaces to the RF Base Station using CAT-5 cable. The CAT-5 cable carries RS-422 signals for data communications and 9VDC power. The 9VDC is regulated to produce 5VDC and 3VDC for the RF Remote Transmitter electronics.

Message Protocol Processor

High level messages are passed between the RF Base Station and the RF Remote Transmitter over the RS422 link and are encapsulated with a CRC. The following messages are sent over the link;

a) **Configure** – synchronize the RF Remote Transmitter with the RF Base Station and configure the transmitter with logical stream information.
b) **Open Stream** – Open a logical stream of bytes. There are 3 logical streams.
c) **Close Stream** – Close a logical stream of bytes.
d) **Get Stream** – Get bytes from one of the logical streams.
e) **Put Stream** – Put bytes to one of the logical streams
f) **Radio Info** – Get radio statistics on how many transmission errors there were and if any data is available on one of the logical streams.

The Message Protocol processor constantly sends the last logical stream messages over the radio link. The stream messages are sliced into 51 time slots which are transmitted on 51 different pseudo random frequencies. The Message Protocol processor sends frequency selection information to the Transceiver chip over an SPI like interface at the beginning of each time slot. The Message Protocol processor also sends asynchronous bytes of message data to the Bit Protocol processor. Byte data sent between the Message Protocol processor and the Bit Protocol Processor is encode in 8-10 format to ensure there is no large consecutive strings of one or zero bits.

When in receive mode the Message Protocol processor sits on one of the 51 pseudo random frequencies until a valid message is received. Once a valid message has been found, the receiver will continue to hop in sync with the transmitter.

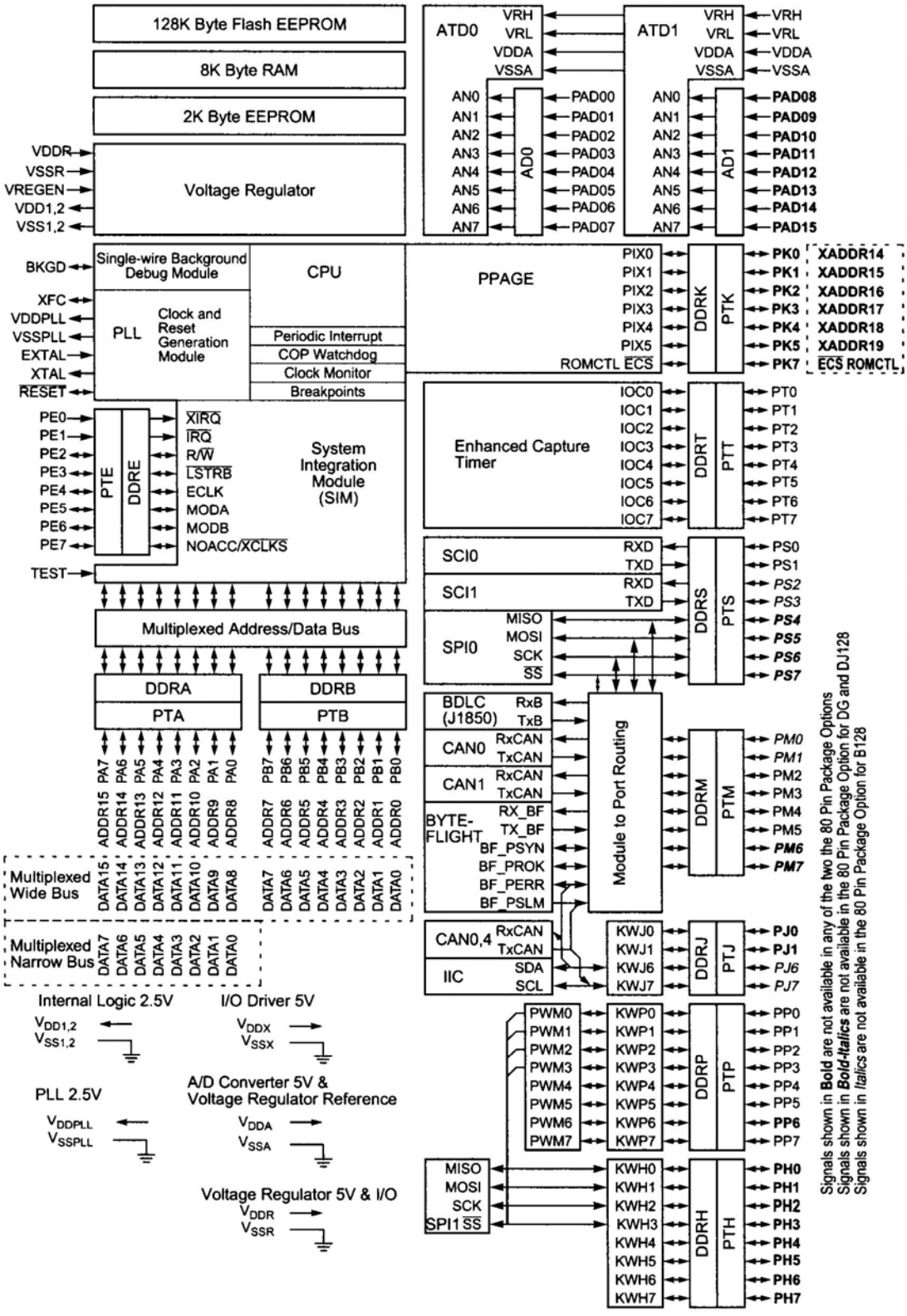
Bit Protocol Processor
The Bit Protocol processor is responsible for taking asynchronous data to/from the Message Protocol Processor and converting it to/from synchronous data which is sent to/from the Transceiver chip. The Bit Protocol processor is also responsible for adding and stripping sync bits to the stream messages sent. The Bit Protocol processor ensures that critical timing is adhered to on bits sent.

Transceiver Chip
The transceiver chip can operate in transmit or receive mode on a fixed narrow band frequency and these parameters are controlled using a SPI like interface. Data is transferred to the Transceiver chip at a rate of 10Kbps.

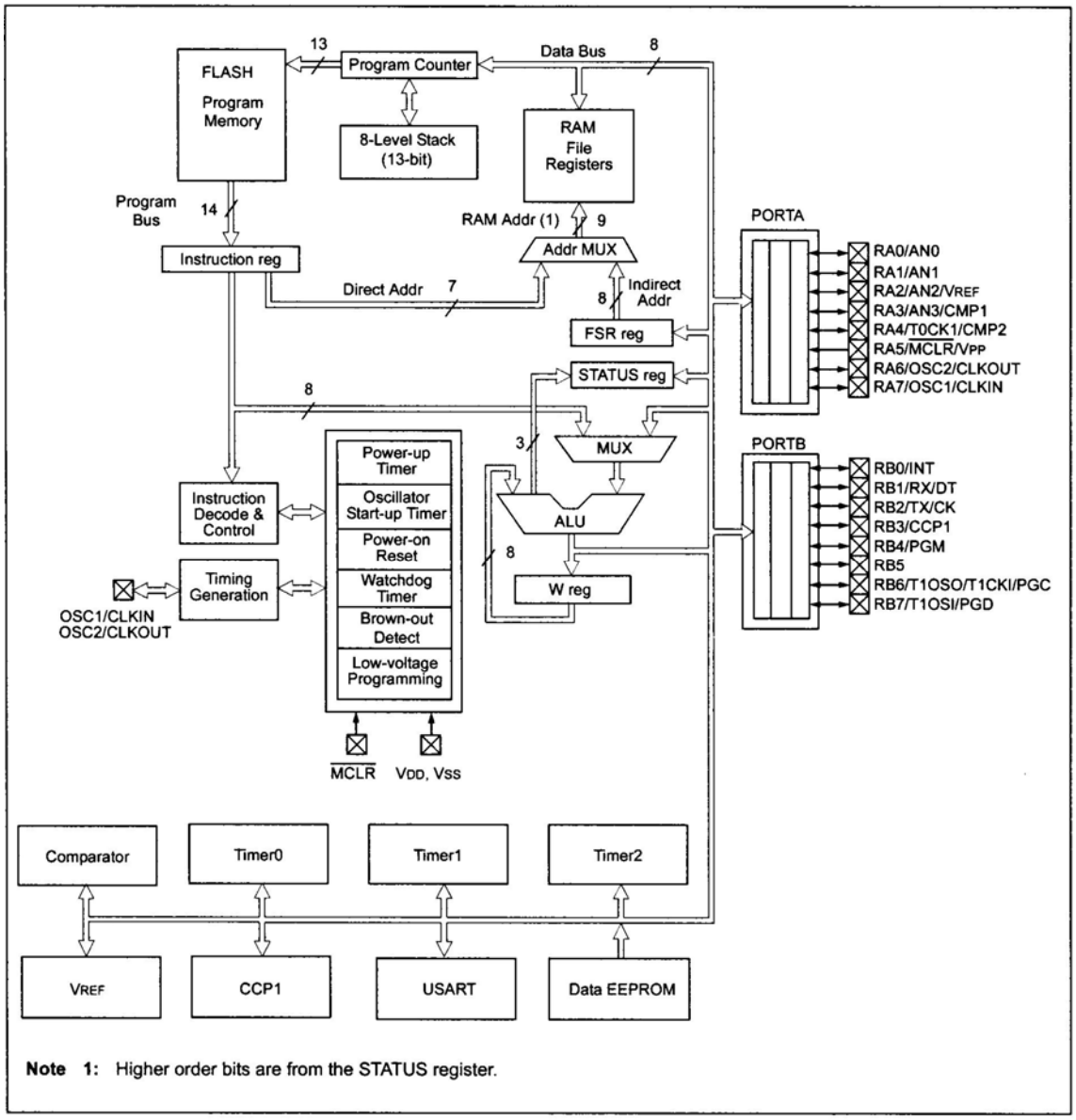
Subsystem Block Diagrams
The following are block diagrams of the three major ICs used in the RF Remote Transmitter.

MC9S12A128 Block Diagram

Figure 1-1 MC9S12DT128 Block Diagram

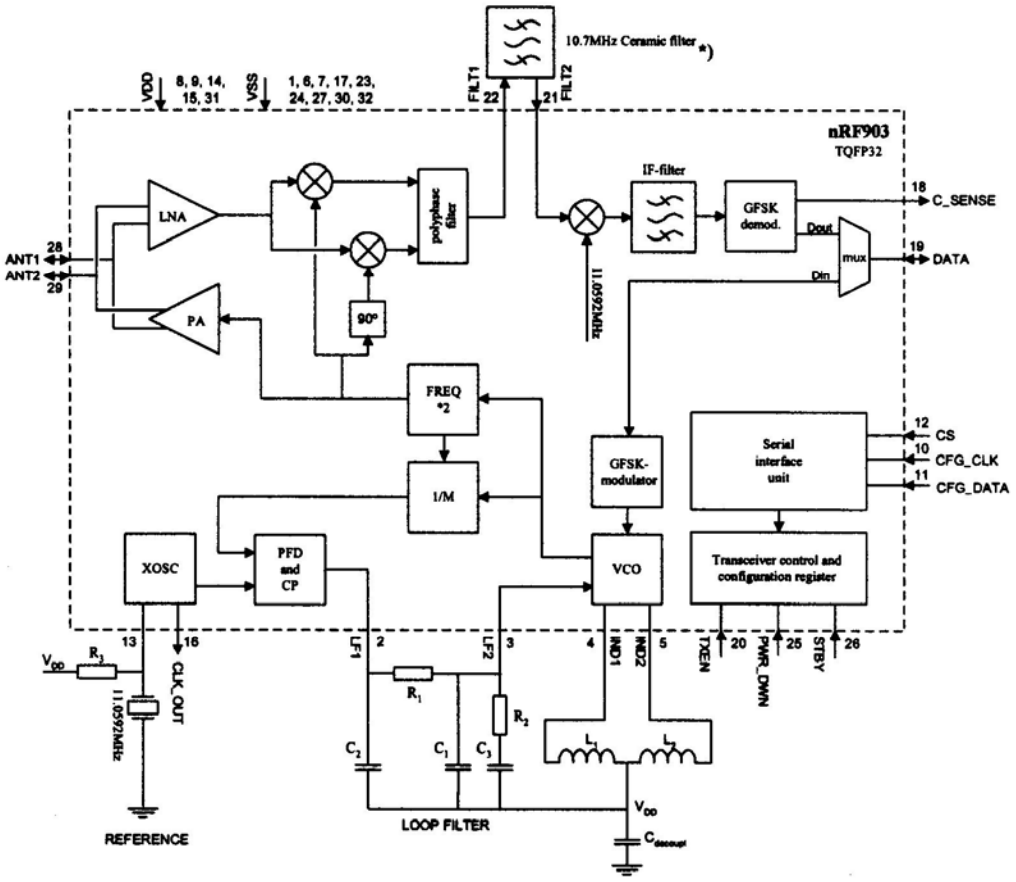


PIC16F62X Block Diagram



NRF903 Block Diagram

BLOCK DIAGRAM



*) The external filter may be replaced with a 10nF capacitor at the expense of receiver performance (see page 18)

Figure 1. nRF903 block diagram with external components.