MC1320x RF Daughter Card

User's Guide

1 Introduction

The MC1320x RF Daughter Card, 1320xRFD-A00, is used in conjunction with a microcontroller development board for RFIC evaluation, code development, and system evaluation. It interfaces directly to the M68EVB908GB60, RG60 and QG60 HCS08 family Microcontroller Development Board and the M5223 EVB Microcontroller Development Board, but it can be adapted to other boards that offer access to the MCU input/output ports.

The board is configured with all the off-chip circuitry required for functional performance of the MC1320x RF data modem except the MCU. The MCU interface required by the RFIC is pinned out at the edge of the card using standard header pins. The RF interface is accomplished through onboard antenna and can be modified for SMA connector interface. The SMA connectors can be connected to test equipment via coax cables for testing. Figure 1 Shows the RF Daughter Card. Figure 5 Shows the RF Daughter Card installed in a GB60 development board.

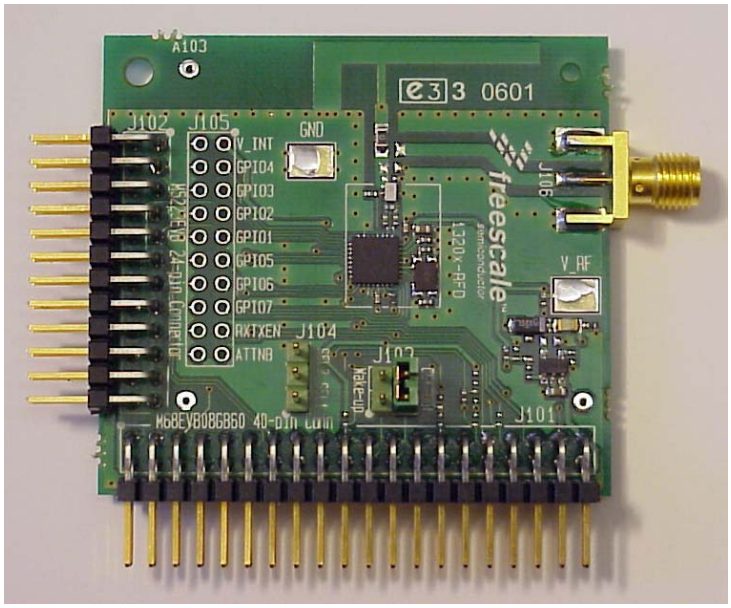

Figure 1. MC1320xRF Daughter Card.

2 Safety Information

Any modifications to this product may violate the rules of the Federal Communications Commission and make operation of the product unlawful.

47 C.F.R. Sec. 15.21

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

47 C.F.R. Sec.15.105(b)

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. The antenna(s) used for this equipment must be installed to provide a separation distance of at least 8 inches (20cm) from all persons.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

3 MCU Interface Basics

Refer to the data sheet, MC1320x, and reference manual, MC1320xRM, for interface details.

4 Board Details

Figure 2 shows the top side of the PCB and Figure 3 shows the bottom side. Figure 4 is the board schematic and Table 1 is the bill of materials.

Referring to Figure 2 and Figure 4, connector J101 is the main interface to the M68EVB908GB60 HCS08 family Microcontroller MCU board. The interface connections fall under three broad categories; Serial Peripheral Interface (SPI), control and power. See Figure 5 for mounting.

> **Note:** *MC1320x RFD J101 pin 1 need to be connected to M68EVB908GB60 GB_PORT pin 1.*

Referring to Figure 2 and Figure 4, connector J102 is the main interface to the M5223 EVB board. See Figure 6 for mounting.

> **Note:** *MC1320x RFD J102 pin 1 need to be connected to M5223 EVB MCU_PORT pin 1.*

> **Note:** *All pin references in the following chapters are for the M68EVB908GB60 HCS08 family Microcontroller MCU board. Pin references in brackets are for the M5223 EVB Microcontroller MCU board.*

4.1 SPI Connections

J101 pins 35 through 38 (J102 pin 17, 19, 21 and 23) provide the four wire SPI interface, MOSI, SPICLK, CE, and MISO. The MC1320x always functions as a slave device. SPI operation is described in detail in the MC1320x data sheet and reference manual.

> **Note:** *CE on the J102 pin 23 and 24 are wired to a header J104. This controls the functionality of CE. When the pins 2 and 3 of J104 are shunted, CE is wired to J102 pin 24 (PTE2/CE-AN7). When Pins 1 and 2 of J104 are shorted, the CE is wired to J102 pin 23 (PTE2/CE-QSPI_CS0).*

4.2 Control Connections

J101 Pin 19 (J102 pin 2) is the IRQ line from MC1320x. Connection to the MCU will depend on how the MCU services interrupts. RXTXEN, J101 Pin 31 (J102 Pin 20), allows the MCU to initiate transceiver functions. The ATTN line, J101 Pin 34 (J102 Pin 15), allows the MCU to wake up the MC1320x from Doze or Hibernate low power modes. RXTXEN and ATTN are also available at header J105 for manual control. J101 Pin 24 provides the MC1320x CLKO to the MCU when a jumper is installed at J103. J101 Pin 32 (J102 Pin13) interfaces with the MCU to provide a Reset to the MC1320x. J101 pins 5 and 22 can provide a wake up function to the MCU when a shunt is installed at J103. J101 pin 13 and 14 (J102 pins 9 and 11) provide access to MC1320x GPIO1 and GPIO2 ports.

4.3 Power Connections

J101 pin 39(J102 pin 1) provides the supply voltage to the RF Daughter Card. Voltage on this line should never exceed 16.0 V and the nominal supply should not exceed 16.0 V. J101 pin 40 (J102 pin 3) is ground. Please note that MCU connection signals are dependant of the on-board voltage regulator. If R105, D101 and C101 is mounted, while R115 is removed, the J101 pin 39 also provides the interface supply voltage and never must exceed 3.6 V. Nominal supply should not exceed 3.4 V.

4.4 Non-MCU connections

Header J105 provides connections to a number of MC1320x contacts for non MCU interface. As mentioned, RXTXEN and ATTN lines are available for external control via switches or other hardware. The MC1320x GPIO is available for interface to external hardware.

4.5 Software configuration

Referring to Figure 4, there is a table legend in schematic recommending jumper settings for Wake, Clk. Out and Chip Enable setup.

Note: *The Wake and Clk. Out is for the GB60 board interface only, and the Chip Enable is for the M5223 EVB interface only.*

For software development we recommend to get newest available SW development tools and user guides at the following web pages:

For Zigbee related SW. www.freescale.com/zigbee

For Microcontroller SW. See your Development kit or www.codewarrior.com

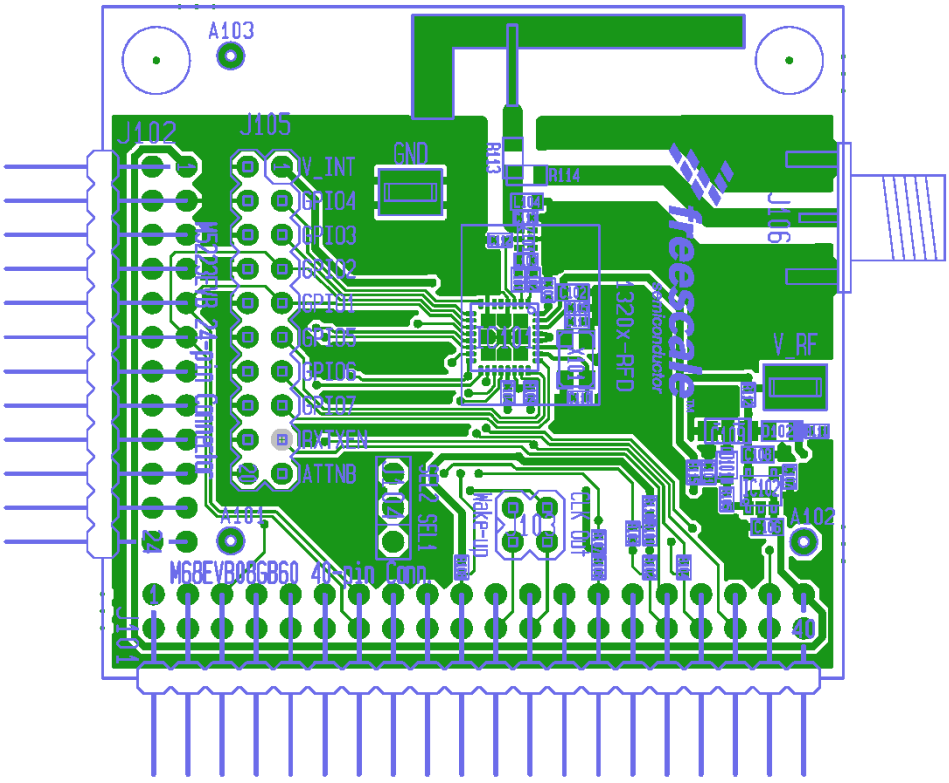

Figure 2. Daughter Board Layout Top layer with comp placement.

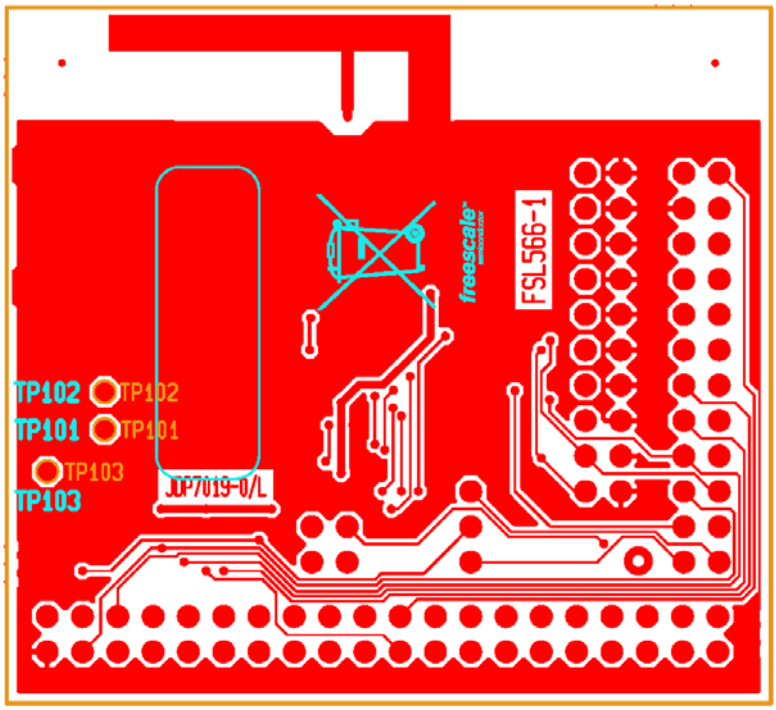

Figure 3. Daughter Board Layout. Bottom layer.

Qty	Unit	Value	Rating	Tolerance	Manufacturer	Manufacturer's Part Number	Part Reference
3	pcs	100nF	6.3V	10% X5R	Murata	GRP155R60J104KA01E	C103, C104, C105
2	pcs	1µF	6.3V	10% X5R	Murata	GRM188R60J105KA01D	C102, C106
1	pcs	3.3µF	10V	20%	Vishay Sprague	293D335X0010A2T	C109
2	pcs	6.8pF	50V	±0.25pF NP0/C0G	Murata	GRM1555C1H6R8DZ01J	C110, C111
1	pcs	10pF	50V	5% NP0/C0G	Murata	GRM1555C1H100JZ01D	C112
1	pcs	Green_LED			Citizen	CL-170G-CD-T	D102
1	pcs	MC13202			Freescale Semiconductor	MC13202	IC101
1	pcs	LP2981IM5-3.3			National	LP2981IM5-3.3	IC102
1	pcs	2*20p Pin Header - Right Angle			Molex	10-89-4402	J101
1	pcs	2*12p Pin Header - Right Angle			Molex	10-89-4242	J102
1	pcs	2*2p Pin Header			AMP	0-826632-2	J103
1	pcs	jumper_1x3			AMP	826629-3	J104
1	pcs	SMA_edge_Receptacle_Female			Johnson	142-0701-831	J106
2	pcs	ProbeLoop			Toby Electronics	TP-107-02-5-T	J107, J108
2	pcs	1.2nH		±0.3nH	Murata	LQG15HN1N2S00	L101, L102
1	pcs	3.9nH		±0.3nH	TOKO	LL1005-FH3N9S	L103
3	pcs	0R	62.5mW/50V	5%	Phycomp	2322 705 91001	R103, R112, R115
1	pcs	470K	62.5mW/50V	1%	ROHM	MCR01MZSF4703	R109
1	pcs	220R	62.5mW/25V	5%	YAGEO	RC0402JRE07220RL	R111
1	pcs	0R	125mW/150V	5%	YAGEO	RC0805JR-07	R113
1	pcs	16.000MHz	20ppm	20ppm	KDS	ZD00882	X101
1	pcs	LDB212G4005C-001			Murata	LDB212G4005C-001	Z101

Table 1. Bill of Materials

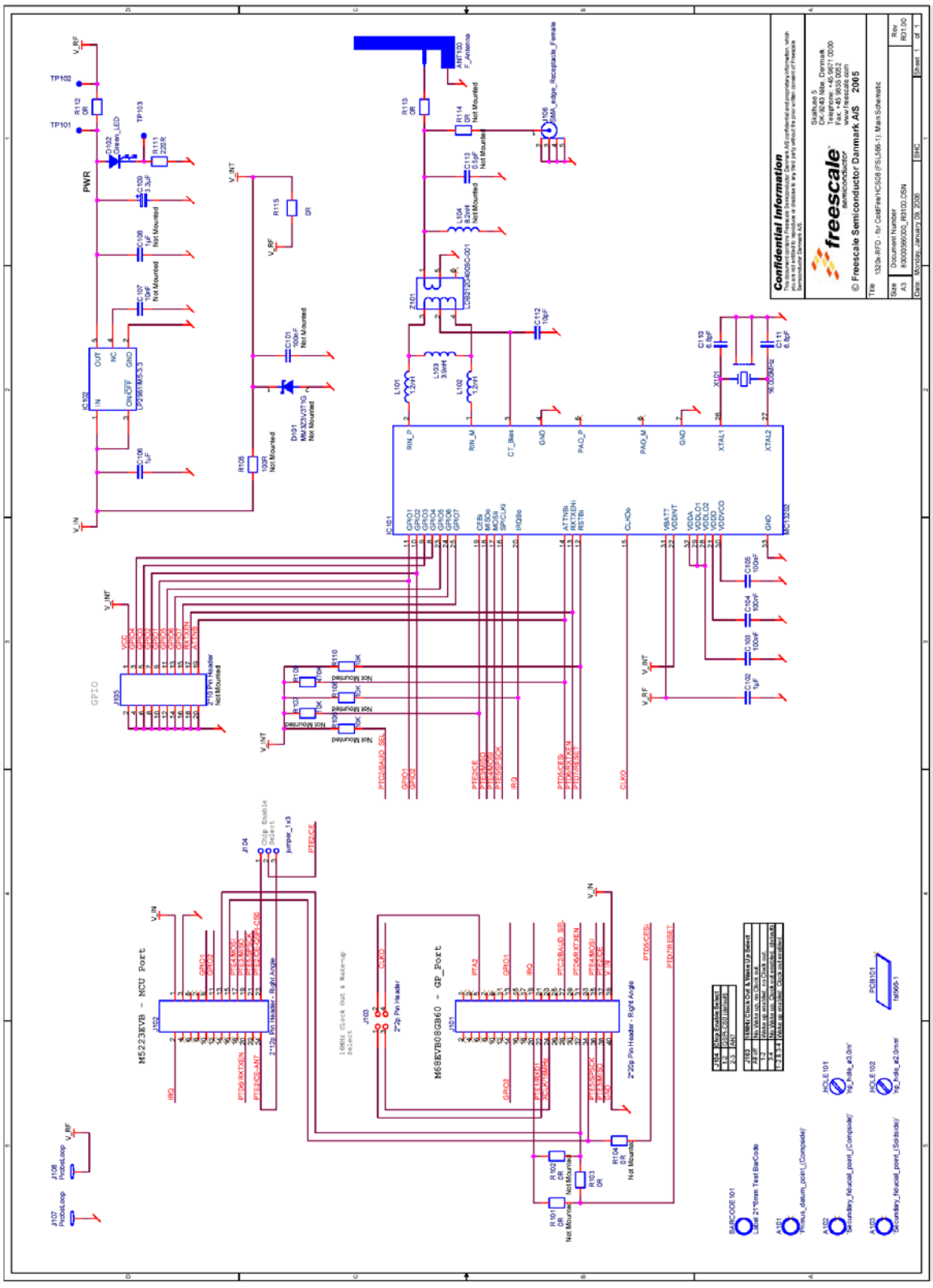

Figure 4. RF Daughter Card Schematic

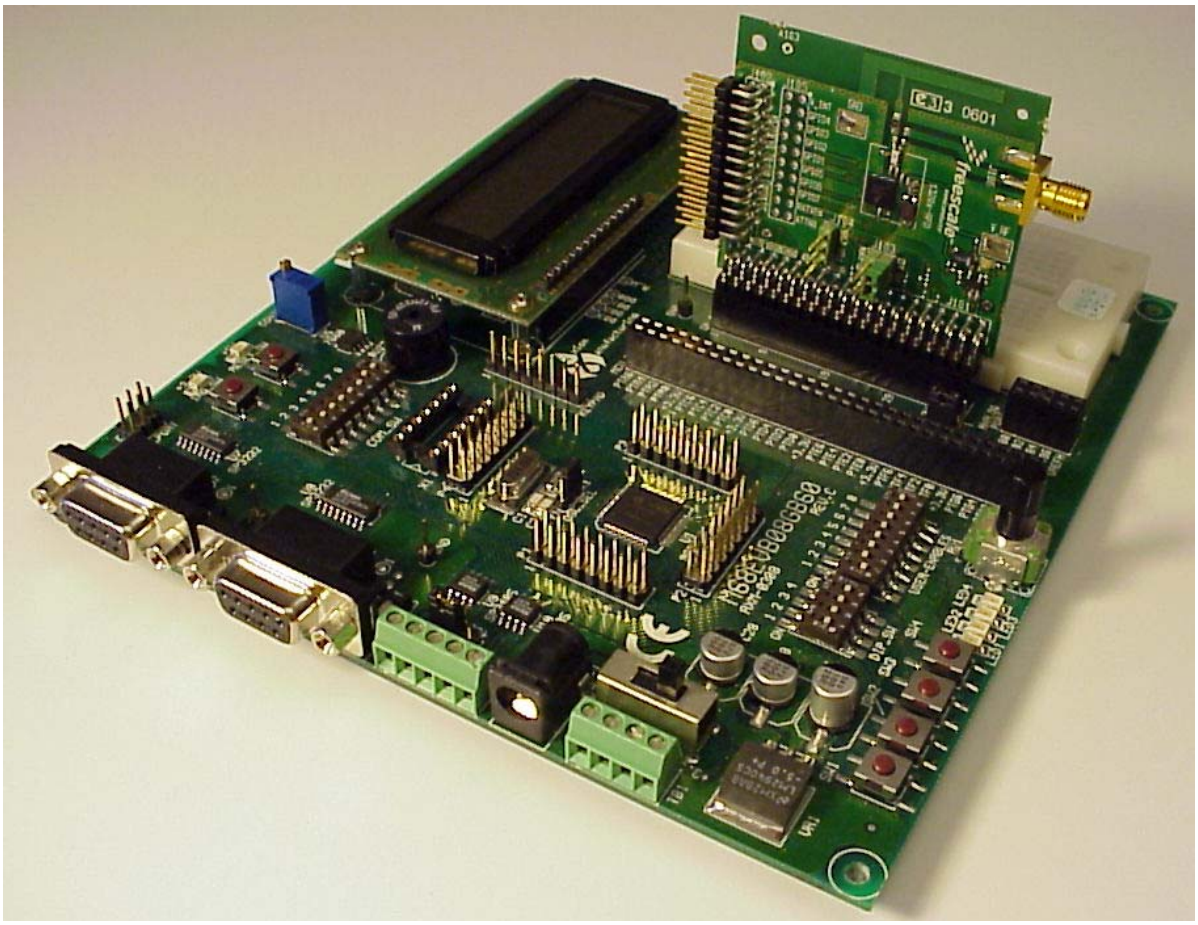

Figure 5. RF Daughter Card Installed in the GB60 Development Board