ETERNA2 Operational Description

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1 Operational Description

ETERNA2 provides a IEEE 802.15.4 compliant radios that modulate a DSSS OQPSK set of symbols at a chip rate of 2 Mcps. Dust radios operate on a TDMA time schedule that uses either 7.25 or 10 ms timeslots. A transmit timeslot consists of 5 stages:

1. Initialization: radio is prepared for transmit (transmitter is off)
2. Ramp: transmitter is ramped to peak power
3. Transmit: 128 bytes of data maximum + 5 bytes preamble/SFD
4. Turnaround: radio is set to receive
5. Receive: radio waits in receive for ACK, then turns off

Total transmit time for a 128 byte packet plus all overhead (SFD / Preamble / Ramp) is 4.33ms.

A receive timeslot consists of 5 stages:

1. Initialization: radio is prepared for receive
2. Check for start of packet – if no packet is received within a guard time the radio is disabled and no further action is taken
3. Receive the packet: up to 128 bytes of data maximum + 5 bytes preamble/SFD
4. Turnaround: radio waits 1 ms and then is set to transmit
5. Transmit: radio sends an ACK (21 bytes of data + 5 bytes preamble/SFD), then turns off

Total transmit time for an ACK is plus all overhead (SFD / Preamble / Ramp) is 1.101 ms.

Measured records and calculations of ETERNA2 radio transmit duty cycling are included in "ETERNA Duty cycle.pdf".

When the radio is not in operation, the CPU is occasionally (every few seconds for a few milliseconds) operating, monitoring temperature and voltage. The remainder of the time the ETERNA2 in a low power mode operating solely from a 32 kHz crystal source.