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1. INTRODUCTION

The purpose of this document is to describe the hardware architecture of the Mitsubishi Type VGM08. There are two versions of it, called M420i and M760. The two models share the same hardware. The M420i is a 'I-Mode' product whereas the M760 is the 'MMS' version. Only 'M420i' will be used in the following chapters

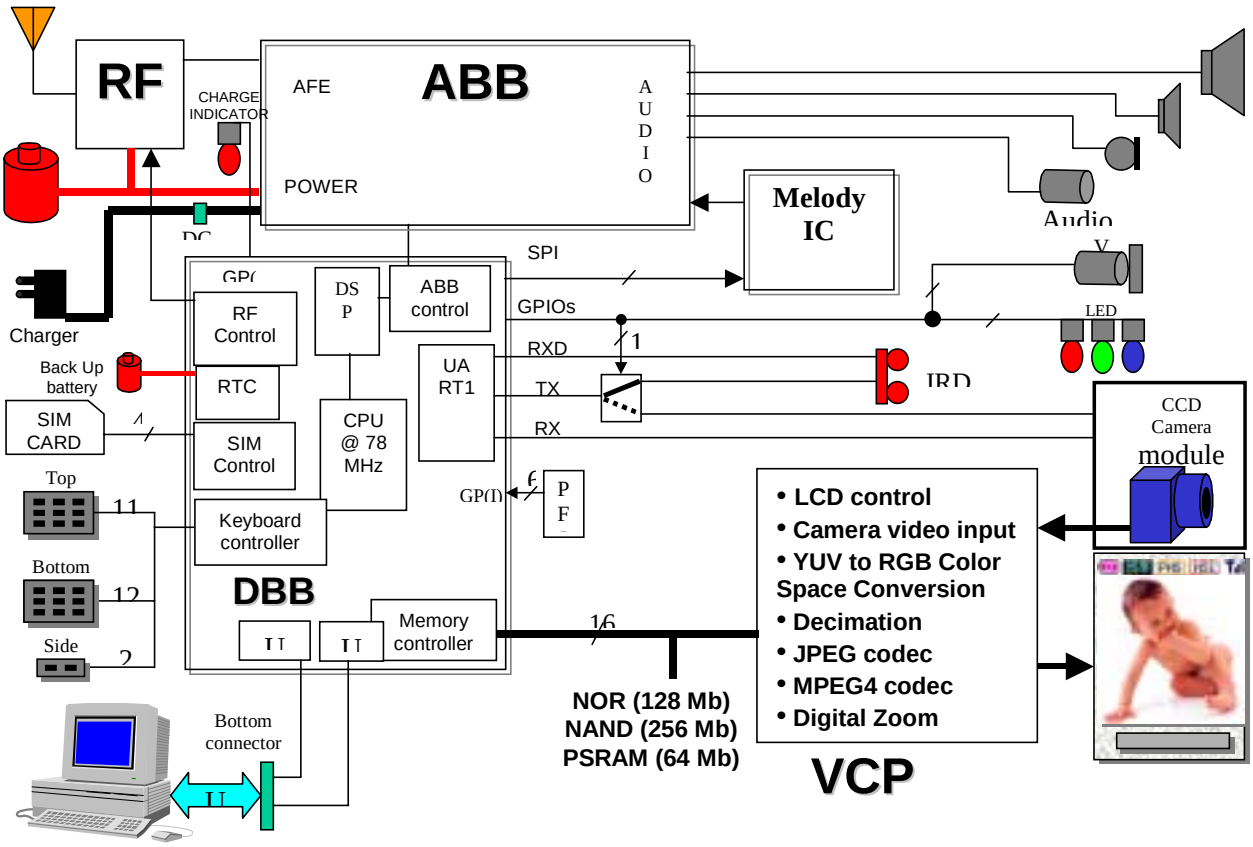

Figure 1 : Overall Diagram

The M420i is a tri-band GSM 2G multimedia mobile phone, including GPRS (Class 10) features.

Main feature

Length	98mm
Width	48mm
Thickness	23mm
Volume	< 100cc
Weight	< 115g including battery
Mini SD slot	No
SIM voltage	3V
Battery voltage	3,7 volt
Battery type	SGS Li-Ion
Battery capacity	830 mA/h
Main Screen	176x240 TFD 265K colors
Camera	CCD 960x1280 pixels
EGSM	Class 4 (2W)
DCS 1800	Class 1 (1W)
PCS 1900	Class 1 (1W)

Radio characteristics

	Frequency Bands	Arfcn	Frequencies (Mhz)
PGSM 900 TX	890-915 MHz	$1 \le n \le 124$	$F_{TX} = 890+0.2*n$
PGSM 900 RX	935-960 MHz	$1 \le n \le 124$	$F_{RX} = F_{TX} + 45$
EGSM 900 TX	880-915 MHz	$975 \le n \le 1023$ $0 \le n \le 124$	$F_{TX} = 890 + 0.2*(n-1024)$ $F_{TX} = 890 + 0.2*n$
EGSM 900 RX	925-960 MHz	$975 \le n \le 1023$ $0 \le n \le 124$	$F_{RX} = F_{TX} + 45$
DCS 1800 TX	1710-1785 MHz	$512 \le n \le 885$	$F_{TX} = 1710.2 + 0.2*(n-512)$
DCS 1800 RX	1805-1880 MHz	$512 \le n \le 885$	$F_{RX} = F_{TX} + 95$
PCS 1900 TX	1850-1910 MHz	$512 \le n \le 810$	$F_{TX} = 1850.2 + 0.2*(n-512)$
PCS 1900 RX	1930-1990 MHz	$512 \le n \le 810$	$F_{RX} = F_{TX} + 80$

2. TRANSCEIVER ARCHITECTURE

The M420i uses an integrated transceiver for multi-band GSM/GPRS. This highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules.
The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity. The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (PLL) with a fully integrated transmit VCO. The frequency synthesizer uses proven technology that includes integrated RF and IF VCOs, varactors, and loop filters.
The unique integer-N PLL architecture produces a transient response superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the transceiver well suited to GPRS multi-slot applications where channel switching and settling times are critical.

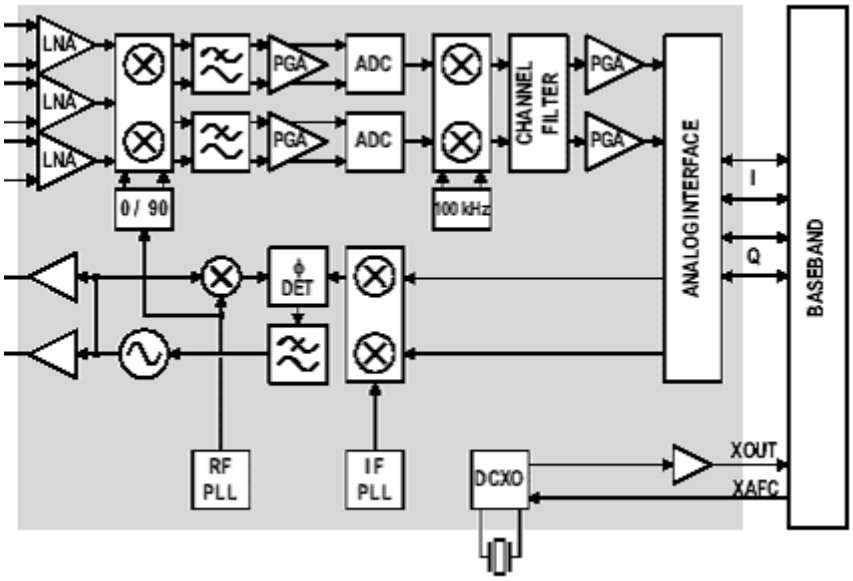

Figure 2 : Transceiver Block Diagram

2.1 TRANSMIT BLOCK

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two 50 Ω output buffers that can drive external power amplifiers (PA), one for the E-GSM 900 (880–915 MHz) band and one for the DCS 1800 (1710–1785 MHz) and PCS 1900 (1850–1910 MHz) bands. The OPLL requires no external duplexer to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power.

Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA. A quadrature mixer upconverts the differential in-phase (IP, IN) and quadrature (QP, QN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL. The IFLO frequency is generated between 766 and 896 MHz.

IFLO = 798 MHz for TX EGSM [880-895] and [900-915]
IFLO = 790 M for TX EGSM [895-900]
IFLO = 766 MHz for TX DCS
IFLO = 854 MHZ for TX PCS

The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz. For the E-GSM 900 band, two different IFLO frequencies are required for spur management. Therefore, the IF PLL must be programmed per channel in the E-GSM 900 band. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by two for E-GSM 900 band. The synthesizer generates the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the E-GSM 900 band, and low-side injection is used for the DCS 1800 and PCS 1900 bands. Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable.

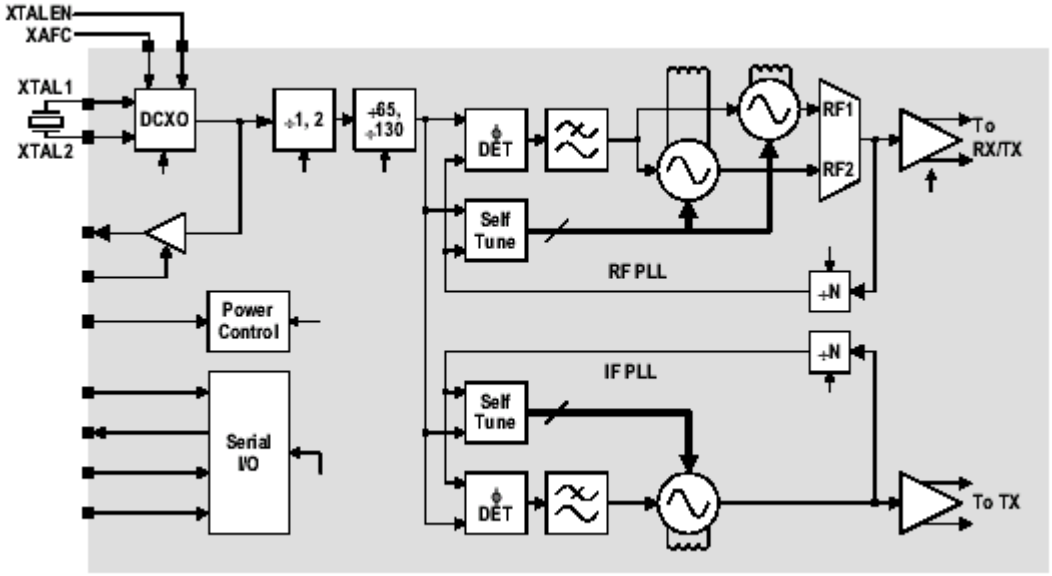

Figure 3 : Synthesizer Block Diagram

2.2 SYNTHESIZER BLOCK

The transceiver integrates two complete PLLs including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode. All VCO tuning inductors are also integrated. The IF and RF output frequencies are set by programming the N-Divider registers, NRF1, NRF2, and NIF. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$FOUT = Nxf_0$$

A programmable divider in the input stage allows either a 13 or 26 MHz reference frequency depending on the choice of crystal. A 26 MHz reference clock is used on our product. The RF PLL phase detector update rate (f_0), can be programmed to either f_0= 100 kHz or f_0 = 200 kHz. The IF PLL always uses f_0 = 200 kHz. Receive mode should use f_0 = 100 kHz in DCS 1800 and PCS 1900 bands, and f_0 = 200 kHz in the E-GSM 900 band. Transmit modes should always use f_0 = 200 kHz.

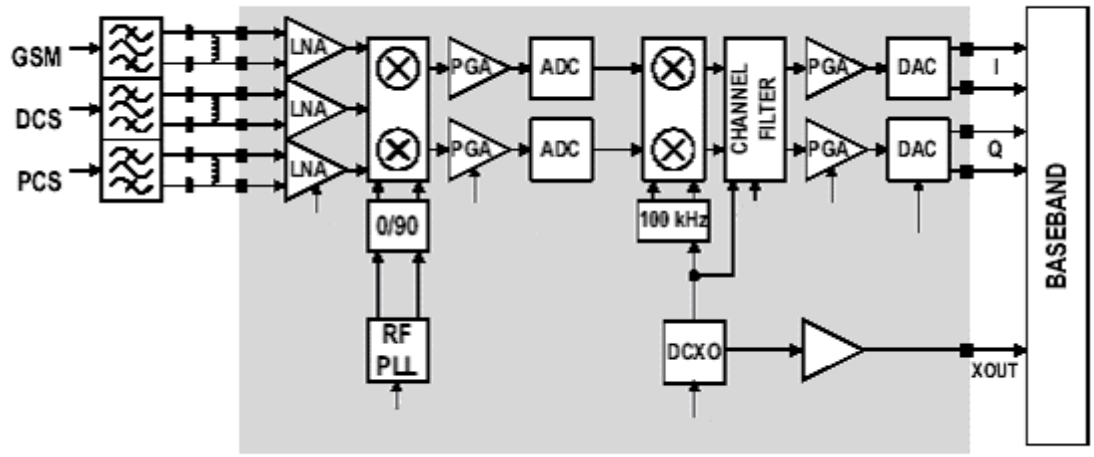

Figure 4 : Receiver Block Diagram

2.3 RECEIVER BLOCK

The transceiver uses a low-IF receiver architecture that allows for on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional super heterodyne architectures. Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, 2nd-order distortion of blockers, and device 1/f noise. This relaxes the common mode balance requirements on the input SAW filters and simplifies PC board design and manufacturing.
Three differential-input LNAs are integrated. The GSM input supports the EGSM 900 (925–960 MHz) band. The DCS input supports the DCS 1800 (1805–1880 MHz) band. The PCS input supports the PCS 1900 (1930–1990 MHz) band.
The LNA inputs are matched to the 200 Ω balanced output SAW filters through external LC matching networks.
A quadrature image-reject mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the frequency synthesizer. The RFLO frequency is between 1737.8 and 1989.9 MHz, and is divided by two for E-GSM 900 mode.
The mixer output is amplified with an analog programmable gain amplifier (PGA), which is controlled converters (ADCs).

The ADC output is downconverted to base band with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. The response of the IIR filter is programmable to a high selectivity setting or a low selectivity setting. The low selectivity filter has a flatter group delay response that may be desirable where the final channelization filter is in the base band chip. This is our implementation on M420i because we have a FIR in the baseband block. After channel selection, the digital output is scaled with a digital PGA.

2.4 HPA BLOCK

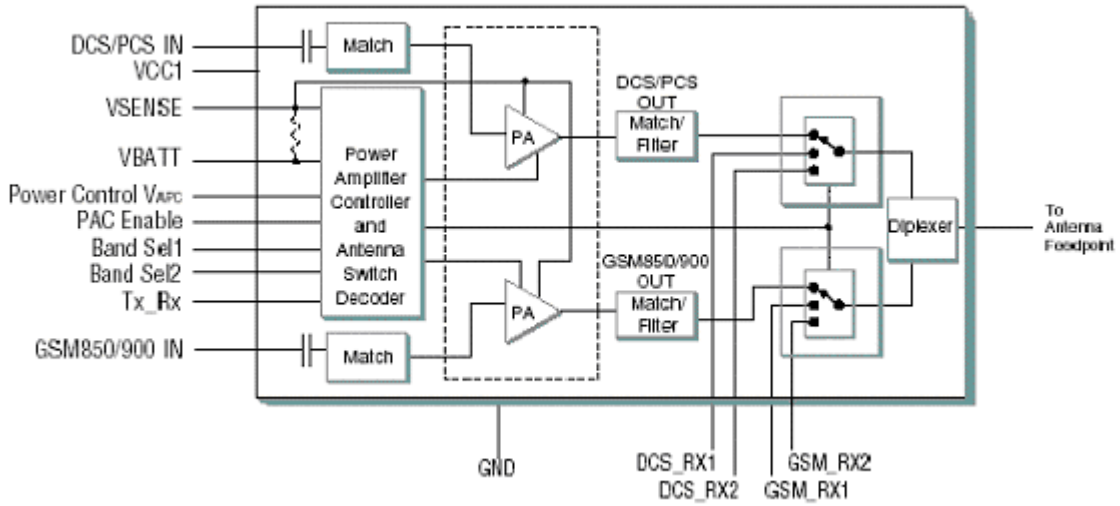

Figure 5 : Functional Block Diagram of the PA

The transmitter module is a tri-band Power Amplifier device with integrated power amplifiers (two lines), the antenna switch, and a power amplifier control (iPAC). The iPAC approach is based on current sense architecture that incorporates a DC feedback loop around the Power Amplifier to maintain a temperature, supply, and input power invariant collector current in the amplifier final stage. An error amplifier reads the voltage drop across an internal current sense resistor placed in series with the battery and the GaAs PA die. The output of the error amplifier adjusts the PA gain according to the set of DAC ramps determined during the handset calibration. The current is regulated at all times, so this architecture provides overload protection for the transmitter under adverse load conditions.

2.5 POWER RAMP UP AND RAMP DOWN

The rising and falling edge ramp profiles are critical in minimizing the ORFS. The waveform used for the burst edges is based on raised cosine shape. This waveform can be expressed as:
$y(t) = 0.5 * (1 + \cos[\pi t/\tau + \pi])$
where τ is the desired ramp duration and t is the discrete time point along the ramp.

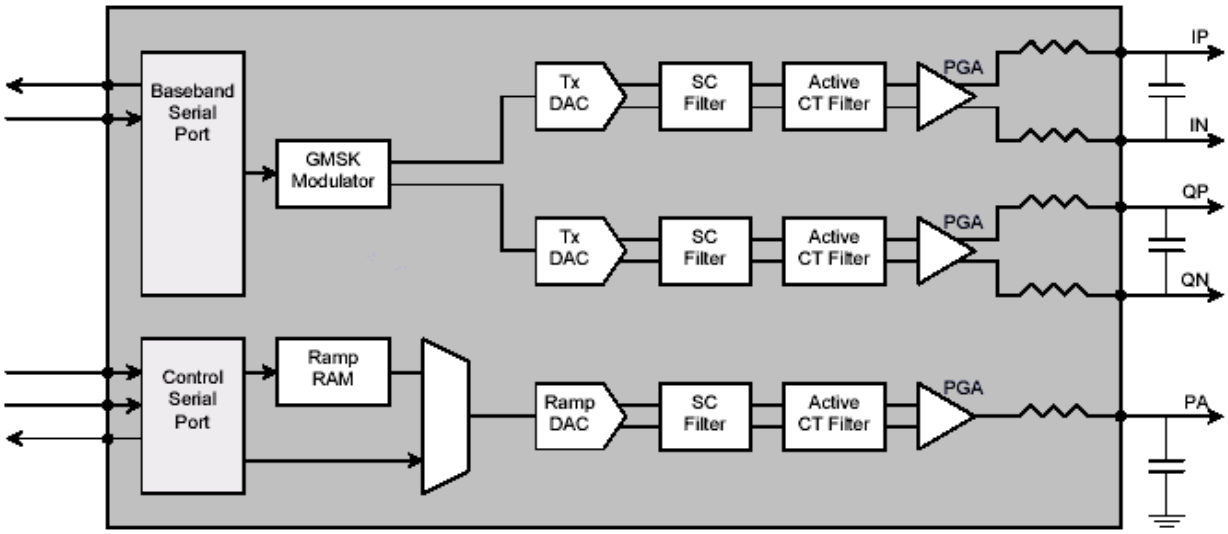

Figure 6 : Baseband transmit section

3. BASEBAND

3.1 BASEBAND TRANSMIT SECTION

The Baseband Transmit Section is designed to support GMSK for both single-slot and multislot applications. The complete transmit path is shown in Figure 6.

The transmit DACs convert the input digital data to charge packets. The Switched-Capacitor Filters are 2nd order filters that convert the charge packets to voltages. The Active-RC Filters are 1st order filters. A combination of integrated resistors and an off chip capacitor creates a final continuous time filter with a corner frequency around 816 kHz.
The Power Ramping DAC converts the input digital data to charge packets. The input digital data is provided by a 32x10-bit Ramp RAM that stores the power ramping coefficients for the next two power ramp events. The Switched-Capacitor Filter is a 2nd order filter that converts the charge packets to voltages. The Active-RC Filter is a 1st order filter with an input PGA that can amplify the signal by either 0 dB or 6 dB. The Active-RC Filter performs a differential to single ended conversion on the Switched-Capacitor Filter output. A combination of an integrated resistor and an off chip capacitor creates a final continuous time filter with a corner frequency around 452 kHz. The Ramp DAC output may be held low when the Ramp DAC is not active.

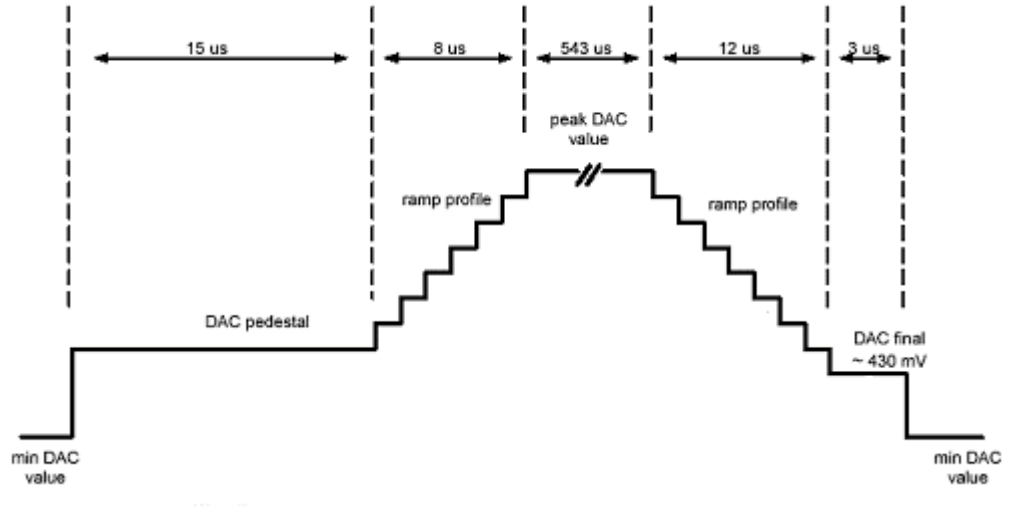

Figure 7 : DAC Ramp

Tableau 1 : GMSK Modulator Characteristics

Specification	Value	Units
Input Data Rate	13000/48	Kbits/s
Output Data Rate	6.5	MSamples/s
Gaussian Impulse response	3	Symbol/periods
GMSK Modulation Delay	11.5	µs

3.2 BASEBAND RECEIVE SECTION

The Baseband Receive Section is designed to support GMSK applications.

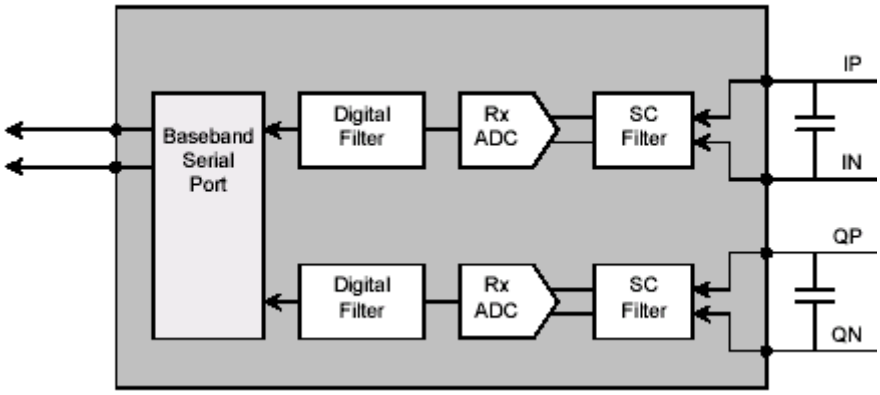

Figure 8 : Baseband receive section

The differential inputs to the Receive ADCs are filtered by the Switched-Capacitor Anti-Alias Filters. The SC Filters relax attenuation requirements for external anti-alias filters.
The Digital Filter attenuates adjacent channel interference and removes quantization noise produced by the Receive ADCs. The Digital Filter is a 576-tap FIR filter with linear phase. The Digital Filter produces one output sample per symbol.

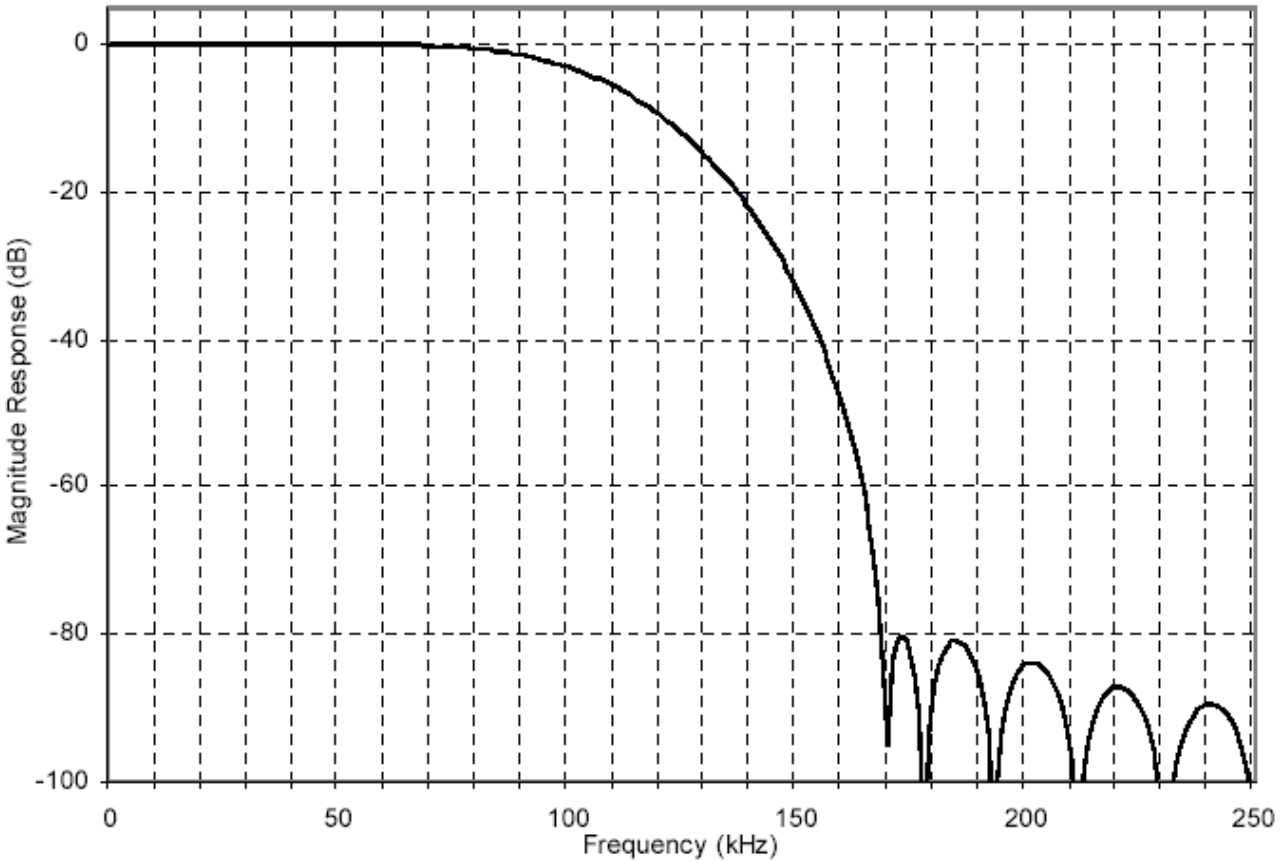

Figure 9 : Digital filter response

3.3 AUTOMATIC FREQUENCY CONTROL (AFC) DAC

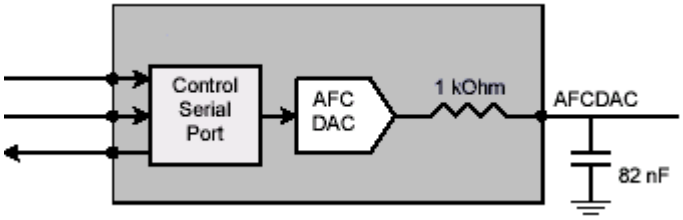

Figure 10 : AFC DAC

Tableau 2 : AFC DAC Specification

Specification	Value	Units
Resolution	13	bits
Input Data Rate	Fclk/48	kHz
Passive RC filter Corner	2	KHz

The AFC DAC is a 13-bit Sigma-Delta DAC that intrinsically does not exhibit differential nonlinearity. A 1st order lowpass filter is necessary to meet the AFC DAC performance specifications and to stabilize the AFC loop. The lowpass filter is formed using an integrated 1 kohm resistor and an external capacitor (82 nF) connected to the system reference clock inside the transceiver using an external crystal oscillator (26 MHz). The baseband determines the appropriate frequency adjustment based on the receipt of the FCCH burst and then adjusts the XAFC voltage using the baseband AFC DAC (13-bit).

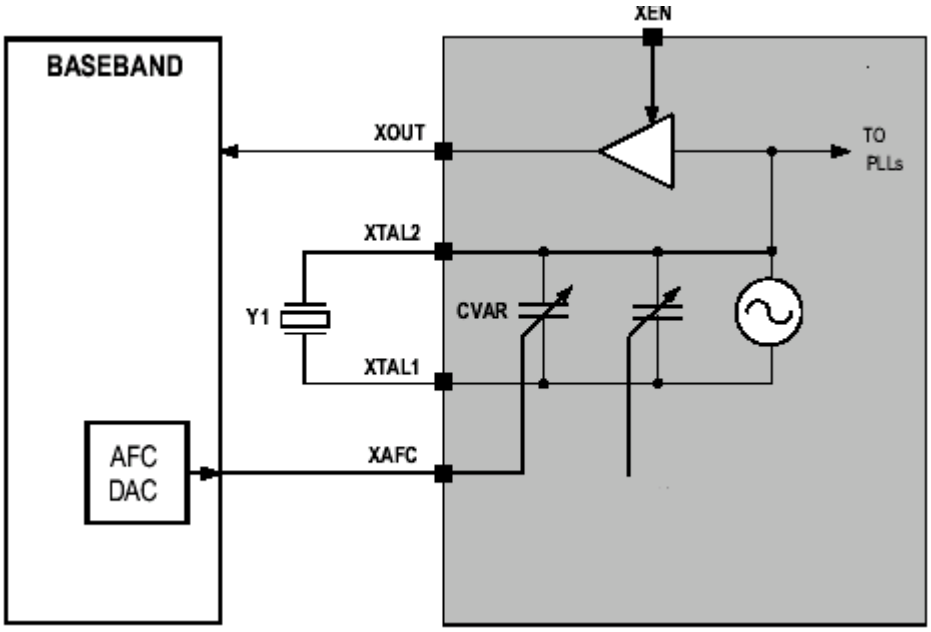

Figure 11 : Frequency Control