FCC Part 15.247 Certification
Test Report

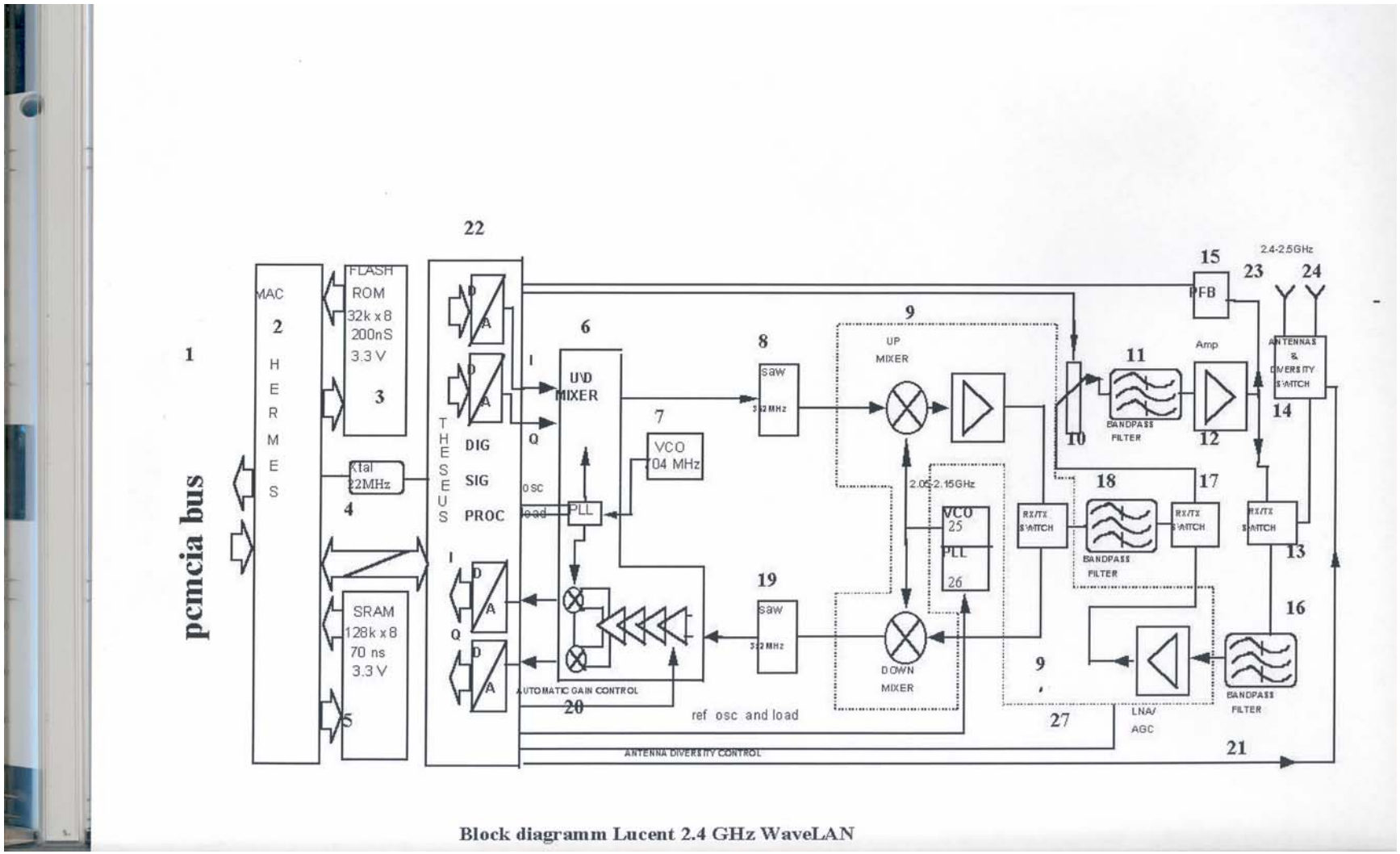
FCC ID: SH5-WASP

FCC Rule Part: 15.247

ACS Report Number: 04-0219-15C

Manufacturer: Miltope Corporation
Equipment Type: Wireless LAN System
Model: WASP

System Block Diagram



Block diagramm Lucent 2.4 GHz WaveLAN

DESCRIPTION OF THE BLOCK DIAGRAM

The various parts of the Block diagram are numbered and an explanation is given of these blocks.

First the transmitter will be described:

A) Digital Signal Processor. (22)

Function : Generate spreaded signal with an Barker sequence of 11, the original raw data rate of 1, 2, 5.5 or 11 Megabits is transformed to a symbol rate of one MegaBaud and multiplied with eleven and modulated with a DQPSK (Differential Quadrature Phase Shift Keying) Modulation for 1 and 2 Mbps or DQPSKCCK (CCK = Complementary Code Keying) for 5.5 and 11 Mbps. The unfiltered data comes out of I and Q and goes to the up/down mixer (6)

B) The above signals are mixed in (6) in a so called quadrature modulator with the Intermediate Frequency (IF) of 352 MHz.

C) The upmixer is fed by the VCO of 704 MHz, which is divided by 2 to 352 MHz.
D) The SAW (8) filters all unwanted mixing products, such that only the 352 MHz band remains.
E) This signal goes into the RF upmixer (9) SA2420 were it is mixed with the RF VCO with a range of 2050 to 2150 MHz.
F) The Rx/Tx switch (17) brings the signal to the variable attenuator (10), where the output level is controlled.
G) The signal is fed through a 2.4- 2.5 GHz bandpass filter (11) to remove all unwanted mixer products, and thus to get a clean signal for further processing.
H) The signal is amplified in (12), with approx 23 dB to an output level of approx. 15 dBm
I) This signal goes to the RX/TX antenna (23/24) via the special connector with a switch inside to disable the antenna.
J) The output power is controlled with a so called power feed back loop (15) in which the output power is compared with a DAC value from (10)

Receiver functions.

K) The receive signal enters the antenna passes the RX/TX switch (14) and (13) this is set to RX mode.
L) The signal goes through the 2.4 GHz filter (16) to remove all unwanted spectral components in order to deliver a clean signal for the receiver.
M) A Low Noise Amplifiers (LNA) (in 9) is used to amplify the weak signal to a level fitted for down mixing.
N) The AGC (27) can amplify or attenuate the signal according to the Digital signal processor required input with a step size of 26 dB.
O) Again the Rx/Tx switch in the Rx mode is passed and also the same filter as in transmit mode (18).
P) The down mixer (9) mixes the 2.4 GHz with the 2.1 GHz to the 352 MHz IF.
Q) The signal of 352 MHz is amplified again (9) and filtered by a SAW filter (19) to give a clean signal for the second mixer.

R) The Downmixer (6) mixes the 352 MHz signal down to the I and Q signals, also the auto gain control can increase the level to the required level via line 20.

S) The very low amplitude baseband I and Q signal is amplified in the AMPs (6) to a level fitted for the Analog to Digital converters (22), which make it a proper signal for the digital signal processor.

T) The digital signal processor (22) removes the spreading as present on the signal with a so called autocorrelation function. The resulting output of the processor is a received data rate of 1, 2, 5.5 or 11 Megabits.

VCO , PLL and OSC.

U) These three form one entity to generate a single tone signal for down mixing.
There are two of these blocks available, one for the IF LO (7 and 6) (352MHz) and one for the RF LO (25 and 26) of 2050 to 2150 MHz.

V) All the PLL's and the processor (2) have one reference Crystal of 22 MHz (4) with an accuracy of 25 ppm.

General circuits:

W)Antenna Diversity.
This functin may be placed on the radio board or on extended board (as part of external antenna.
Depending on the signal strength and signal quality the Digital processor (22) can choose between the two antenna's (23) and (24) which gives the best signal. This is done initial during the training sequence in the received signal.

X) Automatic Gain control.
Depending on the signal strength and signal quality the Digital processor (22) can choose to increase or decrease the signal level at the digital input, this is done by reducing or increasing the gain in the receiver via the LNA-AGC (in 9).

Y) The Signal processor (22) can read via the MAC (2) the registers for programming all parameters for transmit/receive functions

Z) The MAC is used to do the handshaking with the PCMCIA bus (1) and handling the IEEE protocol. Also used to load the PLL frequencies and dividers, also used to interface to the FlashROM which contains all parameters for the PLL's and the Callcode.

AA) Not shown is the regulator to supply the 3.3 Volt out of the 5 Volt out of the PCMCIA Bus (1)

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Rev. A 12Apr99/BVos

INDICATION MAIN PARTS

Rev. A 12Apr99/BVos

2: HERMES

3. AT29C010

4 CDFDCJ2

5. KM68V1000

6. SA1630

7. MQE 901-704

8 + 19. L545D

9. SA2420

11 + 18. LFSN30N17C2450B

12. BFP420 + BFP450

13 + 17. BAR63

14. BAR80

16. LFJ30-07B2450

22. THESEUS-HS (High Sped)

25. MQG101-2098

26. UMA1021