CIRCUIT DESCRIPTION
(ETOMS PS2 RFWES PROJECT)

B. Controller Section.

1. Circuit Power Supply

1.1 IC U5 transform 3.3V to supply for MCU and RF module working.

1.2 U1 switch three modes as Off/On/Motor on.

2. Signal Dispose

2.1 IC U8 MCU obtain data which will be transmit to RF module starting to receiver by button and stick operation

2.2 RF module obtain signal to transmit to MCU that control Q4 Q8 to make Motor vibrate.

2.3 Y1 provide clock so that MCU procedure run.

2.4 U7 encoder switch set 1-8 ID to comply with the appointed receiver ID.

2.5 LED1 function is showing current working mode. Under analogue mode the LED will illuminate opposite go into digital mode.

2.6 LED2 on circuit display the connection status. The LED flash fast when the controller hasn't connected with receiver. The LED flash slowly under connection status and normally working condition.

1. RF Module Circuit

1.1 IC on module is combined start and receiving function with 2.44GHz IC chip. Utilize DSSS technology to complete transmission.

1.2 RFW488R on RF module oscillate to provide clock for Module IC

1.3 RFW 488C on RF module filter the signal that will be started or received.

Start and receive RF signal through coil PCB antenna.

附件2

Datasheet
October 2002
Rev. 1.03

RFWaves Ltd.

RFW102 ISM Transceiver Chipset

Key Features

- **Designed for short range wireless communication in 2.4GHz - world wide license free band**
- **Data rate – up to 1Mb per second**
- **Simple interface – 3 line digital interface**
- **Low power consumption – ideal for battery operated devices**
- **+2dBm typical peak output transmission power**
- **-80dBm typical sensitivity**
- **Typical standby current of 2.6μA**
- **Complies with FCC regulations**
- **Wide range operating voltage (2.7 – 3.6V)**
- **Direct Sequence Spread Spectrum (DSSS) 11dB processing gain**
- **Short signal acquisition time (1.2μs)**

Typical Applications

- **Home automation and security**
- **Industrial automation**
- **Peripherals: keyboards, mice, game pads**
- **Remote control devices**
- **Toys and games**

General Description

The RFW102 ISM Transceiver Chipset is a short-range, half duplex wireless radio transceiver. The transceiver is intended for use in the world wide unlicensed Industrial Scientific and Medical (ISM) band of 2400-2483.5MHz, complying with the FCC (part 15.247) and ETSI (300 328) regulations and standards. The chipset consists of 3 chips, offering small size, low power consumption and simple integration into applications.

As illustrated in Figure 2, implementing a transceiver using the RFW102 chipset is simple and easy. Only a few passive components (capacitors and inductors) are required in addition to the chipset (3 chips). In addition, an antenna of 200Ω impedance or a matching circuit to a 50Ω impedance antenna can be implemented as part of the circuit layout. The transceiver has a fully digital serial I/O interface providing a simple 3-line interface, requiring NO RF knowledge to use.

The transceiver provides a peak output power of 2dBm and data rate transfer of up to 1Mb/s.

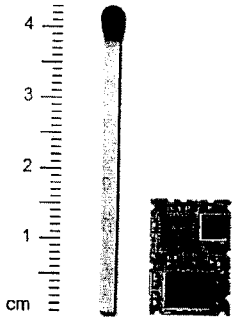


Figure 1: Actual Size of a Typical Transceiver Using RFW102 Chipset

Power consumption during transmit is extremely low (21mA in 1Mb/s, 28μA in 1Kb/s), directly depending on the bit transfer rate. During standby, ACT = GND, the transceiver consumes almost no power (2.6μA @ Vcc=3V) and features an extremely short wakeup time of 20μs. This results in a very efficient power consumption management method, by using the standby mode in a frequent manner.

The communication link between the transceivers is a Direct Sequence Spread Spectrum (DSSS) pulse pipe. The modulation scheme is 100% Amplitude Shift Keying (ASK). The spreading modulation scheme is Bi-Phase modulation where each bit has a 13 bit Barker series.

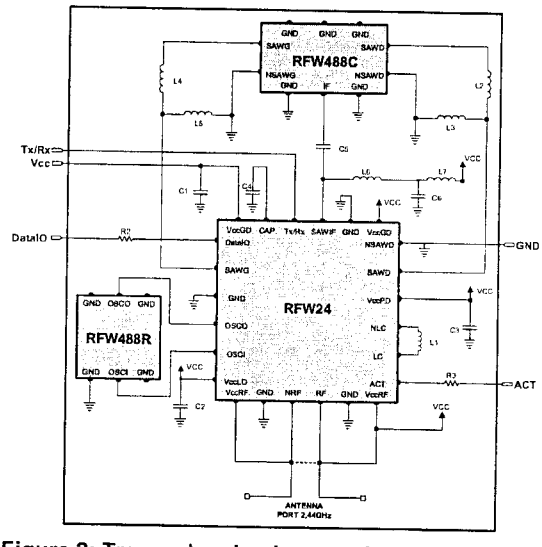


Figure 2: Transceiver Implementation - Using RFW102 Chipset

Absolute Maximum Rating

Rating	Min.	Max.	Unit
Supply Voltage	-0.3	6	V
All Input or Output Voltages with Respect to Ground	-0.3	Vcc + 0.3	V
Temperature Under Bias	-10°	70°	°C
Storage Temperature	-60°	150°	°C
Output Short-Circuit Duration (to GND)	Continues		

Stresses exceeding those listed under "Absolute Maximum Rating" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the devices at these or any other conditions, beyond those indicated in the operational sections of the datasheet, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Life Support Policy and Use in Safety-Critical Applications
RFWaves' products are not authorized for use in life-support or safety-critical applications.

Electrical Characteristics

T_A = 0 °C to +50 °C, Vcc = 2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc		2.7	3.3	3.6	V
Operating Ambient Temperature	T_a		0°	25°	50°	°C
Current Consumption in Standby Mode	I_{shdn}	ACT=GND I/O=High Z @Vcc = 3V		2.6	6.0	µA
Wakeup Time	T_{wa}			20	30	µs
Current Consumption at Wakeup Time	I_{wa}			7.5	9	mA
All input pins (DataIO, ACT, Tx/Rx)						
Rise Time	T_r		8		1000	ns
Fall Time	T_f		8		1000	ns
Input Capacitance	C_{in}				1	PF
ACT						
Logic High input	V_{ih_act}		Vcc-0.8		Vcc	V
Logic Low input	V_{il_act}		GND		0.8	V
Sink Current	I_{si_act}	ACT=Vcc		20	44	µA
Source Current	I_{src_act}	ACT=GND		2.0	4.4	µA
Tx/Rx						
Logic High input	V_{ih_tr}		Vcc-0.8		Vcc	V
Logic Low input	V_{il_tr}		GND		0.8	V
Source Current	I_{src_tr}		0.5		5	µA
Source Current in Standby Mode	I_{src_shdn}	ACT=GND	0.5		5	µA
Sink Current in Standby Mode	I_{si_shdn}	ACT=GND	0.1		1	µA
DataIO						
Source Current in Standby Mode	I_{src_shdn}	ACT=GND	0		10	µA
Sink Current in Standby Mode	I_{si_shdn}	ACT=GND	0		5	µA
Transmit to Receive Transition Time	$T_{t\_to\_r}$				1.5	µs
Receive to Transmit Transition Time	$T_{r\_to\_t}$				1.5	µs
Antenna Load		@ 2.44GHz	240\\69i	300\\73i	375\\77i	Ω
Processing Gain	PG		10	10.7	11	dB
Bit Rate			0.01		1	Mb/s

Transmitter Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Power Peak	$Pout_{max}$	@Vcc = 3.3V	-3	2	8	dBm
TxD						
Logic High input	V_{ih_d}		Vcc-0.8		Vcc	V
Logic Low input	V_{il_d}		GND		0.8	V
Source Current	I_{src_di}			4	10	µA
Sink Current	I_{si_di}			2	5	µA
Pulse Length	T_{dil}		20		Not Limited	ns
Current Consumption	Is	Bit rate = 1Kb/s[1][2]		25	37	µA
		Bit rate = 10Kb/s[1][2]		220	320	µA
		Bit rate = 100Kb/s[1][2]		2.2	3.2	mA
		Bit rate = 1Mb/s[1]	15	21	31	mA
Current Consumption – No Data Transmitted	Isnd	DataIO = 0	8	9	11	mA
Peak Current in Tx mode	Is_{max}				50	mA
Bandwidth	BW	@-20dBc			30	MHz
Out of Band Spurious (>1GHz)[3]	Spur	@RBW = 1MHz; @VBW = 10Hz			54	dBµV/m
Time from Data In to Output Power	T_d		350	400	450	ns
Transmit Time per Bit	T_{op}		650	700	750	ns

[1] When transmitting a uniform distribution of '1' and '0' bits.
[2] Burst transmission. Assuming that when not transmitting goes down to Standby mode (ACT=0).
[3] Tested using RFWaves layout and antennas with ERW102 evaluation kit. Measured from a distance of 3m.

Receiver Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Acquisition Time	T_{acq}			1.2	1.5	µs
Sensitivity	Sens	@BER= 10^{-4}		-80		dBm peak
Input Compression Point	IIP1		-35	-32		dBm
RxD						
Source Current	I_{src_do}	Vdo<Vcc-0.5	5			mA
Sink Current	I_{si_do}	Vdo>0.5	5			mA
Output Capacitance	C_{out}				1	pF
Pulse Length	T_{pw}		500	560	600	ns
Current Consumption RF power @antenna port <-40dBm peak	Is	Bit rate = 1Kb/s(1)		40	55	µA
		Bit rate = 10Kb/s(1)		380	490	µA
		Bit rate = 100Kb/s(1)		3.8	4.9	mA
		Bit rate = 1Mb/s	30	38	48	mA
Peak Current in Rx mode	Is_{max}				48	mA
Image Rejection	ImRej			30		dB
Delay Time(2)	T_{dr}		380	400	425	ns
Emission Level Between 30MHz and 1GHz					-57	dBm
Emission Level Between 1GHz and 12.75					-47	dBm

(1) Assuming that when not receiving goes down to Standby mode (ACT=0) and the receiver is synchronized with the transmitter.
(2) Time between the end of the received power and the Data Out pulse.

Transceiver Interface

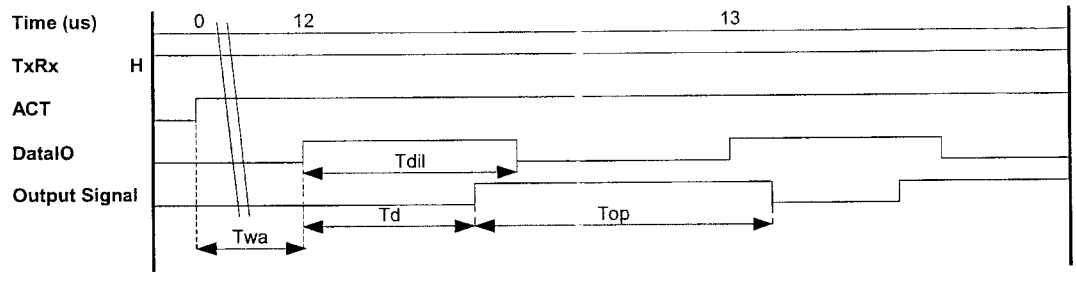
The transceiver implementation using the RFW102 chipset (see Reference Design) includes the following interface.

Name	Characteristic
Vcc	IC power supply input. A regulated voltage of 2.7-3.6Volts.
GND	Apply the supply ground to this pin.
Tx/Rx*	Mode selection input. Apply Vcc for transmit mode. Apply 0V (GND) for receive mode.
ACT*	Apply 0V (GND) for standby mode. Apply Vcc to this pin to turn the module on. It typically takes the module 20µs to wake up into a fully operational mode. CMOS-level pin.
DataIO*	In Tx mode this is an input pin, positive edge trigger. Every time TxD goes from GND to Vcc, a spread bit is transmitted. In Rx mode this is an output pin. CMOS-level pin.
RSSI	Received Signal Strength Indicator. Indicates the power transmitted in the RFW102 frequency band, allowing determining whether to transmit (Tx). Please refer to the relevant application note for more information.

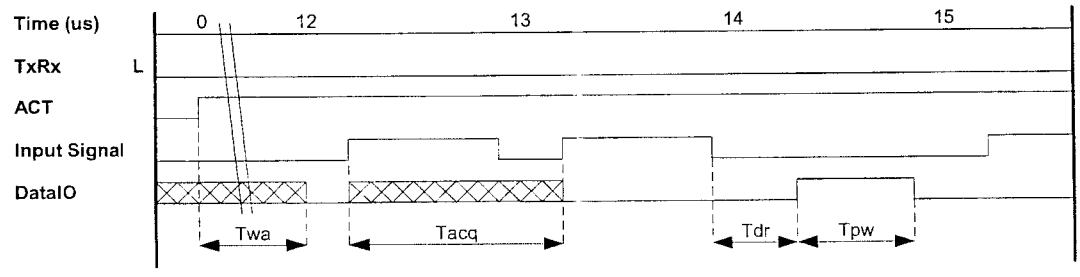
* ESD protected pin.

Timing Diagrams

Transmit Timing



Receive Timing



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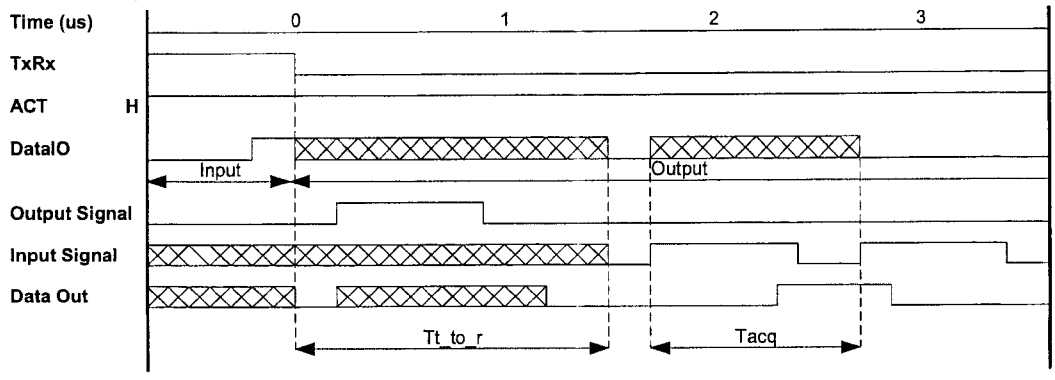
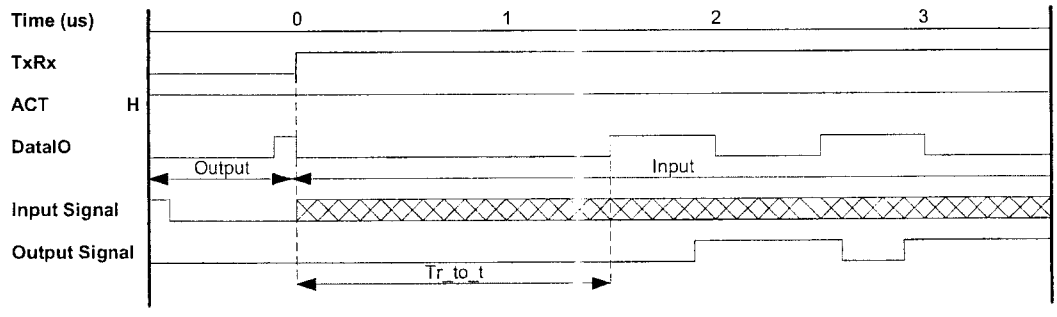
Transmit to Receive Timing



Receive to Transmit Timing



Theory of Operation

The RF Waves modem is based on a SAW correlator that functions as a spreading/de-spreading element in the system. The SAW correaltor is a 3-port passive device (described in this chapter).
Along with the SAW correlator, two other devices are embedded in the system: A 488MHz 1-port SAW resonator – provides the source of frequency for the system, and a Silicon RFIC – functions as the active part of the system. The silicon RFIC is an On Off Keying transceiver, which operates with an IF of 488MHz and a LO of 1952MHz. The SAW resonator generates both frequencies.

System overview

The chipset includes three chips:

- RFW24 – The silicon chip (RFIC) whose specification is the 'active' part of the system. It performs all the timing, amplifying, switching, transmitting and receiving functionality.
- RFW488C – A 4-pin SAW correlator, realized on a Quartz substrate. This chip is completely non-differential passive device used as a direct sequence spread spectrum spreading/de-spreading element. It functions as a transversal 13-bit BPSK Barker code correlator (a matched filter).
- RFW488R – A 1-port SAW resonator, with resonance frequency of 488MHz, serving as the system's CW oscillation source.

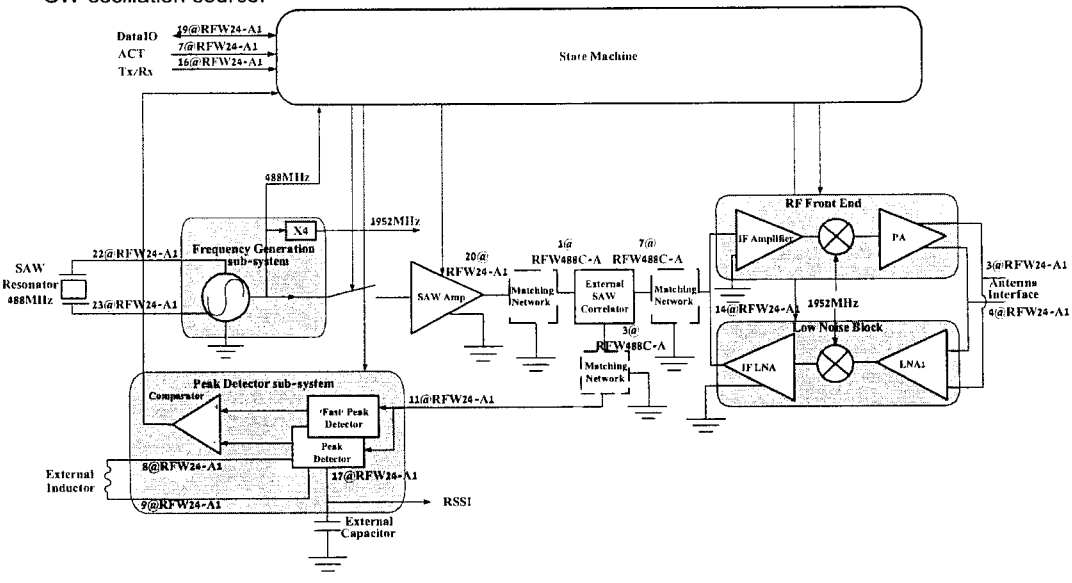


Figure 3: Detailed Block Diagram

SAW Correlator Theory

The SAW correlator is a linear passive 3-port device. It can be represented as a series of delay lines with band pass filters and phase inverters threaded between them. The current SAW correlator is a matched filter, designed to match a 13-bit BPSK – modulated Barker code.
Impedance: All 3 ports of the SAW correlators are matched by external passive elements to 200Ω. The matching circuit is presented in the schematic diagram.
Frequency of Operation: The central frequency of operation is 488MHz.
Spreading Chip Rate: The chip rate is 21 cycles/chip = 43ns/chip = 23Mcps.
Interrogation: In order to produce the spread sequence (in the transmitting side of the module) the SAW is interrogated by a 488MHz 76ns RF pulse. The pulse is characterized by a rise/fall time of 30ns and a flat time of 16ns as shown in Figure 4.

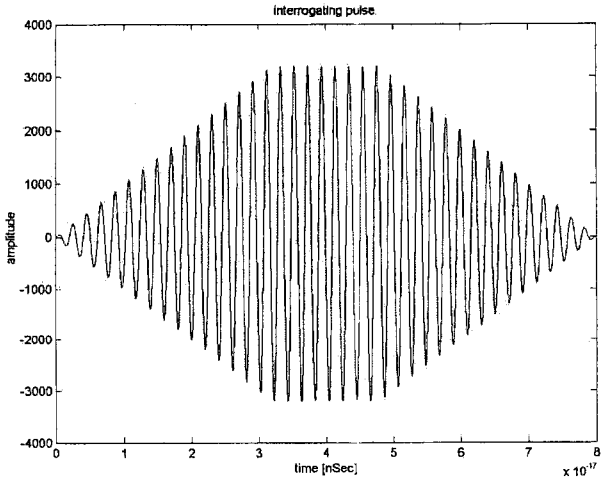


Figure 4: Interrogating Pulse – Simulated

Pulse Response

A measurement of the SAW response to the interrogating pulse is presented in Figure 5.

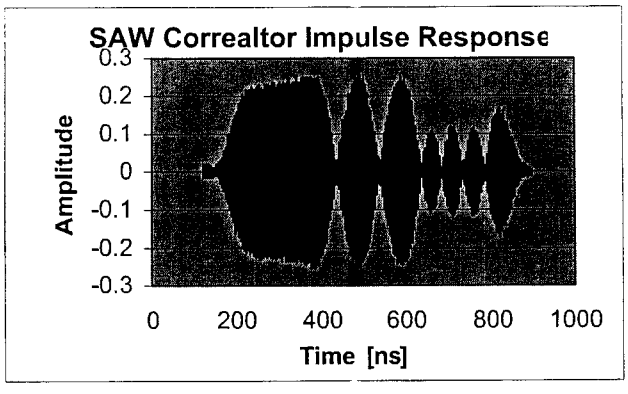


Figure 5: Pulse Response of the Correlator - Measured

Pulse Shaping and Spectral Response

The pulse shaping effect is easily noticed in the time domain. Whenever a phase inversion occurs, it involves a 'soft' envelope around it – hence lowering the side bands. A measurement of the spectral density of the signal is presented in Figure 6.

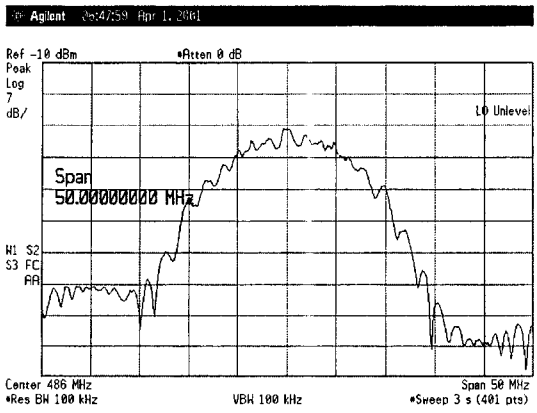


Figure 6: Spectral Density - Measured

Auto Correlation and Interference Handling

The SAW correlator functions as a matched filter building up a peak of energy when it correlates with its own impulse response. This peak is a clear mark stating the correlator has detected its own correlation function.

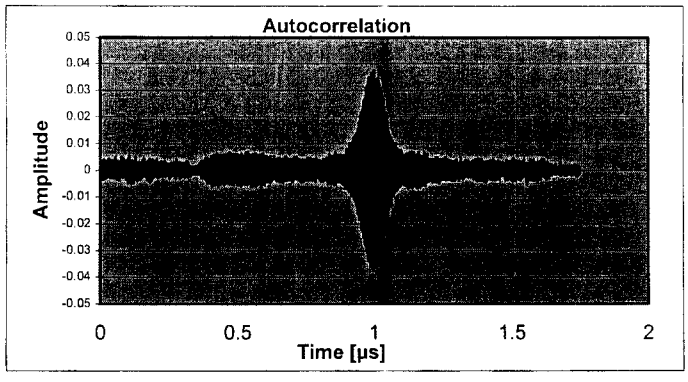


Figure 7: Autocorrelation

Numbers and Figures:

- The **Insertion Loss** of the SAW correlator is 19dB @ 488MHz, when fully tuned. Since it is a relatively wide-band element (>30MHz over a central frequency of 488MHz gives Q≈14), tuning it is an easy task – with a lot of tolerance to passives values.
- **Energy Preservation:** When a 76ns shaped pulse interrogates the SAW correlator (40ns effective pulse length) it produces a 750ns-spread sequence (see Figures above). Therefore, there is a loss of additional 10*log (750/40)≈13dB.
- The **Equivalent Noise Bandwidth** of the SAW correlator is approximately 20MHz.

Frequency Generation

The frequency generation circuit is a general-purpose element in the system. It is the only part of the system that is active in transmit and receive modes, and is off in standby mode for energy saving reasons. Its functions are to provide:

- A basic clock for the state machine
- A source for the generation of an interrogating pulse to the SAW correlator
- A source for the front end up/down conversion circuitry

The circuit consists of a SAW-resonator based oscillator (RFW488R), whose frequency is multiplied by 4 to achieve the desired up-conversion frequency. The most important feature of this circuit is the fast wakeup time (<35μs from standby to stability).

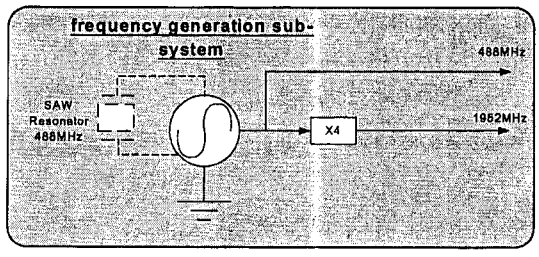


Figure 8: A Block Diagram of the Frequency Generation Sub-System

Transmission Link

Pulse Generator

The pulse generator is the element which is in charge of generating an approximately 76ns IF pulse that shall interrogate the SAW correlator. It is a state machine with a timing mechanism that switches on and off the relevant analog units that generate the pulse. The output stage is a non-differential power amplifier, matched to push maximum power to the SAW 200Ω input.
The interrogating pulse has a ramp up-ramp down envelope, to lower the spectral density of side bands.

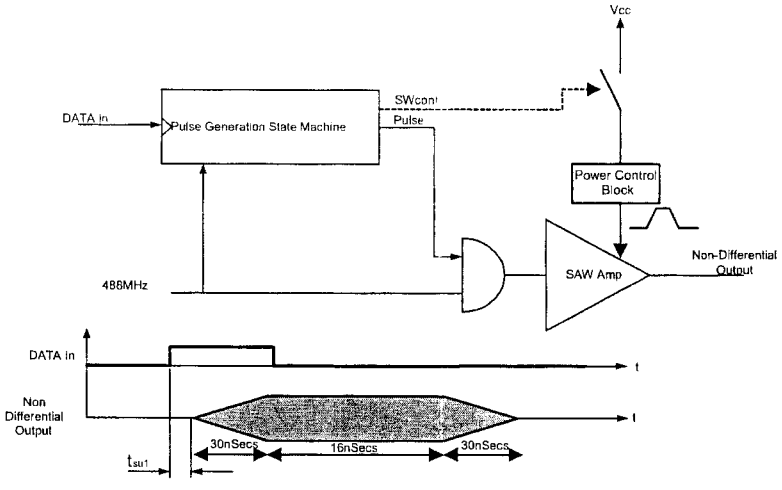


Figure 9: Pulse Generator Block Diagram

RF Front End

The RF Front End is the final stage of amplification and up-conversion prior to feeding the antenna. Its input is the 13-bit BPSK series that is the output signal of the correlator in an intermediate frequency of 488MHz, and its output is the same signal amplified by 40dB and up-converted to 2440HMz. The 1st stage of amplification is in the IF, and the 2nd is in the RF. The mixer is an image rejection mixer, with at least 35dB rejections.

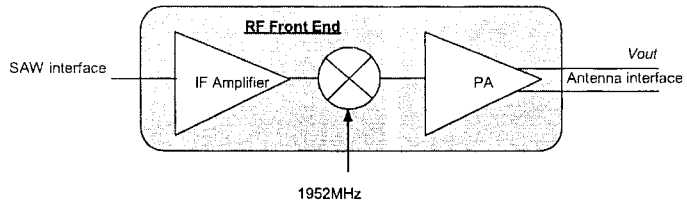


Figure 10: RF Front End Block Diagram

Receiving Link

The receiving link is a one stage down converting link, followed by a de-spreading function (implemented by the SAW correlator) and an ASK receiver. All the signal processing is done in the IF, or in the base-band. Basically, it consists of 4 elements:

- A low noise block – this element is a low noise-amplifier and a down conversion unit
- The SAW correlator – to be used as a de-spread function
- A logarithmic peak detector
- A decision stage

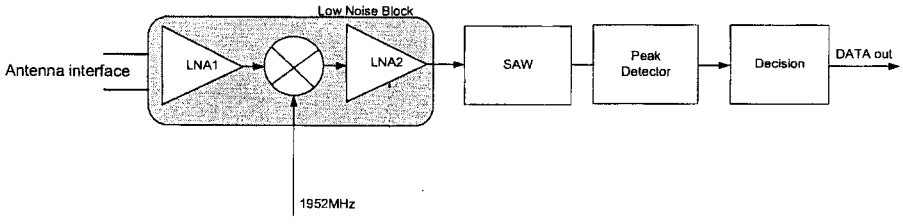


Figure 11: Receiving Link Block Diagram

Low Noise Block

The Low Noise Block is the input from the antenna on one side, and the output is attached to the SAW correlator on the other side. Since there is no RF filter between the antenna and LNA1, other than a simple printed filter, a wide dynamic range of transmitting/receiving is required, therefore, a very high dynamic range is featured in this front – end block. After this block comes the SAW correlator, which functions also as a filter that rejects out of band signals, and suppress in-band interference.

Low Noise Block (LNB) features:

- Gain: 38dB
- Source = input impedance: Antenna 200Ω (differential)
- Load (SAW Correlator): 200Ω, none differential
- Compression points:
  - Input IP1 > -35dBm
  -
- Noise figure: NF < 16dB
- Image rejection > 30dB

Peak Detector

The peak detector is the next stage after the SAW correlator. It functions as an envelope signal detector, moving from IF directly to Base Band. It is the 1st stage of the ASK receiver. Since its input may have a very high range of input signals, a high dynamic range is its main feature.

Two peak detectors are applied in parallel a 'fast' peak detector, and a 'slow' one. The difference between the two is their output bandwidth. The 'fast' peak detector has a bandwidth of 10MHz. The 'slow' peak detector has a bandwidth that will be determined by an external capacitor, connected between pin 17 and system GND.

In order to maintain the high dynamic range that is required, a logarithmic peak detector is applied. It can be modeled as $V_{out}=\alpha^{*}P_{in}$, where P_{in} is in dBm (logarithmic), and V_{out} is in volts (linear).

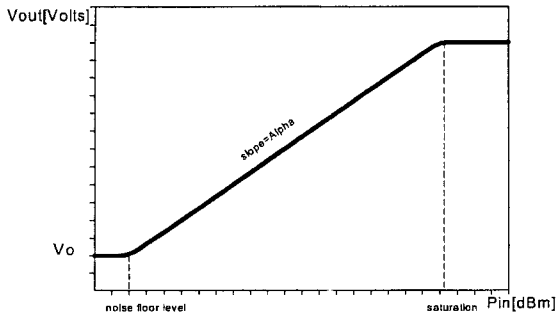


Figure 12: Peak Detector Vout (Pin) Graph

The noise floor is P_{min}, and the saturation point is P_{max}. Between these two points, the peak detector functions as follows: $\mathbf{V_{out}=V_0+\alpha*P_{in}}$.

- α[V/dB] is the slope, $\alpha \equiv 10$[mV/dB]
- $P_{max} - P_{min}$ is the dynamic range: $\mathbf{P_{min}<-82dBm}$, **Pmax> -5dBm .**
- Slope linearity: Within the dynamic range the slope α remains linear with a ±1dB tolerance.
- Central frequency of operation (detection) is 488MHz±5MHz. An external inductor is used as part of the band pass filter that defines bandwidth for the peak detector. This inductor is connected in parallel to an on-chip capacitor, between pins 8 and 9 of the silicon RFIC.
- Input impedance: 200Ω, non differential.

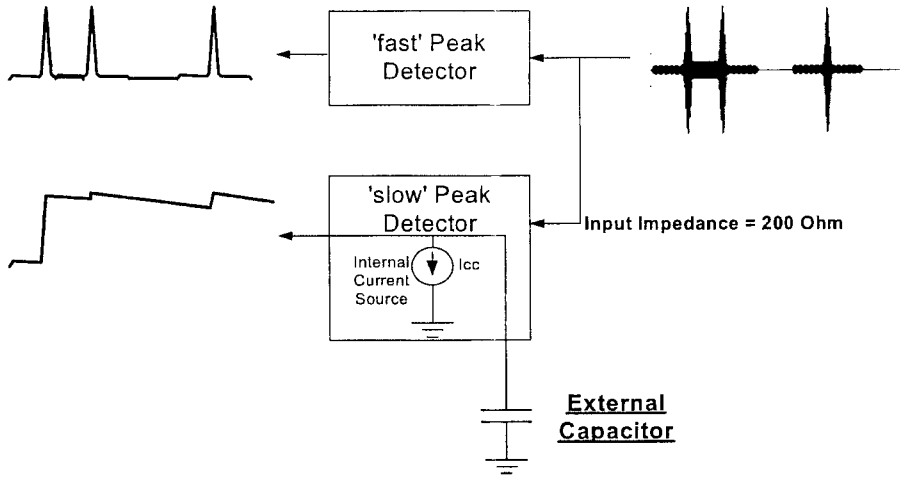


Figure 13: Peak Detectors & ASK Receiver

Determining the Values of the External Capacitor (C1 Connected to pin 17)

The time constant of the slow peak detector is determined by an external capacitor that is connected between pin 13 of the RFIC and GND.
The slow peak detector is the reference signal source for the decision stage. Since the system supports various transmitting/receiving rates, the reference signal time constant is externally controlled. The time constant can be set as an internal current source that discharges the external capacitor.
The capacitor is being charged by an internal current source, charging it to the voltage, which is the output of the peak detector. The fastest charging time is usually related to high power signals at the output of the SAW correlator. The peak charging current is 10mA.
An internal current source is constantly discharging the capacitor with a current of Icc= 0.2µA.
In order to determine the optimal value of the capacitor, one needs to consider the maximum and minimum spaces between two consecutive pulses, and the amount of faulty pulses that can be tolerated when the link is being set up.

Example1: High bit rate system

- Minimum time between consecutive pulses: 1µs.
- Maximum time between consecutive pulses: 100µs.
- Number of faulty pulses to be tolerated: 1

1. Since only one faulty pulse can be tolerated, the capacitor must be charged to its fullest voltage with the 1st pulse. Assume 82dB above noise pulse, the capacitor must be charged to 82[dB]*α[mV/dB]=82[dB]*10[mV/dB]=820[mV] within 0.5µs
Charging current is 10mA, so the maximum allowed capacitor is:

$$C_{max}=I*t/V=10[mA]*0.5[\mu s]/820[mV]=6[nF]$$

2. Since the maximum time between two consecutive pulses is 100µs, we need to keep the capacitor from discharging for at least 100µs. The discharging current is 0.2µAmps, and the allowed voltage to be discharged is V=1[dB]*α[mV/dB]=10mV.
The minimum capacitor allowed is:

$$C_{min}=I*t/V=0.2[\mu A]*100[\mu s]/10[mV]=2[nF]$$

Conclusion: a capacitor of 2-6nF will be suitable for the requirements defined above.

Example2: Low bit rate system

- Minimum time between consecutive pulses: 20µs.
- Maximum time between consecutive pulses: 500µs.
- Number of faulty pulses to be tolerated: 3

1. Since only three faulty pulses can be tolerated, the capacitor must be charged to its fullest voltage with the 3rd pulse. Assume 82dB above noise pulse, the capacitor must be charged to 82[dB]*α[mV/dB]=82[dB]*10[mV/dB]=820[mV] within 3µs, which is the equivalent of 3 1µs pulses.
Charging current is 10mA, so ignoring the intermediate discharge the maximum allowed capacitor is:

$$C_{max}=I*t/V=10[mA]*3[\mu s]/820[mV]=36[nF]$$

2. Since the maximum time between two consecutive pulses is 500µs it is required to keep the capacitor from discharging for at least 500µs. The discharging current is 0.2µAmps, and the allowed voltage to be discharged is V=1[dB]*α[mV/dB]=10mV.
The minimum capacitor allowed is:

$$C_{min}=I*t/V=0.2[\mu A]*500[\mu s]/10[mV]=10[nF]$$

Conclusion: a capacitor of 10-36nF will be suitable for the requirements defined above.

Notice: In some extreme requirements a capacitor value may not be found.

Decision Stage

The decision stage is the final one in the receiving link. It is the stage where the final signal processing is done. Its output is a digital pulse, that indicates whether a valid signal has been identified or not. It consists of an analog comparison stage followed by a simple state machine.

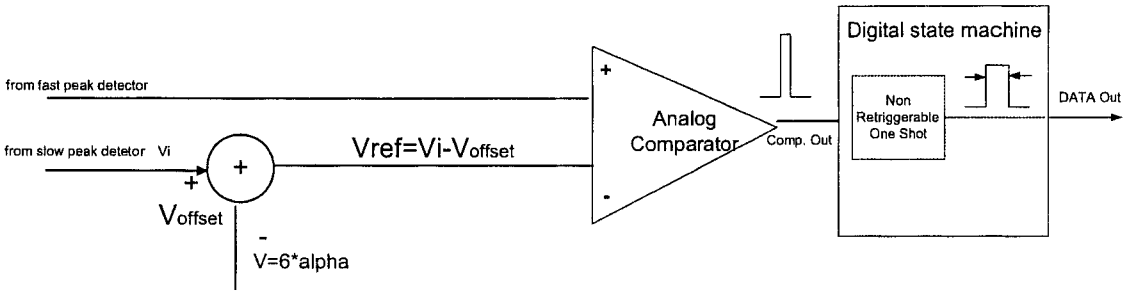


Figure 14: Decision Stage Block Diagram

A voltage offset equivalent to 6dB is subtracted from the output of the slow peak detector. This is considered an optimal threshold for ASK receivers under Gaussian white noise environment.
The first stage of the decision is an analog voltage comparator that compares the outputs of the two peak detectors. The output of the fast peak detector is connected to the positive (non-inverting) input and the output of slow peak detector (after a 6dB subtraction) is connected to the negative (inverting) input.
Following the comparator is a digital one-shot stage, intended for shaping the digital output pulse.

State Machine

The state machine is the digital part of the chip. It performs all the timing, control and digital processing of the chip.
The input signals are:

- DATA I/O – this is a high impedance input pin in the transmitting mode.
- Tx/Rx – 'H' = Tx, 'L' = Rx.
- ACT – 'LH' = device is shut down, current consumption minimal, 'HL' = device activated.
- Clk (internal 488MHz signal from the oscillator).
- Comp Out (internal signal from the analog comparator).

The output signals are:

- DATA I/O – this is a low impedance output pin in the receiving mode.
- Pulse (internal signal to the pulse generator) – positive logic signal.
- SW cont. (internal signal to the pulse generator) – 'H' enables voltage to pulse generator output amplifier.
- SW cont. (internal signal to the pulse generator) – 'H' enables voltage to pulse generator output amplifier.
- Acont (internal signal to control the power amplifier) – 'H' enables voltage to output power amplifier.
- Rxcont (internal signal to control the receiving link) – 'H' activates the receiving link. Rxcont ≡ not (Tx/Rx).

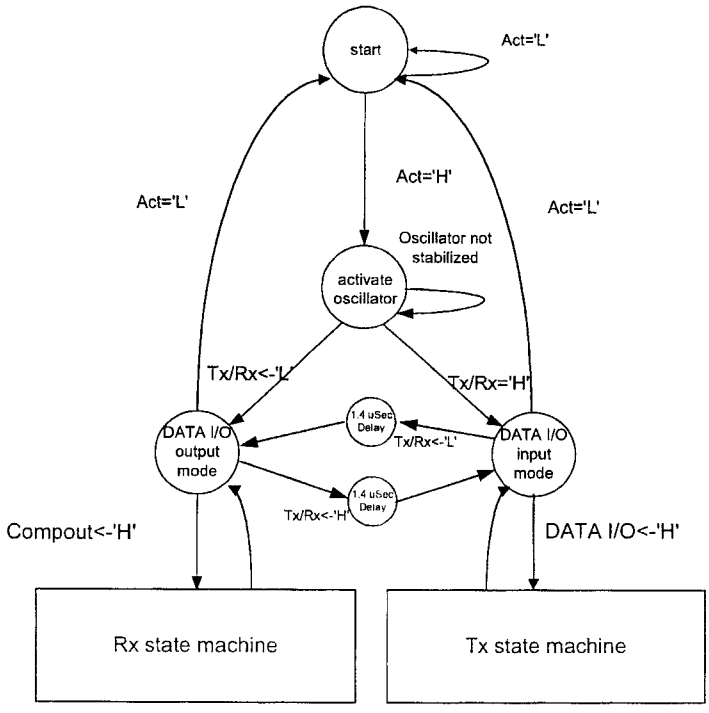


Figure 15: General State Machine Block Diagram

Pin Out

RFW24 Silicon Chip (24 pin)

Pin #	Symbol	Type[1]	Description
1	VccRF	Vcc	Supplies voltage to the RF element
2	GND		Ground
3	NRF	A	Connected to antenna
4	RF	A	Connected to antenna
5	GND		Ground
6	VccRF	Vcc	Supplies voltage to the power amplifier element
7	ACT[3]	D I	Activate pin. L - standby; H - active mode
8	LC	A	Connecting to 22nH inductor
9	NLC	A	Connecting to 22nH inductor
10	VccPD	Vcc	Supplies voltage to the peak detector element
11	SAWD[2]	A	Input to the peak detector from the RFW488C (D)
12	GND		Ground
13	VccGD	Vcc	Supplies voltage to the state machine and pulse generator elements
14	GND		Ground
15	SAWIF[2]	A	Output/Input of the IF to/from the RFW488C (IF)
16	Tx/Rx[3]	D I	Vcc - Tx mode; GND - Rx mode
17	CAP	A	Connect an external capacitor to this pin. Nominal recommended value is 2.2nF.
18	VccGD	Vcc	Supplies voltage to the state machine and pulse generator elements
19	DataIO[3]	D IO	Input/Output data
20	SAWG[2]	A	Output of the transmitted pulse as input to the RFW488C (G)
21	GND		Ground
22	OSCO	A	Connection to the resonator
23	OSCI	A	Connection to the resonator
24	VccLO	Vcc	Supplies voltage to the oscillator element
Puddle	GND		Ground.

[1] A = Analog; D = Digital.
[2] The characteristic impedance for those pins is approximately 200Ω. An impedance matching network should be used between those pins and the RFW488C correlator chip pins, depending on the characteristic impedance of each of those pins. See an implementation in the "Reference Design" section.
[3] ESD protected pin.

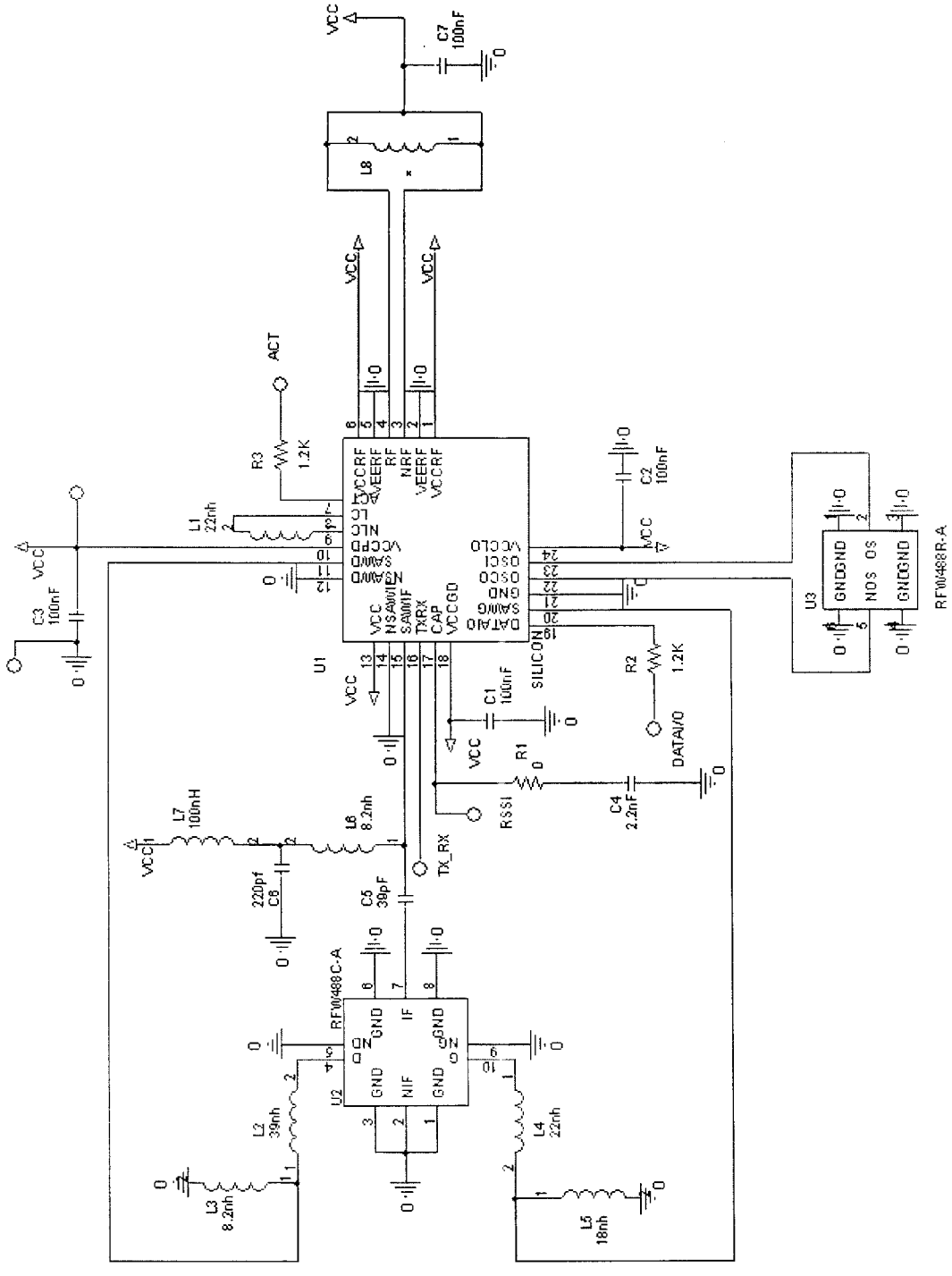
RFW488C Correlator Chip (10 pin)

Pin #	Symbol	Description
1	GND	Ground
2	NIF	Ground
3	GND	Ground
4	D	Output to the peak detector (SAWD). Characteristic impedance of pin: (5-112j)Ω @ 488MHz
5	ND	Ground
6	GND	Ground
7	IF	Output/Input to/from the IF (SAWIF) to the SAW. Characteristic impedance of pin: (3-13j)Ω @ 488MHz
8	GND	Ground
9	NG	Ground
10	G	Input of the transmitted pulse (SAWG) to the SAW. Characteristic impedance of pin: (3-13j)Ω @ 488MHz

RFW488R Resonator Chip (6 pin)

Pin #	Symbol	Description
1	GND	Ground
2	OS	The serial resonance between this pin & pin 5
3	GND	Ground
4	GND	Ground
5	NOS	The serial resonance between this pin & pin 2
6	GND	Ground

Reference Design



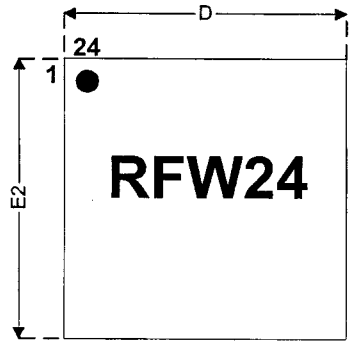
*Based on RFWaves reference design layout.

Mechanical Data

NOTES:
A. All linear dimensions are in millimeters.
B. These drawings are subject to change without notice.

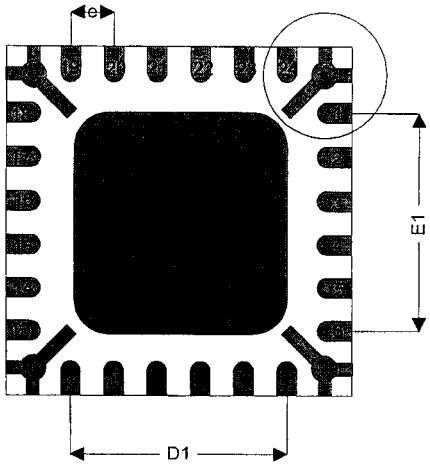
RFW24

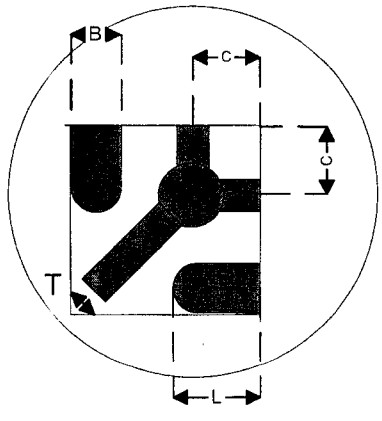
Top View



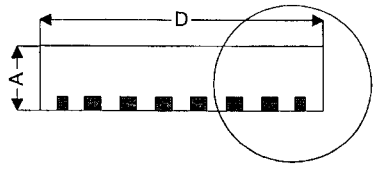
Sym.	Min	Nominal	Max
A	0.85	0.90	0.95
A1	0.18	0.20	0.22
C		0.325	
A2	0.68	0.70	0.72
D	3.90	4.00	4.10
D1		2.50 BSC	
E1		2.50 BSC	
E2	3.90	4.00	4.10
B	0.18	0.23	0.28
T	0.10	0.15	0.20
L	0.35	0.40	0.45
E		0.5	
This package is compliant with JEDEC MO-220C			

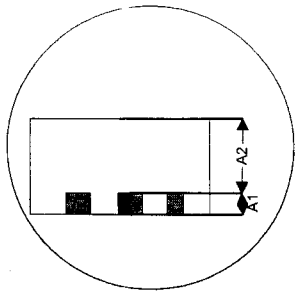
Bottom View





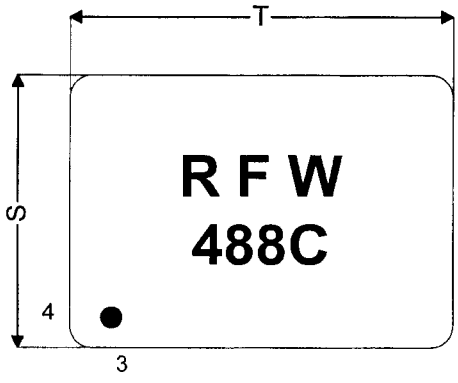
Side View





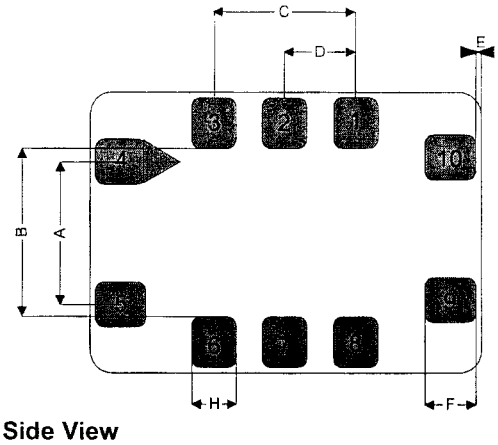
RFW488C

Top View

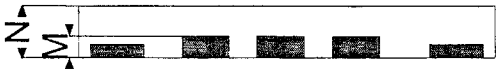


Symbol	mm	Mil
A	2.54	100.0
B	3.00	118.11
C	2.54	100.0
D	1.27	50.0
E	0.10	3.937
F	0.90	35.433
G	1.40	55.118
H	0.80	31.496
N	0.60	23.62
M	0.30	11.81
T	7.00	280.0
S	5.00	200.0

Bottom View

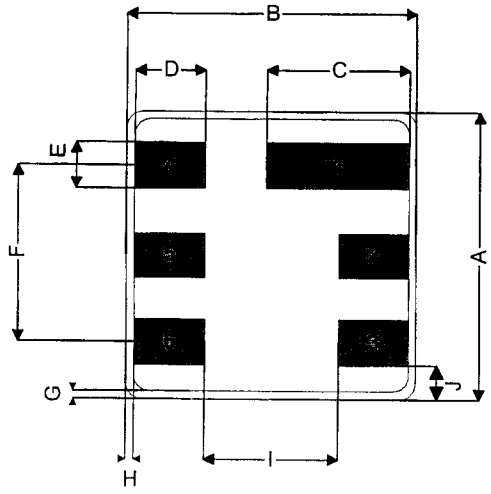


Side View



RFW488R

Bottom View



Symbol	mm
A	3.80
B	3.80
C	1.90
D	0.85
E	0.60
F	2.54
G	0.10
H	0.10
I	1.90
J	0.33
L	0.25
M	1.00

Side View

Features are subject to revisions or changes without notification

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