

CIRCUIT DESCRIPTION

JS109H(TECHCOPR PS2 NORDIC PROJECT)

A. Receiver Section

1 Signal Dispose

- 1.1 PS2 console switch data with RF module by U2 and MCU disposed
- 1.2 Y1 provide clock so that U2 procedure go on.
- 1.3 U3 switch will force change to the frequency no interfering when there is other same frequency interfering during working
- 1.4 D1 on circuit show LED light during normal working, opposite will be off.
- 1.5 D2 on circuit show LED flash during connection or no signal input. The LED will illuminate upon finished connection.

2. RF module circuit

- 2.1 IC U1 on module is combined start and receive function with 2.4G IC chip. With GFSK signal and CRC adjust and identify ID code function.
- 2.2 Y1 on module provide time standard for U1 so that firmed on normal frequency.
- 2.3 Receiving and start appointed RF signal by C8 coupling and C10 filtering then through PCB antenna completed.

Frequency Table (Frequency in GHz)

CH1	2.414	CH2	2.418	CH3	2.422
CH4	2.426	CH5	2.430	CH6	2.434
CH7	2.438	CH8	2.442	CH9	2.446
CH10	2.450	CH11	2.454	CH12	2.458
CH13	2.462	CH14	2.466	CH15	2.470
CH16	2.474				



Single chip 2.4 GHz Transceiver

nRF2401

FEATURES

- True single chip GFSK transceiver in a small 24-pin package (QFN24 5x5mm)
- Data rate 0 to 1Mbps
- Only 2 external components
- Multi Channel operation
 - 125 channels
 - Support frequency hopping
 - Channel switching time <200µs.
 - Power supply range: 1.9 to 3.6 V
- Address and CRC computation
- Shock Burst™ mode for ultra-low power operation
- Simultaneous dual receiver topology
- Low supply current (TX), typical 8mA peak @ -5dBm output power
- Data slicer / clock recovery of data
- 100% RF tested
- No need for external SAW filter
- Low supply current (RX), typical 15mA peak in receive mode
- World wide use

APPLICATIONS

- Wireless mouse, keyboard, joystick
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Intelligent sports equipment
- Industrial sensors
- Toys

GENERAL DESCRIPTION

nRF2401 is a single-chip radio transceiver for the world wide 2.4 - 2.5 GHz ISM band. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channels are easily programmable by use of the 3-wire interface. Current consumption is very low, only 8mA at an output power of -5dBm and 15mA in receive mode. Built-in Power Down modes makes power saving easily realizable.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum GFSK data rate	1000	kbps
Supply current GFSK in transmit @ -5dBm output power	8	mA
Supply current GFSK in receive mode	15	mA
Temperature range	-40 to +85	° C
Sensitivity	-85	dBm
Supply current in Power Down mode	<1	µA

Table 1 nRF2401 quick reference data

**nRF2401 Single Chip 2.4 GHz Radio Transceiver**

Type Number	Description	Version
NRF2401 IC	24 pin QFN 5x5	A
NRF2401-EVKIT	Evaluation kit (2 test PCB, 2 configuration PCB, SW)	1.0

Table 2 nRF2401 ordering information

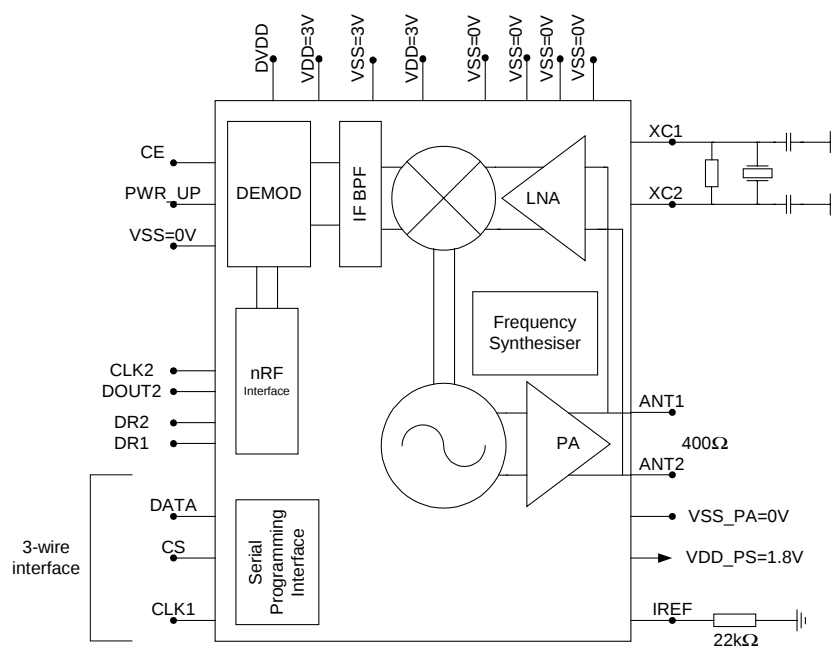
BLOCK DIAGRAM

Figure 1 nRF2401 with external components.



PIN FUNCTIONS

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	DR2	Digital Output	RX Data Ready at Channel#2
3	CLK2	Digital I/O	Clock Output/Input for RX Data Channel#2
4	DOUT2	Digital Output	RX Data Channel 2
5	CS	Digital Input	Chip Select Activates Configuration Mode
6	DR1	Digital Output	RX Data Ready at Channel#1
7	CLK1	Digital I/O	Clock Input (TX) & Output/Input (RX) for Channel#1
8	DATA	Digital I/O	RX Data Channel 1/TX Data Input/ 3-wire interface
9	DVDD	Power	Positive Digital Supply output for decoupling purposes
10	VSS	Power	Ground (0V)
11	XC2	Analog Output	Crystal Pin 2
12	XC1	Analog Input	Crystal Pin 1
13	VDD_PA	Power Output	Power Supply (+1.8V) to Power Amplifier
14	ANT1	RF	Antenna interface 1
15	ANT2	RF	Antenna interface 2
16	VSS_PA	Power	Ground (0V)
17	VDD	Power	Power Supply (+3V DC)
18	VSS	Power	Ground (0V)
19	IREF	Analog Input	Reference current
20	VSS	Power	Ground (0V)
21	VDD	Power	Power Supply (+3V DC)
22	VSS	Power	Ground (0V)
23	PWR_UP	Digital Input	Power Up
24	VDD	Power	Power Supply (+3V DC)

Table 3 nRF2401 pin function

PIN ASSIGNMENT

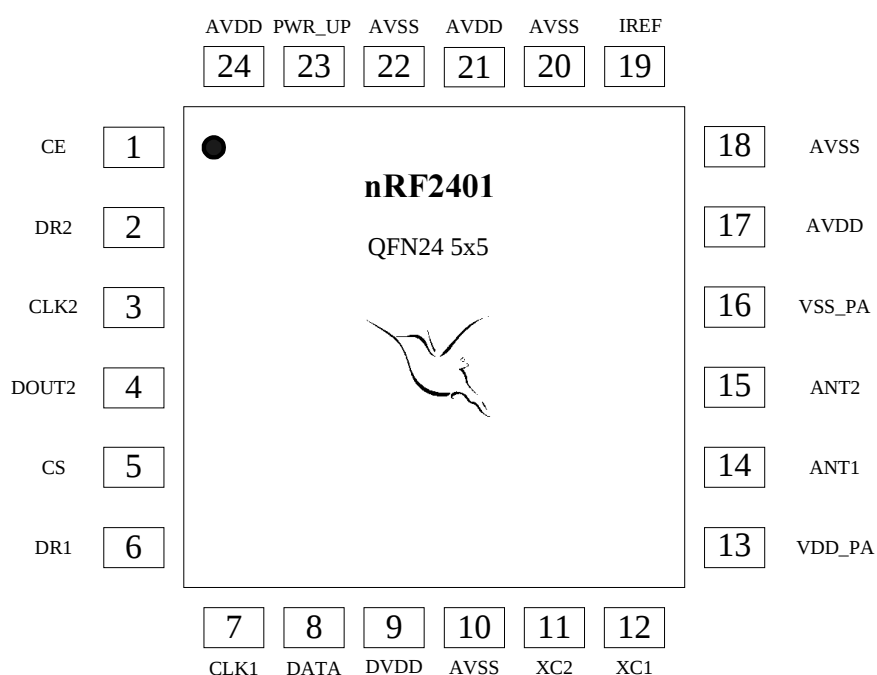


Figure 2. nRF2401 pin assignment (top view) for a QFN24 5x5 package.



ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, T_A = - 40°C to + 85°C

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Operating conditions						
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	27	85	°C
Digital input pin						
V _{IH}	HIGH level input voltage		VDD- 0.3		VDD	V
V _{IL}	LOW level input voltage		Vss		0.3	V
Digital output pin						
V _{OH}	HIGH level output voltage (I _{OH} =-0.5mA)		VDD- 0.3		VDD	V
V _{OL}	LOW level output voltage (I _{OL} =0.5mA)		Vss		0.3	V
General RF conditions						
f _{OP}	Operating frequency	1)	2400		2524	MHz
f _{XTAL}	Crystal frequency	2)	4		20	MHz
Δf	Frequency deviation		±115	±158	±175	kHz
R _{GFSK}	GFSK data rate Shock Burst™		>0		1000	kbps
R _{GFSK}	GFSK data rate Direct Mode	3)	250		1000	kbps
F _{CHANNEL}	Channel spacing		1			MHz
Transmitter operation						
P _{RF}	Maximum Output Power	4)			0	dBm
P _{RFC}	RF Power Control Range		16	20		dB
P _{RFCR}	RF Power Range Control Resolution				±3	dB
P _{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P _{RF2}	2 nd Adjacent Channel Transmit Power 2MHz				-20	dBc
P _{RF3}	3 rd Adjacent Channel Transmit Power 3MHz				-40	dBc
I _{VDD}	Supply current @ 0dBm output power	5)		10	12	mA
I _{VDD}	Supply current @ -5dBm output power	5)		8	9.4	mA
I _{VDD}	Average Supply current @ -5dBm output power, Shock Burst™	6)		0.20		mA
I _{VDD}	Average Supply current in stand-by down			12		μA
I _{VDD}	Average Supply current in power down				1	μA
Receiver operation						
I _{VDD}	Supply current in receive mode			15	20	mA
RX _{SENS}	Sensitivity at 0.1%BER			-80		dBm
RX _{MAX}	Maximum Received Signal		-20			dBm
C/I _{CO}	C/I Co-channel			6	TBD	dB
C/I _{1ST}	1 st Adjacent Channel Selectivity C/I 1MHz			TBD		dB
C/I _{2ND}	2 nd Adjacent Channel Selectivity C/I 2MHz			TBD		dB
C/I _{3RD}	3 rd Adjacent Channel Selectivity C/I 3MHz			TBD		dB
RX _{IM}	Image Rejection (2 nd RF RX Channel)			TBD		dB

NOTES:

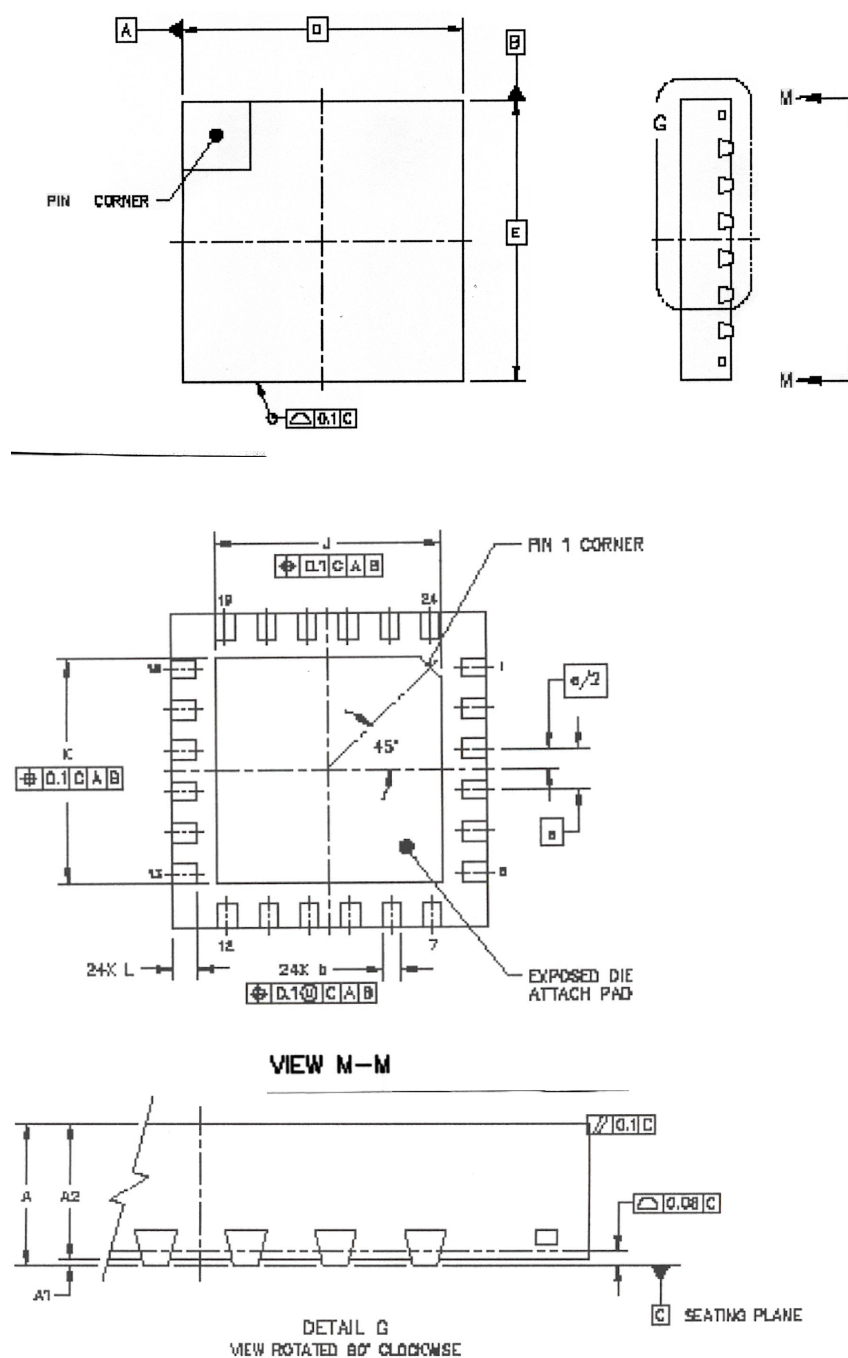
- Usable band is determined by local regulations
- The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word, see Table 8.16MHz is required for 1Mbps operation.
- Data rate must be either 250kbps or 1000kbps.
- De-embedded Antenna load impedance = 400 Ω
- De-embedded Antenna load impedance = 400 Ω. Effective data rate 250kbps or 1Mbps.
- De-embedded Antenna load impedance = 400 Ω. Effective data rate 10kbps.

Table 4 nRF2401 RF specifications



PACKAGE OUTLINE

nRF2401 uses the QFN 24LD 5x5 package. Dimensions are in mm.



Package Type		A	A ₁	A ₂	b	D	E	e	J	K	L
QFN24 (5x5 mm)	Min	0.8	0.0	0.75	0.25	5 BSC	5 BSC	0.65 BSC	3.47	3.47	0.35
	typ.				0.3				3.57	3.57	0.4
	Max	1	0.05	1	0.35				3.67	3.67	0.45

Figure 3 nRF2401 package outline.



Absolute Maximum Ratings

Supply voltages

VDD - 0.3V to + 3.6V

VSS 0V

Input voltage

V_I - 0.3V to VDD + 0.3V

Output voltage

V_O - 0.3V to VDD + 0.3V

Total Power Dissipation

P_D (T_A=85°C)..... 35mW

Temperatures

Operating Temperature.... - 40°C to + 85°C

Storage Temperature..... - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic Sensitive Device

Observe Precaution for handling.





Glossary of Terms

Term	Description
CLK	Clock
CRC	Cyclic Redundancy Check
CS	Chip Select
CE	Chip Enable
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
MCU	Micro controller
OD	Overdrive
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
ST_BY	Standby
TX	Transmit

Table 5 Glossary



MODES OF OPERATION

Overview

The nRF2401 can be set in the following main modes depending on three control pins:

Mode	PWR_UP	CE	CS
Active (RX/TX)	1	1	0
Configuration	1	0	1
Stand by	1	0	0
Power down	0	X	X

Table 6 nRF2401 main modes

For a complete overview of the nRF2401 I/O pins in the different modes please refer to Table 7.

Active modes

The nRF2401 has two active (RX/TX) modes:

- Shock Burst™
- Direct Mode

The device functionality in these modes is decided by the content of a configuration word. This configuration word is presented in configuration section.



Shock Burst™

The Shock Burst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling an extremely reduction in power consumption.

When operating the nRF2401 in Shock Burst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.

By putting all high speed signal processing related to RF protocol on-chip, the nRF2401 offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly reduced risk of 'on-air' collisions due to short transmission time

The nRF2401 can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.

By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the nRF Shock Burst™ mode reduces the average current consumption in applications considerably.

Shock Burst™ principle

When the nRF2401 is configured in Shock Burst™, TX or RX operation is conducted in the following way (20 Kbps for the example only).

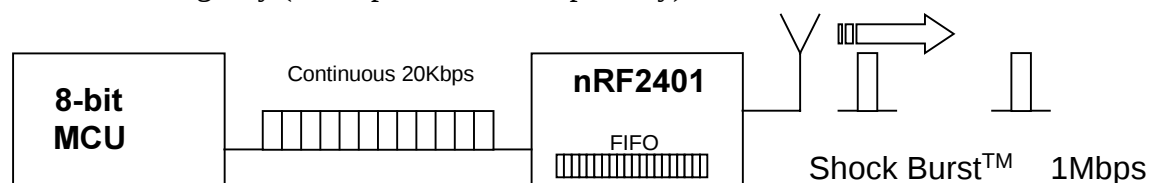


Figure 4 Clocking in data with MCU and sending with Shock-Burst™ technology

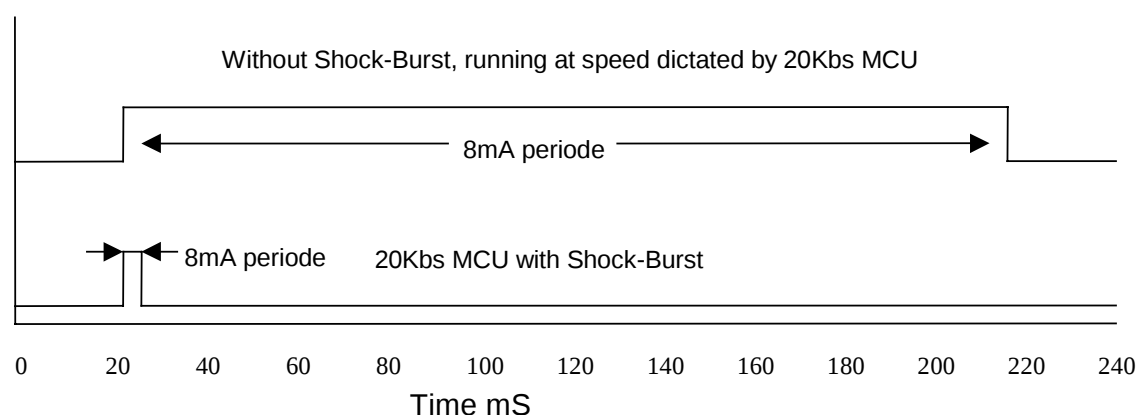


Figure 5 Current consumption with & without Shock-Burst™ technology



TX:

MCU interface pins: CE, CLK1, DATA

1. When the application MCU has data to send, set CE high. This activates nRF2401 on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the nRF2401. The application protocol or MCU sets the speed (ex: 20kbps).
3. MCU sets CE low, this activates a nRF2401 Shock Burst™ transmission.
4. nRF2401 Shock Burst™:
 - RF front end is powered up
 - RF package is completed (preamble added, CRC calculated)
 - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
 - nRF2401 return to stand-by when finished

RX:

MCU interface pins: CE, DR1, CLK1 and DATA (one RX channel receive)

1. Correct address and size of payload of incoming RF packages are set when nRF2401 is configured to Shock Burst™ RX.
2. To activate RX, set CE high.
3. After 200 µs settling, nRF2401 is monitoring the air for incoming communication.
4. When a valid package has been received (correct address and CRC found), nRF2401 removes the preamble, address and CRC bits.
5. nRF2401 then notifies (interrupts) the MCU by setting the DR1 pin high.
6. MCU may (or may not) set the CE low to disable the RF front end (low current mode).
7. The MCU clock out just the payload data at a suitable rate (ex. 20 kbps).
8. When all payload data is retrieved nRF2401 sets DR1 low again, and is ready for new incoming data package if CE is kept high during data download. If the CE was set low, a new start up sequence can begin, see Figure 13.



Direct Mode

In direct mode the nRF2401 works like a traditional RF device. Data must be at 1Mbps, or 250kbps at low data rate setting, for the receiver to detect the signals.

TX:

MCU interface pins: CE, DATA

1. When application MCU has data to send, set CE high
2. The nRF2401 RF front end is now immediately activated, and after 200 μ s settling time, data will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

RX:

MCU interface pins: CE, CLK1, and DATA

1. Once the nRF2401 is configured and powered up (CE high) in direct RX mode, DATA will start to toggle due to noise present on the air.
2. CLK1 will also start to toggle as nRF2401 is trying to lock on to the incoming data stream.
3. Once a valid preamble arrives, CLK1 and DATA will lock on to the incoming signal and the RF package will appear at the DATA pin with the same speed as it is transmitted.
4. To enable the demodulator to re-generate the clock, the preamble (8 bit) must be a square wave with frequency of 125 kHz (250 kbps) or 500 kHz (1 Mbps). After this, data may have any frequency content.
5. In this mode no data ready (DR) signals is available. Address and checksum verification must also be done in the receiving MC.

Simultaneous Two Channel Receive Mode

In both Shock Burst™ & Direct modes the nRF2401 can facilitate simultaneous two parallel receiving channels at the maximum data rate.

This means:

- nRF2401 can receive data from two 1 Mbps transmitters (ex: nRF2401 or nRF2402) 8 MHz (8 channels) apart through one antenna interface.
- The output from the two RX channels is fed to two separate MCU interfaces.
 - Receive channel 1: CLK1, DATA
 - Receive channel 2: CLK2, DOUT2.
 - In Shock Burst™ DR1 and DR2 are also available.

The nRF2401 provides 2 separate dedicated frequency channels for Rx and so replaces the need for two, stand alone receiver systems.

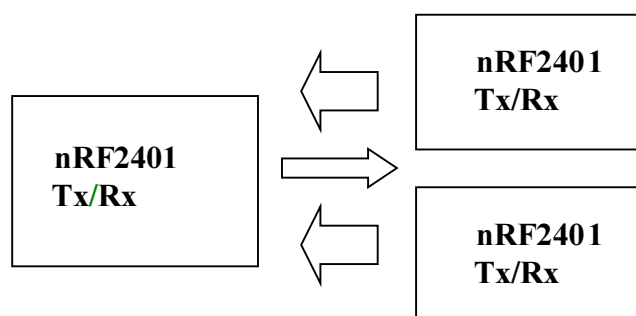


Figure 6 Simultaneous 2 channel receive on nRF2401

Configuration Mode

In configuration mode a configuration word of up to 15 bytes is downloaded to nRF2401. This is done through a simple 3-wire interface (CS, CLK1 and DATA). For more information on configuration please refer to the nRF2401 Device configuration chapter, page14.

Stand-By Mode

Stand by mode is used to minimize average current consumption while maintaining short start up times. In this mode, part of the crystal oscillator is active. Current consumption is dependent on crystal frequency (Ex: 12 μ A @ 4 MHz, 32 μ A @ 16 MHz). The configuration word content is maintained during stand by.

Power Down Mode

In power down the nRF2401 is disabled with minimal current consumption, typically less than 1 μ A. Entering this mode when the device is not active minimizes average current consumption, maximizing battery lifetime. The configuration word content is maintained during power down.

PRELIMINARY PRODUCT SPECIFICATION



nRF2401 Single Chip 2.4 GHz Radio Transceiver

nRF2401 MODES	INPUT PINS			BIDIR PINS			OUTPUT PINS		
	PWR_UP	CE	CS	direction	direction	direction	DR1	DR2	DOUT2
				CLK1	DATA	CLK2			
Power down	0	0	X	In	In	In	0	0	0
				X	X	X			
Stand by	1	0	0	In	In	In	0	0	0
				X	X	X			
Configuration	1	0	1	In	In	In	0	0	0
				CLK	CONFIG DATA	CLK			
TX Shock Burst™	1	1	0	In	In	In	0	0	0
				CLK	DATA	X			
TX Direct	1	1	0	In	In	In	0	0	0
				Set to 0	DATA	CLK			
RX Shock Burst™ in one channel	1	1	0	In	Out	In	DR1	0	0
				CLK	DATA	CLK			
RX Shock Burst™ in two channels	1	1	0	In	Out	In	DR1	DR2	DATA
				CLK	DATA	CLK			
RX Direct in one channel	1	1	0	Out	Out	Out	0	0	0
				CLK	DATA	0			
RX Direct in two channels	1	1	0	Out	Out	Out	DR1	DR2	DATA
				CLK	DATA	CLK			

Table 7 Pin configuration of nRF2401.



DEVICE CONFIGURATION

All configuration of the nRF2401 is done via a 3-wire interface to a single configuration register. The configuration word can be up to 15 bytes long for Shock Burst™ use (two channel receive) and up to 2 bytes long for direct mode.

Configuration for Shock Burst™ operation

The configuration word in Shock Burst™ enables the nRF2401 to handle the RF protocol. Once the protocol is completed and loaded into nRF2401 only one byte, also used in direct mode, needs to be updated during actual operation.

The configuration blocks dedicated to Shock Burst™ is as follows:

- Payload section width: Specifies the number of payload bits in a RF package. This enables the nRF2401 to distinguish between payload data and the CRC bytes in a received package.
- Address width: Sets the number of bits used for address in the RF package. This enables the nRF2401 to distinguish between address and payload data.
- Address (RX Channel 1 and 2): Destination address for received data.
- CRC: Enables nRF2401 on-chip CRC generation and de-coding.

NOTE:

These configuration blocks, with the exception of the CRC, are dedicated for the packages that a nRF2401 is to receive!

In TX mode, the MCU must generate an address and a payload section that fits the configuration of the nRF2401 that is to receive the data.

When using the nRF2401 on-chip CRC feature ensure that CRC is enabled and uses the same length for both the TX and RX devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC
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Figure 7 Data packet set-up

Configuration for Direct Mode operation

For direct mode operation only the two first bytes (bit[15:0]) of the configuring word is relevant.

**Configuration Word overview**

	Bit position	Number of bits	Name	Function
Shock Burst™ configuration	119	8	DATA2_W	Length of data payload section RX channel 2
	111	8	DATA1_W	Length of data payload section RX channel 1
	103	40	ADDR2	Up to 5 byte address for RX channel 2
	63	40	ADDR1	Up to 5 byte address for RX channel 1
	23	6	ADDR_W	Number of address bits (both RX channels).
	17	1	CRC_L	8 or 16 bit CRC
	16	1	CRC_EN	Enable on-chip CRC generation/checking.
General device configuration	15	1	RX2_EN	Enable two channel receive mode
	14	1	CM	Communication mode (Direct or Shock Burst™)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12	3	XO_F	Crystal frequency
	9	2	RF_PWR	RF output power
	7	7	RF_CH#	Frequency channel
	0	1	RXEN	RX or TX operation

Table 8 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS.

NOTE!

On the falling edge of CS, the nRF2401™ updates the number of bits actually shifted in during the last configuration.

Ex:

If the nRF2401 is to be configured for 2 channel RX in Shock Burst™, a total of 120 bits must be shifted in during the first configuration after VDD is applied.

Once the wanted protocol, modus and RF channel are set, only one bit (RXEN) is shifted in to switch between RX and TX.



Configuration Word Detailed Description

The following describes the function of the 120 bits (bit 119 = MSB) that is used to configure the nRF2401.

Shock Burst™ configuration:

The section B[119:16] contains the segments of the configuration register dedicated to Shock Burst™ operational protocol. After VDD is turned on Shock-Burst configuration is done once and remains set whilst VDD is present. During operation only the first byte for frequency channel and RX/TX switching need to be changed.

DATA_x_W

DATA2_W							
119	118	117	116	115	114	113	112

DATA1_W							
111	110	109	108	107	106	105	104

Table 9 Number of bits in payload.

Bit 119 – 112:

DATA2_W: Length of RF package payload section for receive-channel 2.

Bit 111 – 104:

DATA1_W: Length of RF package payload section for receive-channel 1.

NOTE:

The total number of bits in a Shock Burst™ RF package may not exceed 256!
Maximum length of payload section is hence given by:

$$DATAx_W(bits) = 256 - ADDR_W - CRC$$

Where:

ADDR_W: length of RX address set in configuration word B[23:18]

CRC: check sum, 8 or 16 bits set in configuration word B[17]

PRE: preamble, 4 or 8 bits are automatically included

As one can see shorter address and CRC leaves more room for payload data in each package.

**ADDRx**

ADDR2											
103	102	101		71	70	69	68	67	66	65	64

ADDR1											
63	62	61		31	30	29	28	27	26	25	24

Table 10 Address of receiver #2 and receiver #1.

Bit 103 – 64:

ADDR2: Receiver address channel 2, up to 40 bit.

Bit 63 – 24: ADDR1

ADDR1: Receiver address channel 1, up to 40 bit.

NOTE!

Bits in ADDR_x exceeding the address width set in ADDR_W are redundant and can be set to logic 0.

ADDR_W & CRC

ADDR_W						CRC_L	CRC_EN
23	22	21	20	19	18	17	16

Table 11 Number of bits reserved for RX address + CRC setting.

Bit 23 – 18:

ADDR_W: Number of bits reserved for RX address in Shock Burst™ packages.

NOTE:

Maximum number of address bits is 40 (5 bytes). Values over 40 in ADDR_W are not valid.

Bit 17:

CRC_L: CRC length to be calculated by nRF2401 in Shock Burst™.
 Logic 0: 8 bit CRC
 Logic 1: 16 bit CRC

Bit 16:

CRC_EN: Enables on-chip CRC generation (TX) and verification (RX).
 Logic 0: On-chip CRC generation/checking disabled
 Logic 1: On-chip CRC generation/checking enabled

NOTE:

An 8 bit CRC will increase the number of payload bits possible in each Shock Burst™ data packet, but will also reduce the system integrity.

**General device configuration:**

This section of the configuration word handles RF and device related parameters.

Modes:

RX2_EN	CM	RFDR_SB	XO_F			RF_PWR	
15	14	13	12	11	10	9	8

Table 12 RF operational settings.

Bit 15:

RX2_EN:

Logic 0: One channel receive

Logic 1: Two channels receive

NOTE:

In two channels receive, the nRF2401 receives on two, separate frequency channels simultaneously. The frequency of receive channel 1 is set in the configuration word B[7-1], receive channel 2 is always 8 channels (8 MHz) above receive channel 1.

Bit 14:

Communication Mode:

Logic 0: nRF2401 operates in direct mode.

Logic 1: nRF2401 operates in Shock Burst™ mode

Bit 13:

RF Data Rate:

Logic 0: 250 kbps

Logic 1: 1 Mbps

NOTE:

Utilizing 250 kbps instead of 1Mbps will improve the receiver sensitivity by 9 dB. 1Mbps requires 16MHz crystal.

Bit 12-10:

XO_F: Selects the nRF2401 crystal frequency to be used:

XO FREQUENCY SELECTION			
D12	D11	D10	Crystal Frequency [MHz]
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20

Table 13 Crystal frequency setting.



Bit 9-8:

RF_PWR: Sets nRF2401 RF output power in transmit mode:

RF OUTPUT POWER		
D9	D8	P [dBm]
0	0	-20
0	1	-10
1	0	-5
1	1	0

Table 14 RF output power setting.

RF channel & direction

RF_CH#							RXEN
7	6	5	4	3	2	1	0

Table 15 Frequency channel + RX / TX setting.

Bit 7 – 1:

RF_CH#: Sets the frequency channel the nRF2401 operates on.

The channel frequency in *transmit* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz}$$

RF_CH #: between 2400MHz and 2527MHz may be set.

The channel frequency in *receiver#1* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz} \text{ (Receive at PIN\#8)}$$

RF_CH #: between 2400MHz and 2524MHz may be set.

NOTE:

The channels above 83 can only be utilized in certain territories (ex: Japan)

The channel frequency in *receiver#2* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz} + 8\text{MHz} \text{ (Receive at PIN\#4)}$$

RF_CH #: between 2408MHz and 2524MHz may be set.

Bit 0:

Set active mode:

Logic 0: transmit mode

Logic 1: receive mode

**DATA PACKAGE DESCRIPTION**

PRE-AMBLE	ADDRESS	PAYLOAD	CRC
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Figure 8 Data Package Diagram

The data packet for both Shock Burst™ mode and direct mode communication is divided into 4 sections. These are:

1. PREAMBLE	- The preamble field is a requirement for Shock-Burst and Direct modes - Preamble is 8 (or 4) bits in length <table> <tr> <td>PREAMBLE</td><td>1st BIT</td></tr> <tr> <td>01010101</td><td>0</td></tr> <tr> <td>10101010</td><td>1</td></tr> </table> - Preamble is automatically added to the data packet and thereby gives extra space for payload. - In Shock Burst™ mode the preamble is stripped from the received output data, in direct mode the preamble is transparent to the output data.	PREAMBLE	1 st BIT	01010101	0	10101010	1
PREAMBLE	1 st BIT						
01010101	0						
10101010	1						
2 ADDRESS	- The address field is required in Shock Burst™ mode. 8 to 40 bits length. - Address automatically removed from received packet in Shock Burst™ mode. In Direct mode MCU must handle address .						
3 PAYLOAD	- The data to be transmitted - In Shock-Burst mode packet size is 256 bits minus the following: (Preamble: 8 (4) bits. + Address: 8 to 40 bits. + CRC 8 or 16 bits). - In Direct mode the packet size is defined by 1Mbps for 4ms: 4000 bits minus the following: (Preamble: 8 (or 4) bits. + Address: 0 to 40 bits. + CRC: 0, 8 or 16 bits).						
4 CRC	- The CRC is optional in Shock Burst™ mode, and is not used in Direct mode. 8 or 16 bits length - The CRC is stripped from the received output data.						

Table 16 Data package



IMPORTANT TIMING DATA

The following timing applies for operation of nRF2401.

nRF2401 TIMING DATA

nRF2401 timing	Max.	Min.	Name
PWR_DWN → ST_BY mode	3ms		Tpd2sby
PWR_DWN → Active mode (RX/TX)	3ms		Tpd2a
ST_BY → TX Shock Burst™	195μs		Tsby2txSB
ST_BY → TX Direct Mode	202μs		Tsby2txDM
ST_BY → RX mode	202μs		Tsby2rx
Minimum delay from CS to data.		5μs	Tcs2data
Minimum delay from CE to data.		5μs	Tce2data
Minimum delay from DR1/2 to clk.		50ns	Tdr2clk
Maximum delay from clk to data.	50ns		Tclk2data
Delay between edges		50ns	Td
Setup time		500ns	Ts
Hold time		500ns	Th
Delay to finish internal GFSK data		1/data rate	Tfd
Minimum input clock high		500ns	Thmin
Set-up of data in Direct Mode	50ns		Tsdm
Minimum clock high in Direct Mode		300ns	Thdm
Minimum clock low in Direct Mode		230ns	Tldm

Table 17 Switching times for nRF2401

When the nRF2401 is in power down it must always settle in stand-by (Tpd2sby) before it can enter configuration or one of the active modes.

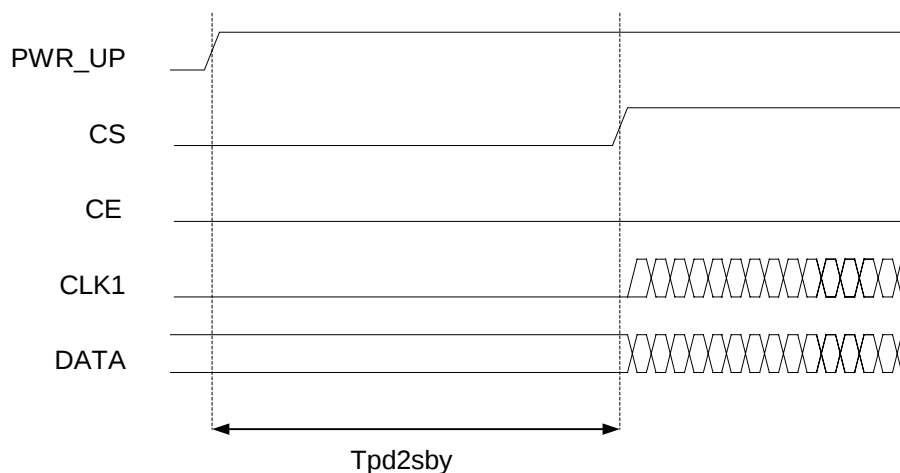


Figure 9 Timing diagram for power down (or VDD off) to stand by mode for nRF2401.

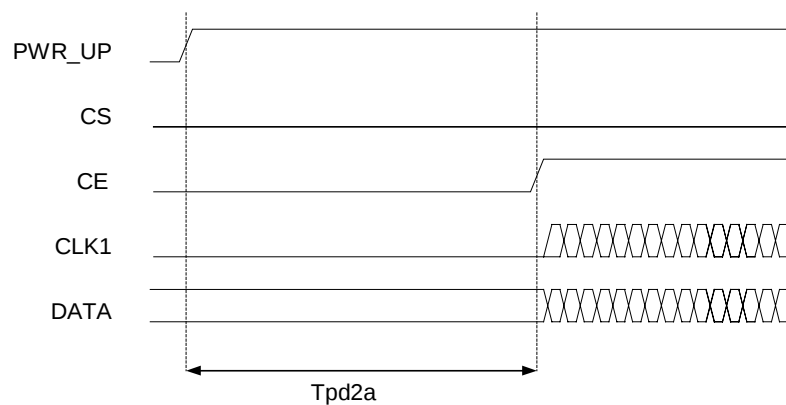


Figure 10 Power down (or VDD off) to active mode

Note that the configuration word will be lost when VDD is turned off and that the device then must be configured before going to one of the active modes. If the device is configured one can go directly from power down to the wanted active mode.

Note:

CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.



Configuration mode

When one or more of the bits in the configuration word needs to be changed the following timing apply.

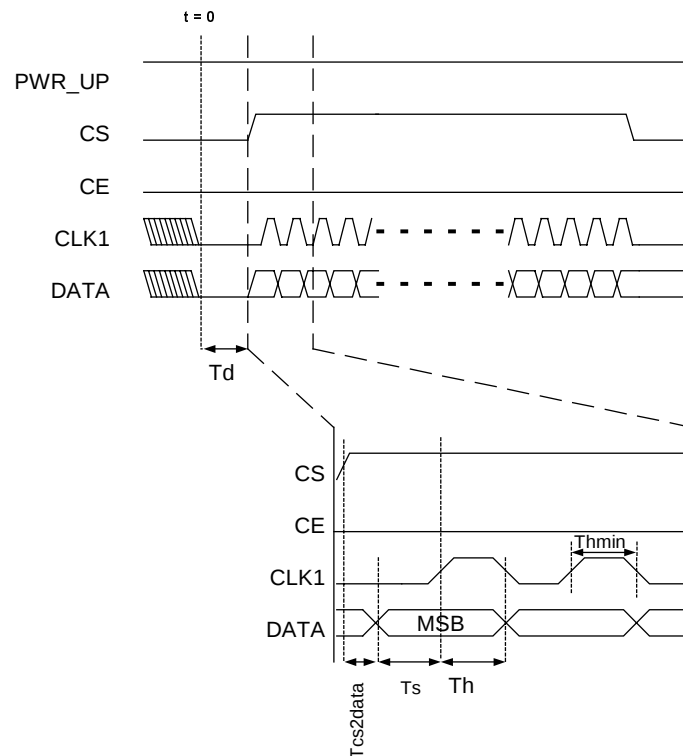


Figure 11 Timing diagram for configuration of nRF2401.

If configuration mode is entered from power down, CS can be set high after T_{pd2sby} as shown in Figure 9.



Shock Burst™ Mode

TX:

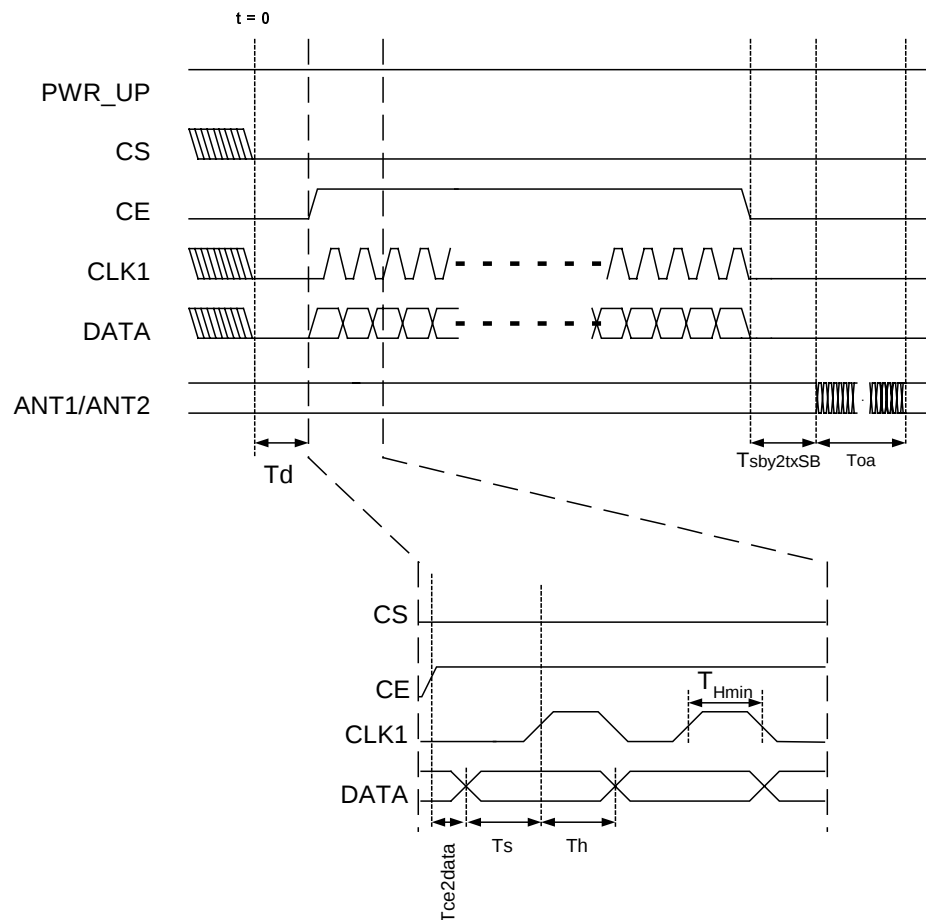


Figure 12 Timing of Shock Burst™ in TX

The package length and the data rate give the delay T_{oa} (time on air), as shown in the equation.

$$T_{OA} = 1 / \text{datarate} \cdot (\# \text{ databits} + 1)$$

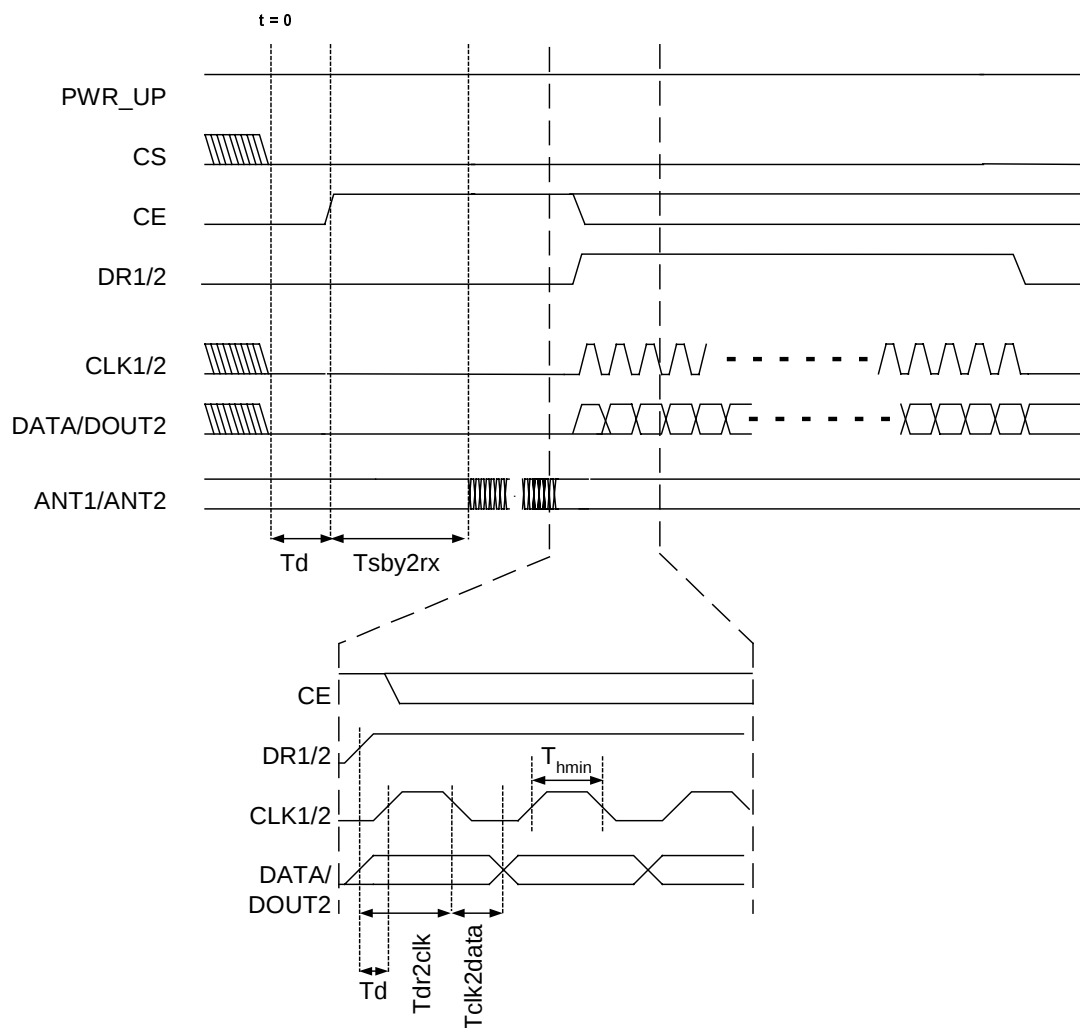
**RX:**

Figure 13 Timing of Shock Burst™ in RX

The CE may be kept high during downloading of data, but the cost is higher current consumption (15mA) and the benefit is no start-up time (200μs) after the DR1 goes low.



Direct Mode

TX:

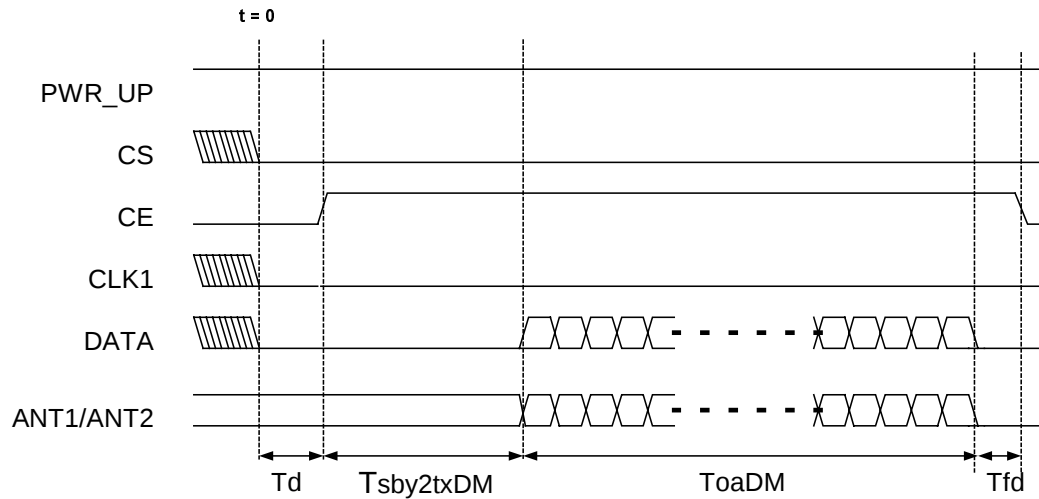


Figure 14 Timing of direct mode TX

In TX direct mode the input data will be sampled by nRF2401 and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay $T_{sby2txDM}$ is given by the equation:

$$T_{sby2txDM} = 194\mu s + 1/F_{XO} \cdot 20 + 2.25\mu s$$

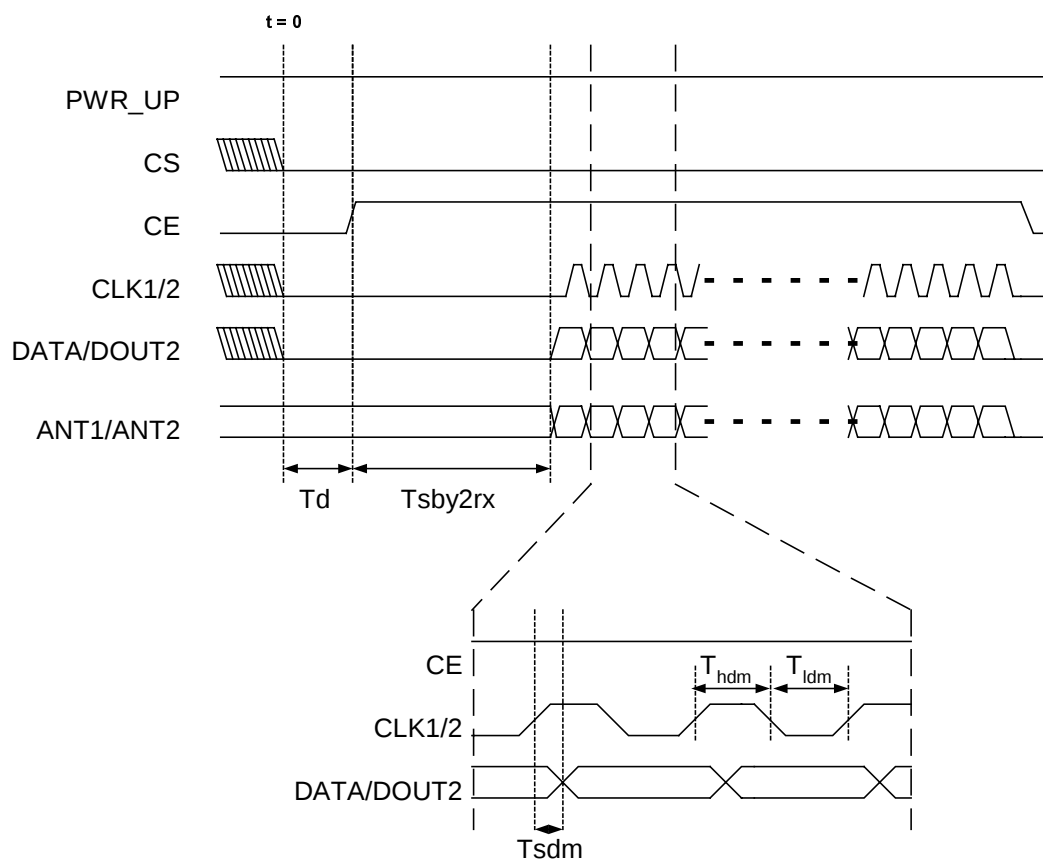
**RX:**

Figure 15 Timing of direct mode RX

T_{sby2rx} describes the delay from the positive edge of CE to the start detection of (demodulated) incoming data.



PERIPHERAL RF INFORMATION

Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700 Ω . A de-embedded load impedance i.e. impedance seen at drain terminals of the output transistors of 400 Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network.

Crystal Specification

Parallel resonant frequency: f_p = 4MHz, 8MHz, 12MHz, 16MHz, or 20MHz,

Load capacitance: C_L = 12 pF

Series resistance, ESR: R_s < 100 ohm

Crystal parallel capacitance: C_o < 7 pF

Crystal Tolerance: 30ppm

Tolerance includes initially accuracy, tolerance over temperature and aging.

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption	Comments
11	0 dBm	9.4 mA	Default
10	-5 dBm	8.0 mA	
01	-10 dBm	7.0 mA	
00	-20 dBm	6.5 mA	

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = 400 Ω .

Table 18 RF output power setting for the nRF2401.



DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 19. Definitions.

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Preliminary Product Specification: Revision Date: 06.12.2002.

Datasheet order code: 061202-nRF2401.

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