Brief Technical Information of the Body Scale

When user plugged 4 AA cells into the battery compartment, the Body Scale (here after called "the device") is ready to use.

Part A—Regarding to Schematic Diagram "Scale_v08.pdf"

The "Bridge_Sensor" outputs voltage (across ***BS-, BS+***) correlated to weight imposed on the device. It passes through an RC network (***R7, R8, C1, C21, C22***) and ends at pins ***AI+, AI-*** of ***U1***.

U1 = SN8P1919

U1 processes the voltage data and display corresponding weight information on the ***LCD*** with calibration data stored inside EEPROM ***U4***. In addition, ***U1*** stores weight data along with time information (obtained from RTC chip ***U3***) to ***U4***.

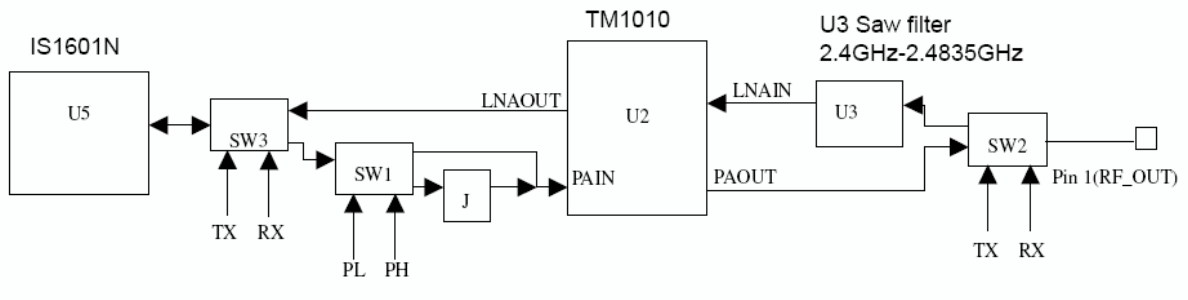
U1 will activate the Bluetooth Module by enabling the power supply to the module. This is done by setting pin 4 (***CE***) of ***U5*** to high voltage level. Pin 5 of ***U5*** will provide a steady 3.3V to the Bluetooth Module.

U1 will then send weight, time and other information to the Bluetooth Module via its ***UART_IN*** pin. Bluetooth Module will, in return, send information back to ***U1*** via ***UART_OUT*** pin of ***U1***.

After sending data out via the Bluetooth module (or after being idle for over 5 minutes), the device will enter its standby mode (power to Bluetooth Module disabled, with other measures done in order to keep current consumption low). The device leaves it standby mode by activating the vibration switch ***S2*** when user steps on the device.

Part B—Regarding to Schematic Diagram "ISBTM8-3(Class1 Module)_1120.pdf"

The Bluetooth Module communicates with ***U1*** (of "Scale_v08.pdf") via its Baseband IC ***U4*** (along with data stored inside the EEPROM U6). ***U5, U2, U3, SW1, SW2, SW3*** are the major components of the module to handle the RF part of the Bluetooth communication. The module outputs the RF signal via its pin 1 (***RF_OUT***). Pseudo-random hopping sequence is used over the total 79 channels between 2.402GHz to 2.480GHz. And with a nominal hop rate of 1600 hops/s. The transmit timming is equal to the bluetooth specification v1.1. Details illustration of the circuit can be found in the following block diagram.



SW1-3 shown about are GaAs MMIC SPDT switches to folk one signal path into two. U5 serves two functions here:

U5=IS1601N

a) ***U5*** modulates digital signal from ***U4*** to RF signal. The RF signal goes through ***SW3*** to ***SW1*** under the control of pins ***TX, RX***. This signal further goes through ***SW1*** to the Power Amplifier of ***U2***. With control pins ***PL, PH***, two different gains can be provided to the Power Amplifier where ***J*** is mainly a voltage divider consisting of ***R2-4***. Finally the signal path ends at ***SW2*** which goes to pin 1 (***RF_OUT***)

b) ***U5*** decodes RF signal received from Pin 1 (***RF_OUT***). RF signal received firstly goes through ***SW2*** to ***U3*** under the control of pins ***TX, RX***. ***U3*** is a 2.4GHZ SAW filter centered at 2442MHz. The LNA of ***U2*** amplifies the RF signal to ***SW3***. Finally, this signal reaches ***U5*** under the control pins of ***TX, RX***.

Part C -- Regarding to Schematic Diagram "Antenna.pdf"

The antenna of the device is printed on the main PCB and is connected to ***RF_OUT*** pin of the Bluetooth Module. This RF_OUT signal feeds into the antenna via a simple LC impedance matching network (L2, L3, C28).

IS1601

Bluetooth RF Transceiver

Data Sheet

Publication Release Date: Sept., 2004
Revision 1.0

TABLE OF CONTENTS

1 INTRODUCTION

1.1 General Description

The ISSC's Bluetooth radio chip is designed for short-range wireless applications. The radio integrates a complete Bluetooth class 2 transceiver, operating in the ISM frequency band, 2.4 – 2.5 GHz. The modulation is Gaussian Frequency Shift Keying, GFSK, with a BT product of 0.5 and a modulation index ranging from 0.28 to 0.35. Fast frequency hopping (1600 hops/s) is used over a total of 79 channels between 2.402 GHz up to 2.480 GHz. The channel bandwidth is 1 MHz. The chip is designed in 0.18 um RF CMOS technology for low power consumption and good RF performance. It is verified for compliance with Bluetooth Radio Specification v1.1 using a standard 36-pin QFN package.

1.2 Features

The ISSC IS1601 provides a very compact radio solution for Bluetooth applications that put extra strong requirements on low cost and small form factors. Because no off-chip radio frequency-sensitive components are needed, the ISSC IS1601 offers very cost-efficient integration directly with the target application. Neither a module nor off-chip radio design is needed. In addition, the application benefits from very low signal loss between the antenna and the radio.
The radio completely integrates the receiver and transmitter baluns, the antenna filter and switch together with the VCO tank on one single die. The fractional-N delta-sigma synthesizer and the internal crystal calibration offer support for a wide range of external reference frequency clocks or crystals. The digital Received Signal Strength Indicator (RSSI) allows for efficient power control and communication with Bluetooth class 1 devices. Several current saving modes are available.
The baseband interface is completely digital and compatible with 8-pin bi-directional BlueRF using the RXMODE2 configuration. It can automatically adapt to the voltage levels used by different baseband controllers, independently of the supply voltage.

1.3 Applicable products

The ISSC IS1601 is primarily targeting cost-sensitive consumer applications that require fast design-in, low power consumption and small designs. It is ideal for applications such as:

- 2G, 2.5G and 3G handsets
- PDA's
- Notebook PC's
- Computer peripherals
- Office network equipment
- Home applications

2 FUNCTIONAL DESCRIPTION

2.1 General

Figure 2-1 shows a block diagram of the ISSC IS1601. The circuit employs a heterodyne receiver architecture with a low intermediate frequency (IF) such that the IF filters can be integrated on-chip.
The transmitter employs direct IQ-modulation using Gaussian-filtered bit-stream data. Also included in the transmitter chain is a VCO buffer and a power amplifier (PA).
The synthesizer, the crystal oscillator block (XO), the power-on-reset (POR) and the automatic tuning functions are shared blocks between the receiver and transmitter chains.

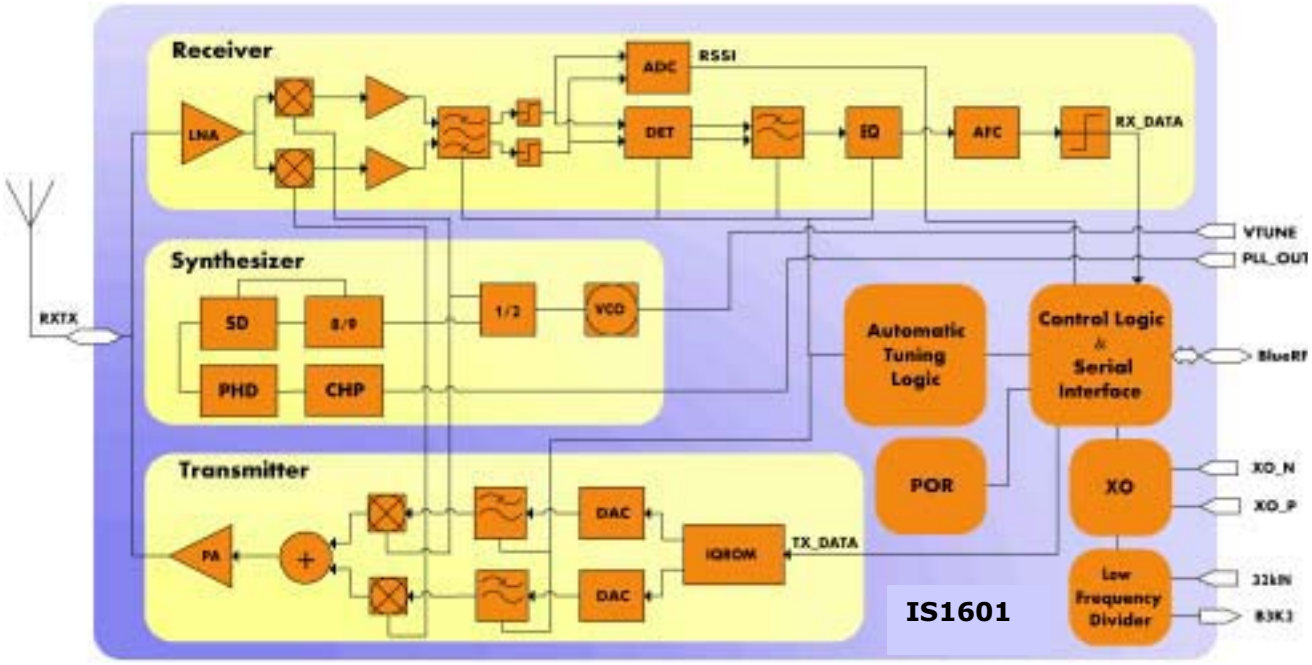


Figure 2-1. Circuit block diagram.

2.2 The Receiver Front-End

The receiver front-end consists of a low-noise amplifier (LNA) followed by two mixers and two low pass filters for the I- and Q- channels.
The IF part of the receiver front-end consists of two IF amplifiers that receive input signals from the mixers, delivering balanced I- and Q-signals to the poly-phase band-pass filter (BPF). The poly-phase BPF rejects noise and spurious signals, mainly caused by adjacent channel interference, in order to prevent unwanted signals from reaching the hard limiting stage. It also provides image frequency rejection.

The poly-phase BPF is directly followed by two hard-limiters that together generate an AD-converted RSSI signal.

2.3 The Receiver Back-End

The output of the two hard-limiters is fed into the IQ frequency discriminator, which is followed by the post-detection filter (PDF). An equalizer (EQ) processes the output of the PDF in order to improve the eye-pattern.
After equalization of the signal, the dynamic AFC (Automatic Frequency off-set Compensation) circuit and the following slicer convert the analog signal into digital data.

2.4 The Automatic Tuning Circuitry

The automatic tuning circuitry is used for tuning the band-pass filter, the detector, the post-detection filter, the equalizer and the transmit filters for process and temperature variations. The circuit also includes an offset compensation for the FM detector.

2.5 The Synthesizer

The ISSC IS1601 features a fractional-N sigma-delta (SD) synthesizer that is able to operate using an external reference frequency in the range of 10-20 MHz or, alternatively, 26 MHz.
The synthesizer consists of a phase detector, a charge pump, a low-pass loop filter, a programmable frequency divider, a voltage-controlled oscillator (VCO), a sigma-delta modulator and a look-up table.
The frequency divider consists of a divide-by-2 circuit, which divides the 5 GHz signal from the VCO down to 2.5 GHz, a divide-by-8-or-9 divider and a digital modulus control. The delta-sigma modulator controls the division ratio, and also generates an input channel value to the look-up table.

2.6 The Transmitter Circuitry

The transmitter consists of ROM tables, two DA converters, two low-pass filters, IQ mixers and a PA.
The ROM tables generate a digital IQ signal based on the transmit data. The output of the ROM tables is inserted into IQ-DA converters and filtered through two low-pass filters. The two signal components are mixed up to 2.5 GHz by the TX mixers and added together before being fed into the transmit PA.

2.7 The Low Frequency Circuitry

The low frequency circuitry includes an adjustable crystal oscillator (XO), an adjustable low power frequency divider, a power-on reset (POR) block and an off-chip reset input. For generation of the system clock, a 10-20 MHz or 26 MHz crystal or reference clock input can be used.
For operation in low power modes, the low frequency circuitry generates a 3.2 kHz clock. For lowest power consumption, it is synthesized from a 32.768 kHz or a 32.000 kHz signal. Alternatively, if none of these signals are present in the system, the system clock can be used as input for low power frequency generation.

2.8 The Digital Circuitry

The digital functions of ISSC IS1601 provide IQ signal generation in the transmitter, baseband interface control, filter tuning, fractional XO and PLL frequency division, and power-up control for all analog blocks. The digital circuitry also allows for programming of the analog blocks in order to compensate for process variations.

The serial interface automatically adjusts the voltage levels of the IO pins to the voltage level of the baseband controller for voltages between 1.5 V and the supply voltage. The interface has built-in timers that can be programmed for flexible timing, which effectively relaxes the real-time requirements on the baseband controller.

The logic is contained in the Control Logic & Serial Interface and the IQROM blocks shown in Figure 2-1. Scan testing is used for all logic.

3 SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings.

Parameter	Min	Max	Unit
Supply voltage	-0.3	3.3	V
Applied voltage to RXTX pin	-0.3	1.95	V
Applied voltage to all other pins	-0.3	VCC + 0.3	V
Storage temperature	-65	+150	°C

3.2 Operating Conditions

Table 3-2. Operating conditions.

Parameter	Min	Typ	Max	Unit
Supply voltage (VCC)	2.5	2.75	3.0	V
Temperature, ambient	-30	+25	+85	°C
Supply current in stand-by mode, XO inactive		50		µA
Supply current in stand-by mode, XO active		180		µA
Supply current in static RX mode		40		mA
Supply current in static TX mode		55		mA

3.3 DC Specification

Table 3-3. Electrical characteristics, VCC = 2.75V.

Parameter	Min	Typ	Max	Unit
Supply voltage on VDDQ	1.5		VCC	V
Supply current on VDDQ			1	mA
Logical high input	0.75*VDDQ		1.15*VDDQ	V
Logical low input	-0.15*VDDQ		0.36*VDDQ	V
Input capacitance, digital pins			10	pF
Logical high output	0.8*VDDQ	VDDQ		V
Logical low output		0	0.2*VDDQ	V
Load capacitance, digital pins			30	pF
Input leakage current/pin			0.5	µA
Rise/fall time all digital inputs			20	ns
Rise/fall time all digital outputs		5	10	ns

3.4 Receiver Specification

Table 3-4. Receiver specification.

Parameter	Min	Typ	Max	Unit
Input sensitivity	-80	-82	-84	dBm
IP_3 at antenna	-21			dBm
Maximum usable input level	-10	0	4	dBm
$C/I_{co\text{-}channel}$		10	11	dB
C/I_{1MHz}		-2	0	dB
C/I_{2MHz}		-33	-30	dB
C/I_{3MHz}		-44	-40	dB
C/I_{image}		-22	-15	dB
Intermodulation	-39	-37		dBm
RSSI range at the LNA input		-72...-52		dBm
RSSI absolute accuracy[1]			±6	dB
Out-of-band blocking, 30 MHz < f ≤ 2.0 GHz			-10	dBm
Out-of-band blocking, 2.0 GHz < f ≤ 2.399 GHz			-27	dBm
Out-of-band blocking, 2.498 GHz < f ≤ 3.0 GHz			-27	dBm
Out-of-band blocking, 3.0 GHz < f ≤ 12.75 GHz			-10	dBm
Spurious emissions, 30 MHz < f < 1.0 GHz			-57	dBm
Spurious emissions, 1.0 GHz < f < 12.75 GHz[2]		-75	-47	dBm

[1] RSSI accuracy is measured at –53 dBm (-80 + 6 + 20 + 1 = -53 dBm). 6 and 20 dB is added according to Bluetooth specification v1.1. One (1) dB is added to ensure that there is one level below the lower threshold of the RSSI.
[2] LO leakage

3.5 Transmitter Specification

Table 3-5. Transmitter specification.

Parameter	Min	Typ	Max	Unit
Transmit power at RXTX pin	-3	+1	+4	dBm
Settling time, ±25 kHz offset		100	120	µs
Transmit carrier drift over 1 slot	-25	0	25	kHz
Transmit carrier drift over 3 and 5 slots	-40	0	40	kHz
Modulation index	0.28	0.32	0.35	-
20 dB Bandwidth for modulated carrier	0.8	0.9	1.0	MHz
Transmit adjacent channel power $\Delta f = \pm 2$ MHz $\Delta f \geq \pm 3$ MHz		 -43	 -20 -40	 dBm dBm
Out-of-band spurious emissions 30 MHz < f ≤ 1.0 GHz, idle 1.0 GHz < f < 12.75 GHz, idle 1.8 GHz < f < 1.9 GHz, idle 5.15 GHz < f < 5.3 GHz, idle		 -57 	 -57 -47 -57 -47	 dBm dBm dBm dBm

3.6 Crystal Requirements

Table 3-6. System clock requirements.

Parameter	Min	Typ	Max	Unit
System reference clock frequency	10		20, 26	MHz
Frequency tolerance			20	ppm
Digital tuning load	0		8	pF
Digital tuning load step size		62.5		fF

Table 3-7. Low power clock requirements.

Parameter	Min	Typ	Max	Unit
Low power clock frequency		32.000 32.768		kHz kHz
Frequency tolerance			200	ppm

4 I/O SIGNAL DESCRIPTION

4.1 Pin Description

Table 4-1. Pin description. A = Analog, D = Digital, PS = Power supply, TP = Test Point.

Item	Pin name	Type	Direction	Description
1	VCC	PS		
2	GND	PS		
3	TEST_ENABLE	D	I	Scantest enable
4	BXTLEN	D	I	BRCLK enable
5	BnPWR	D	I	External reset, active low
6	VCC	PS		
7	GND	PS		
8	BPOR	D	O	Reset signal to baseband controller
9	BPKTCTL	D	I	Access code indication during receive slot, transmit power-up signal preceding transmit slot
10	BnDEN	D	I	DBUS Enable
11	BDDATA	D	IO	DBUS Data
12	BDCLK	D	I	DBUS Clock
13	BDATA1	D	IO	Transmit/receive data
14	BRCLK	D	O	System clock output
15	B3K2	D	O	3.2 kHz clock output
16	32kIN	D	I	32.000 or 32.768 kHz input frequency
17	GND	PS		
18	VDDQ	PS		Supply voltage for digital IO
19	XO_N	A	IO	Crystal negative input
20	XO_P	A	IO	Crystal positive input or external clock input
21	VCC	PS		
22	GND	PS		
23	PLL_OUT	A	O	Charge pump output
24	GND	PS		
25	VTUNE	A	I	VCO tune input
26	GND	PS		
27	VCC	PS		
28	TP6	TP		Test point 6
29	TP5	TP		Test point 5
30	GND	PS		
31	RXTX	A	IO	Antenna IO
32	GND	PS		
33	TP4	A		Test point 4
34	TP3	A		Test point 3
35	TP2	A		Test point 2
36	XODIV2_OFF or TP1	A		Reference clock division disable, active high, or Test point 1

4.2 Pin-Out

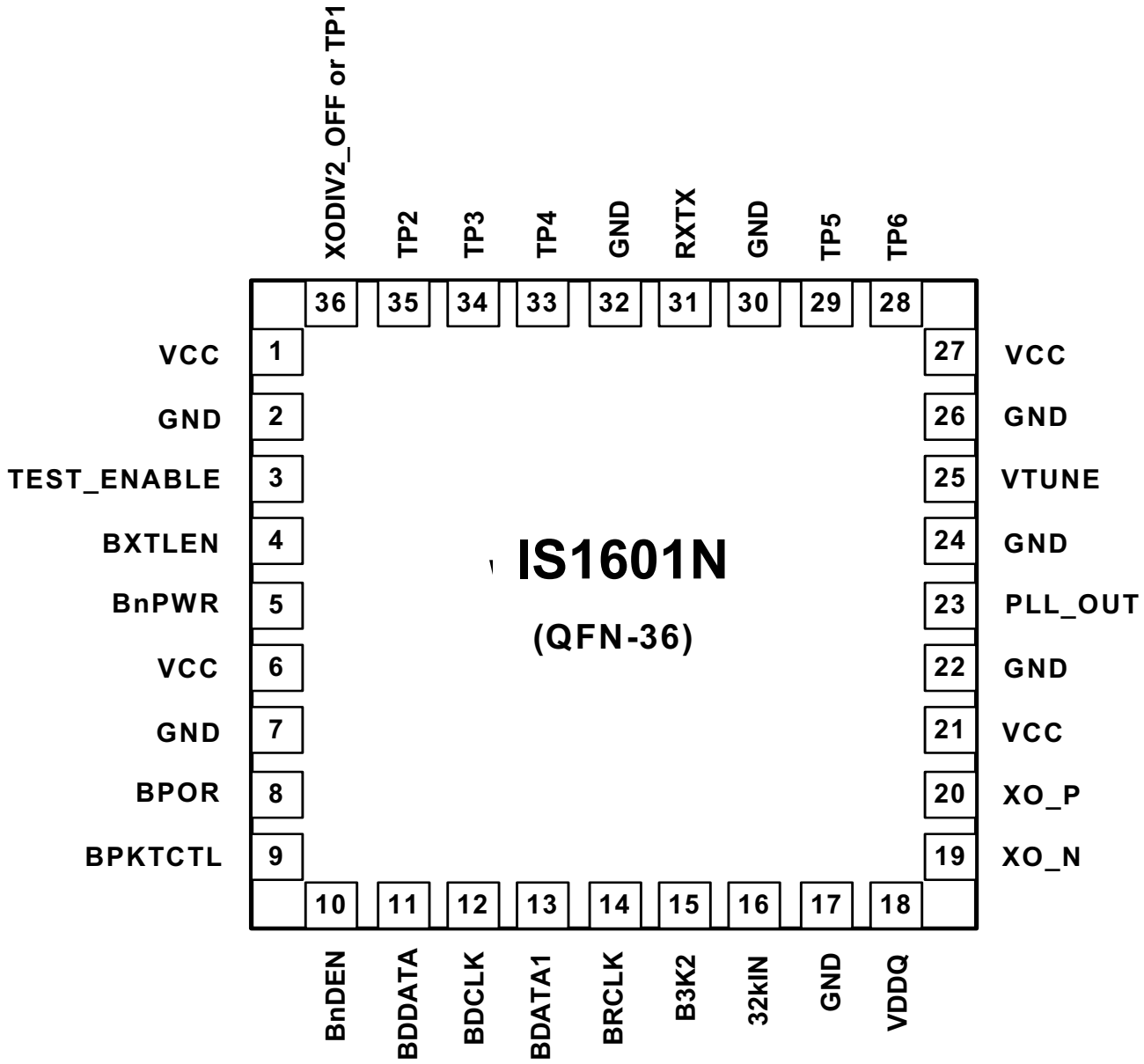


Figure 4-1. Pin-out of the IS1601 in a QFN-36 package.

4.3 Application Circuit

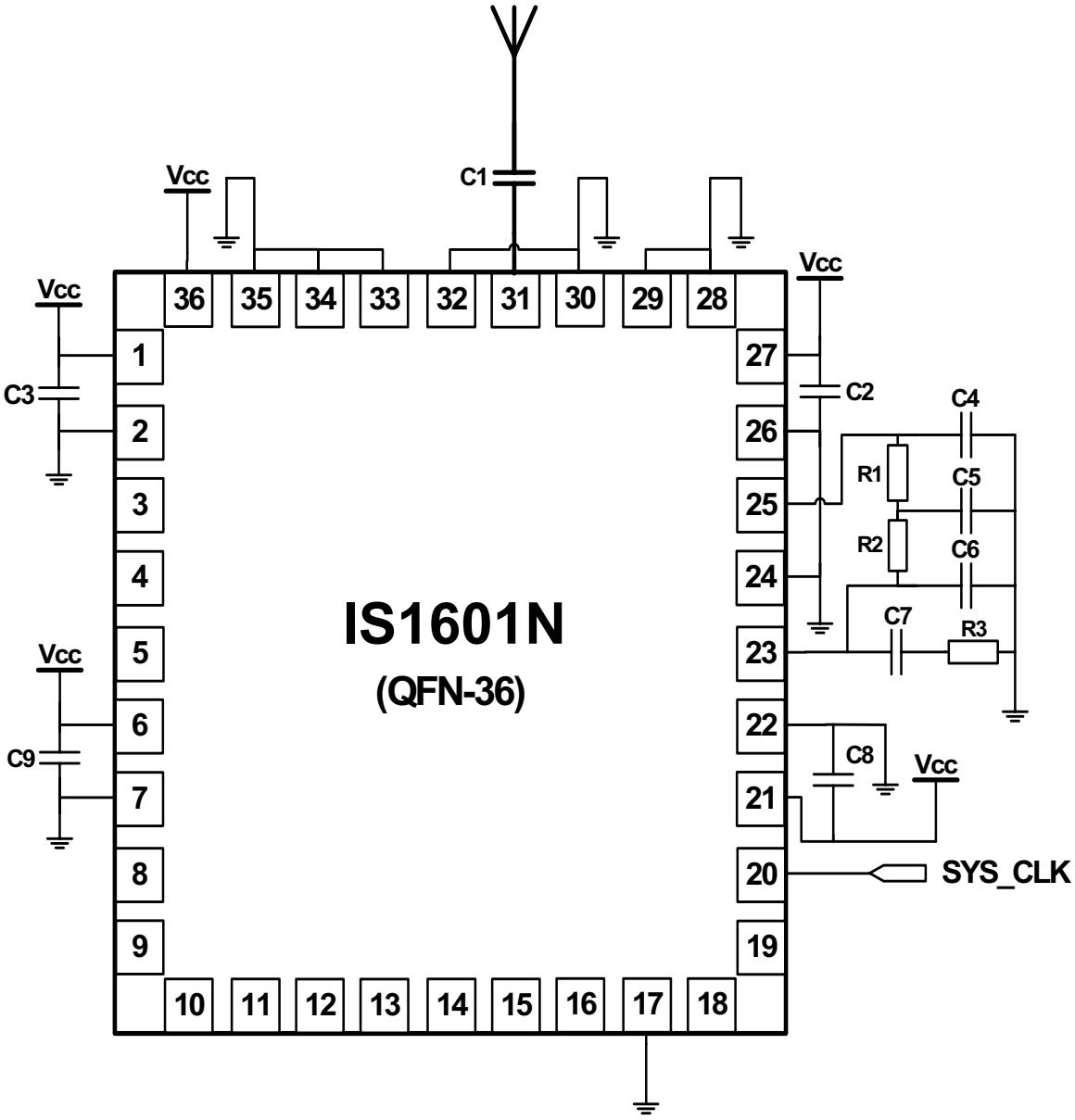
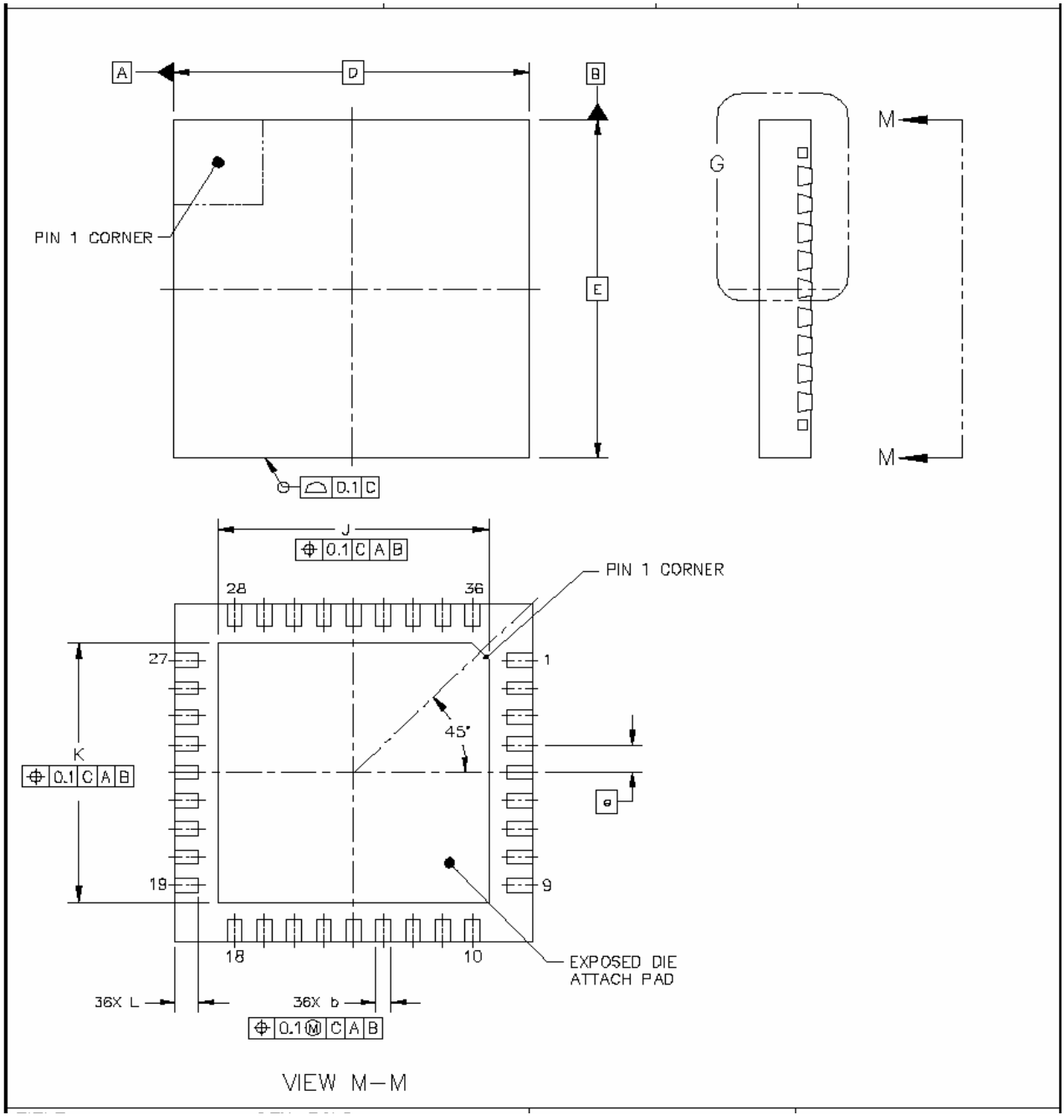


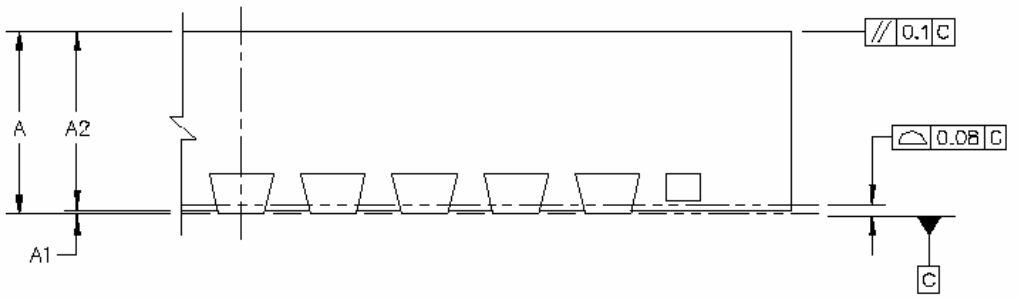
Figure 4-2. Sample application diagram illustrating the IS1601 in a QFN-36 package, using a system clock reference in the range 10-20 MHz.

Table 4-2. Component Bill Of Material

Description	Reference	Value	Tolerance	Size
Ceramic Capacitor	C1, C2, C3, C8, C9	4.7pF	NP0	0402 or 0201
Ceramic Capacitor	C4	27pF	NP0	0402 or 0201
Ceramic Capacitor	C5	39pF	NP0	0402 or 0201
Ceramic Capacitor	C6	270pF	NP0	0402 or 0201
Ceramic Capacitor	C7	4.7nF	NP0	0402 or 0201
Resistor	R1	27kΩ	±10%	0402 or 0201
Resistor	R2	10kΩ	±10%	0402 or 0201
Resistor	R3	3.3kΩ	±10%	0402 or 0201

4.4 Outline


A
D
B
PIN 1 CORNER
E
0.1 C
G
M
M
J
0.1 C A B
28
36
PIN 1 CORNER
27
1
45°
K
0.1 C A B
e
19
9
18
10
EXPOSED DIE
ATTACH PAD
36X L
36X b
0.1 M C A B
VIEW M–M



DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX
A	0.8		1
A1	0		0.05
A2	0.75		1
b	0.2	0.25	0.3
D		6 BSC	
E		6 BSC	
e		0.5 BSC	
J	4.47	4.57	4.67
K	4.47	4.57	4.67
L	0.35	0.4	0.45

NOTES

1.0 COPLANRITY APPLIES TD LEADS, CORNER LEADS AND DIE ATTACH PAD.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	JED MO-220-A (ASECL)

FAQ

PLEASE CONTACT YOUR AGENT DIRECTLY FOR ANY SERVICE.

THANK YOU VERY MUCH !

AGENT SEAL:

SALES INFORMATION

ISSC Head Office:
3F, No.2-1, Industry East Rd., I,
Science-Based Industrial Park,
Hsinchu Taiwan, R.O.C.300
TEL: 886-3-577-8385
FAX: 886-3-577-8501

ISSC TPE Office
4F, No.116, Joutz St., Neihu,
Taipei Taiwan, R.O.C. 114
TEL: 886-2-2659-7699
FAX: 886-2-2659-7967

ISSC Shanghai Office:
2F., Building 59, No. 461, Hongcao Rd., Xu Hui District, Shanghai 200233, P.R. China
TEL: 86-21-6485-6299 # 6701
FAX: 86-21-5427-6519

ALinks Communications Inc.
1095 E.,Duane AVE, Ste#102
Sunnyvale, CA 94085
TEL: 1-408-573-7676
FAX: 1-408-573-7717

ISSC.COM.TW **Sales@issc.com.tw**