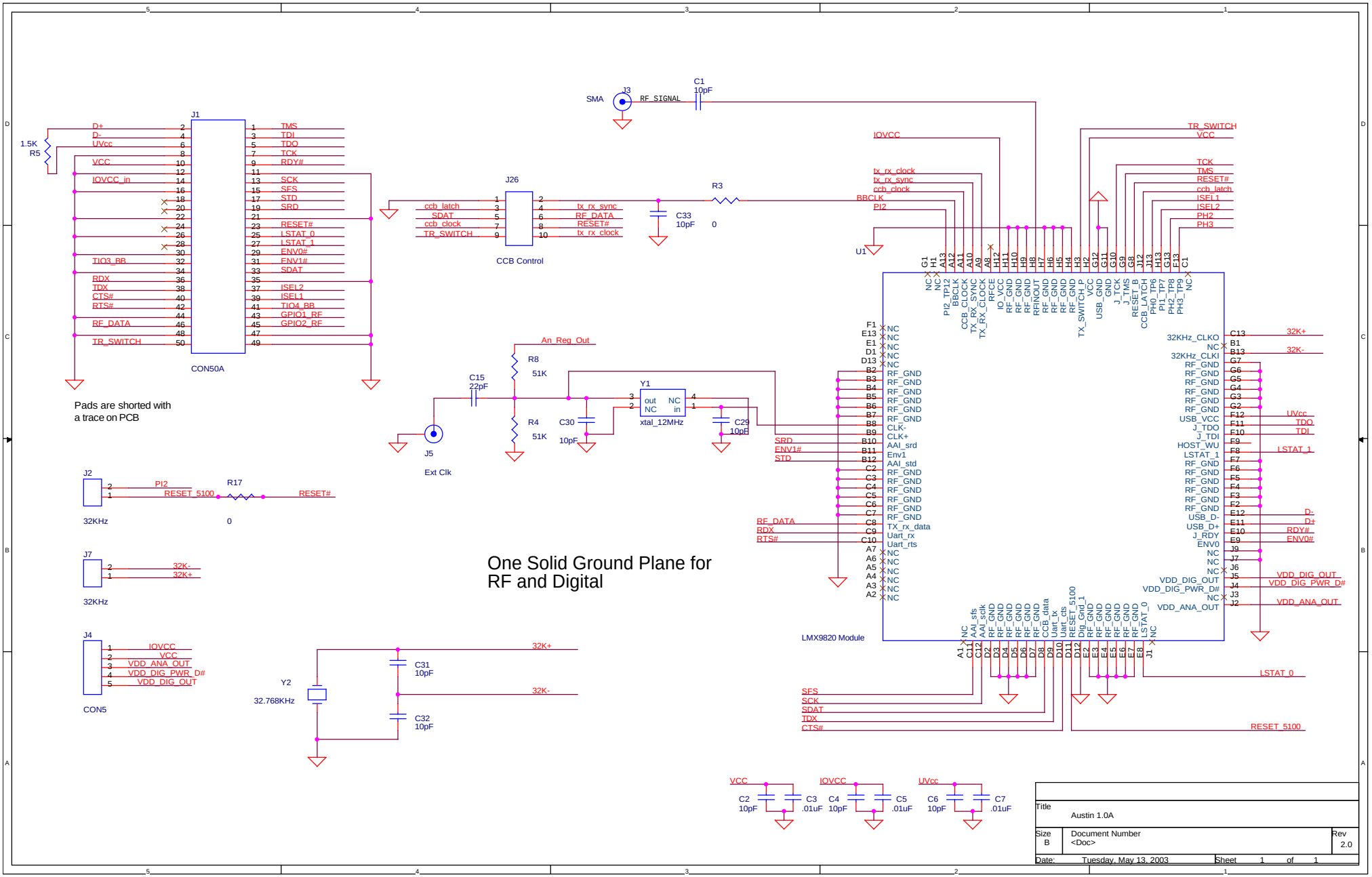
J1
CON50A
1.5K
R5
D+
D-
UVcc
VCC
IOVCC_in
TIO3_BB
RDX
TDX
CTS#
RTS#
RF_DATA
TR_SWITCH
TMS
TDI
TDO
TCK
RDY#
SCK
SES
STD
SRD
RESET#
LSTAT_0
LSTAT_1
ENV0#
ENV1#
SDAT
ISEL2
ISEL1
TIO4_BB
GPIO1_RF
GPIO2_RF
Pads are shorted with
a trace on PCB
SMA
J3
RF_SIGNAL
C1
10pF
J26
CCB Control
ccb_latch
SDAT
ccb_clock
TR_SWITCH
tx_rx_sync
RF_DATA
RESET#
tx_rx_clock
C33
10pF
R3
0
IOVCC
tx_rx_clock
tx_rx_sync
ccb_clock
BBCLK
PI2
U1
LMX9820 Module
TR_SWITCH
VCC
TCK
TMS
RESET#
ccb_latch
ISEL1
ISEL2
PH2
PH3
An_Reg_Out
R8
51K
R4
51K
C15
22pF
C30
10pF
Y1
xtal_12MHz
C29
10pF
J5
Ext Clk
SRD
ENV1#
STD
RF_DATA
RDX
RTS#
32K+
32K-
UVcc
TDO
TDI
LSTAT_1
D-
D+
RDY#
ENV0#
VDD_DIG_OUT
VDD_DIG_PWR_D#
VDD_ANA_OUT
LSTAT_0
SES
SCK
SDAT
TDX
CTS#
RESET_5100
J2
32KHz
PI2
RESET_5100
R17
0
RESET#
J7
32KHz
32K-
32K+
J4
CON5
IOVCC
VCC
VDD_ANA_OUT
VDD_DIG_PWR_D#
VDD_DIG_OUT
Y2
32.768KHz
C31
10pF
C32
10pF
32K+
32K-
One Solid Ground Plane for
RF and Digital
VCC
C2
10pF
C3
.01uF
IOVCC
C4
10pF
C5
.01uF
UVcc
C6
10pF
C7
.01uF
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Size
B
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Tuesday, May 13, 2003
Sheet
1
of
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