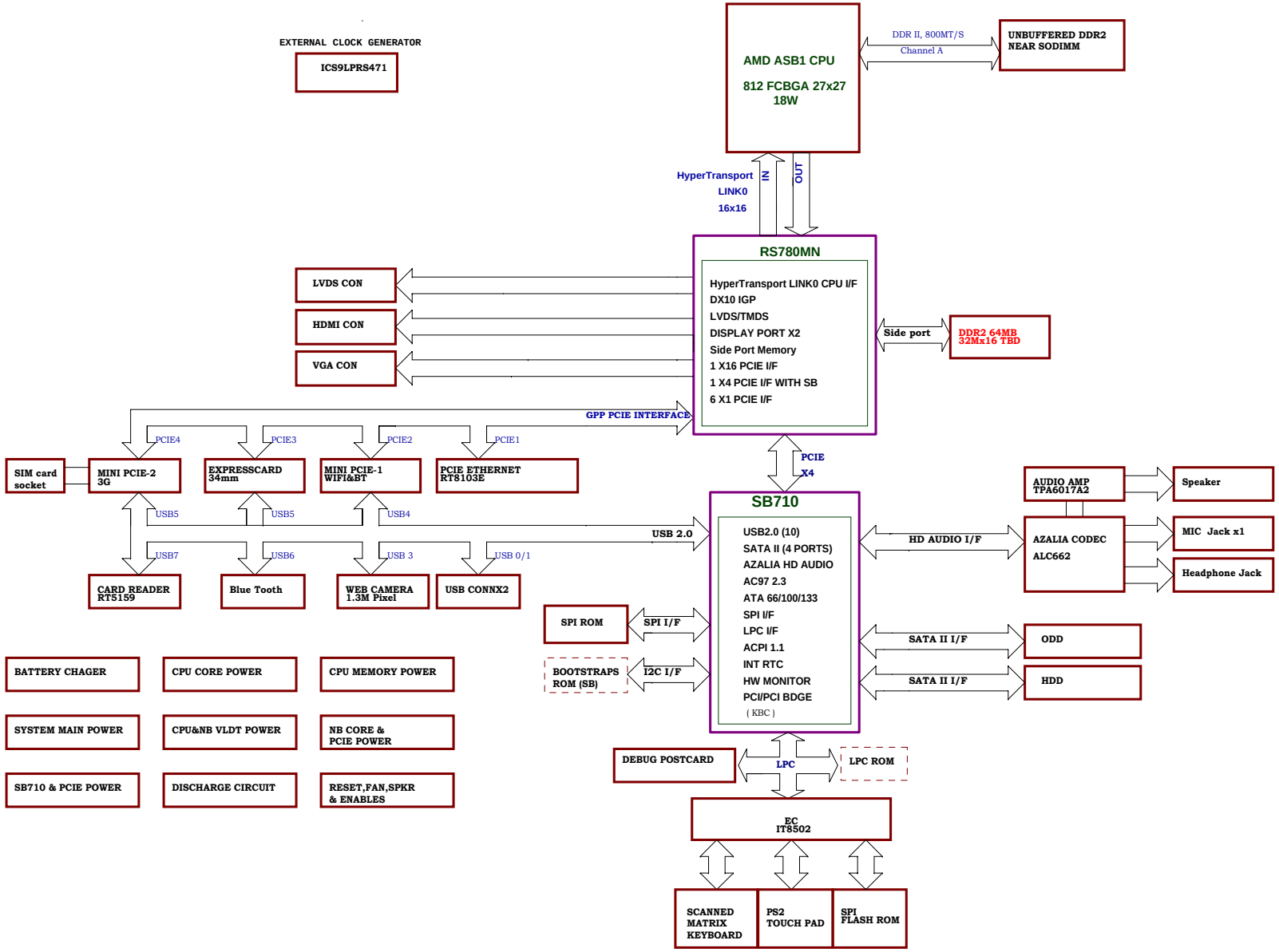
COBY NBPC1220



COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
Size C	Document Number NBPC1220	Rev 1.0
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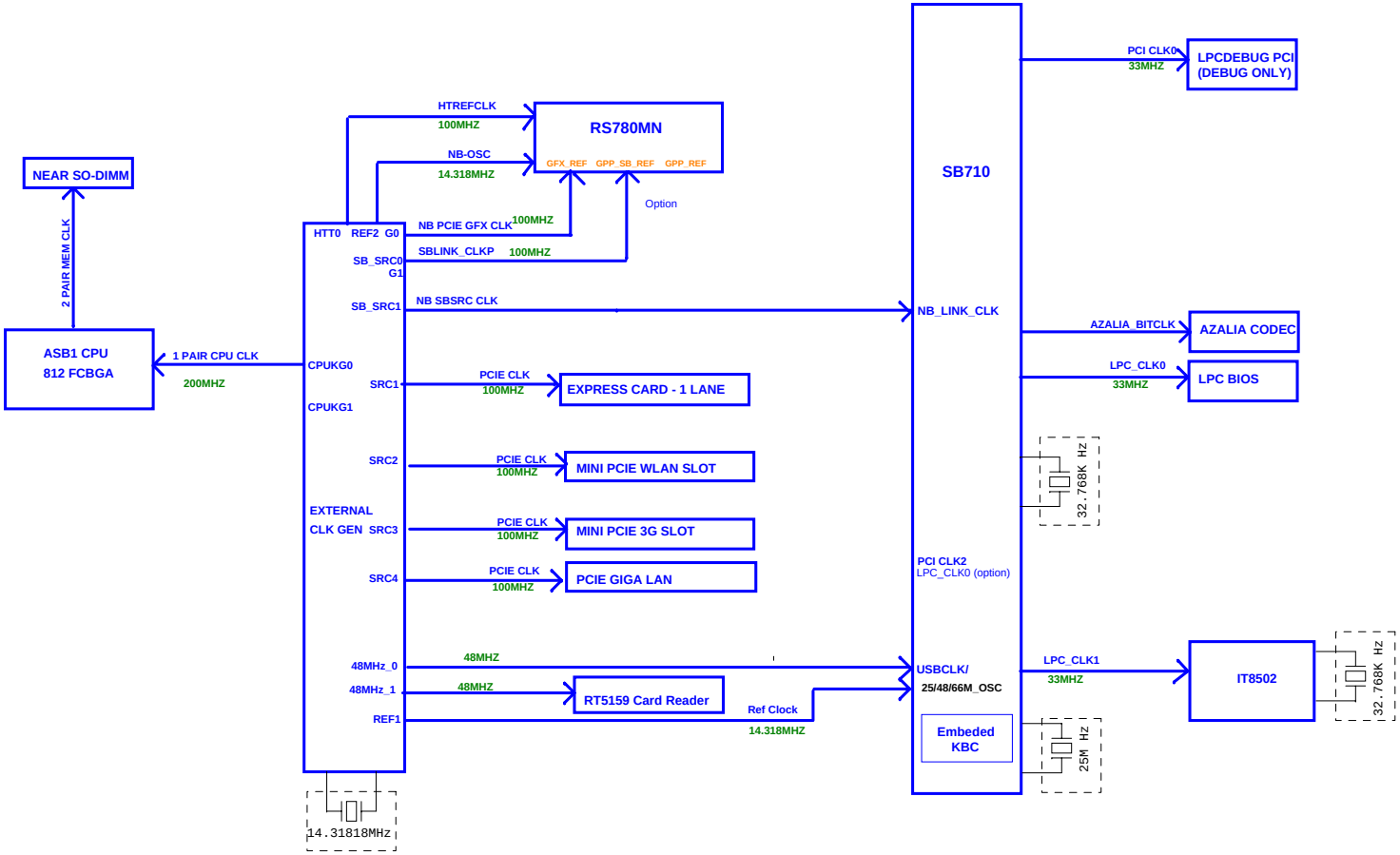

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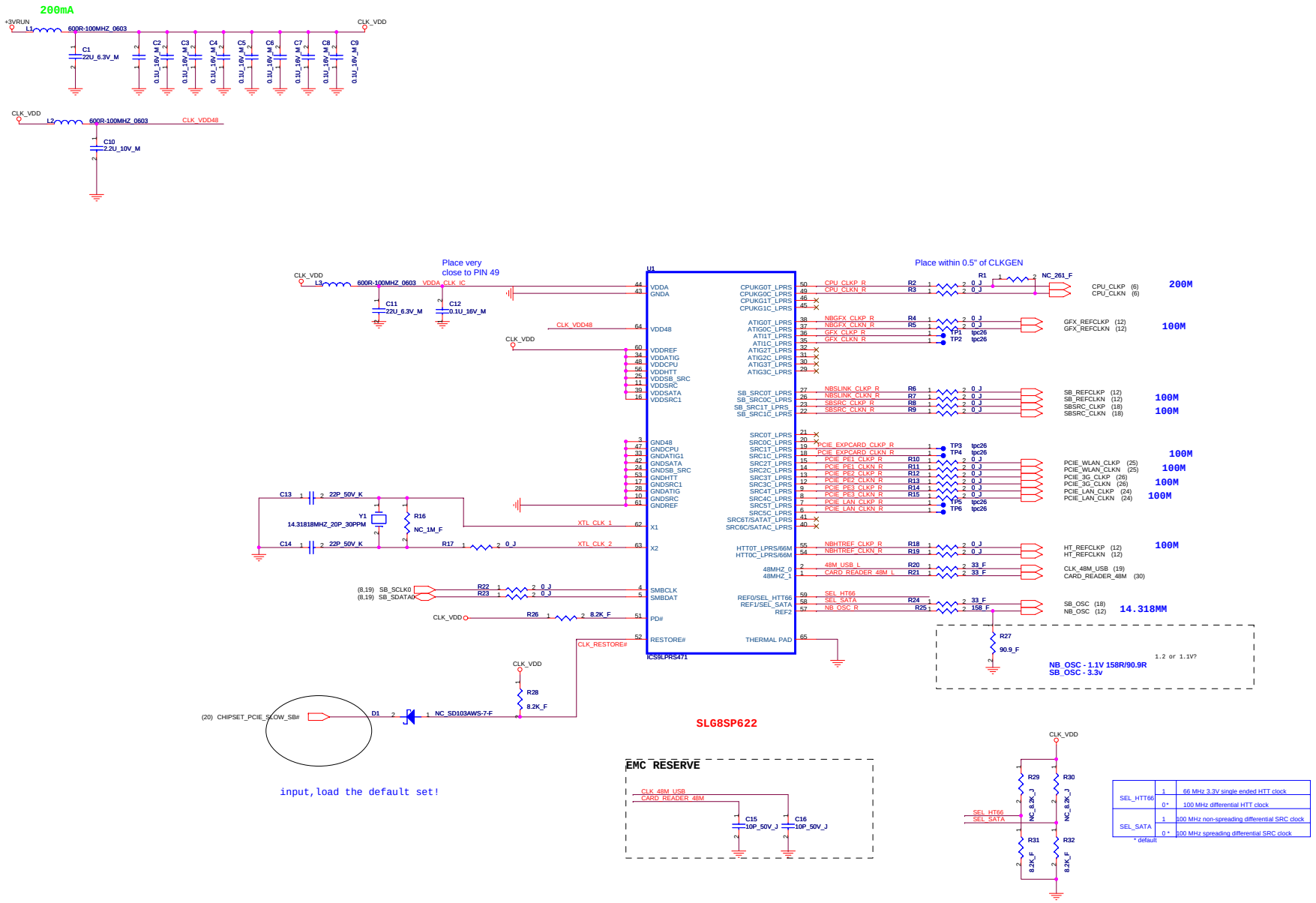

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0 *	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock

* default

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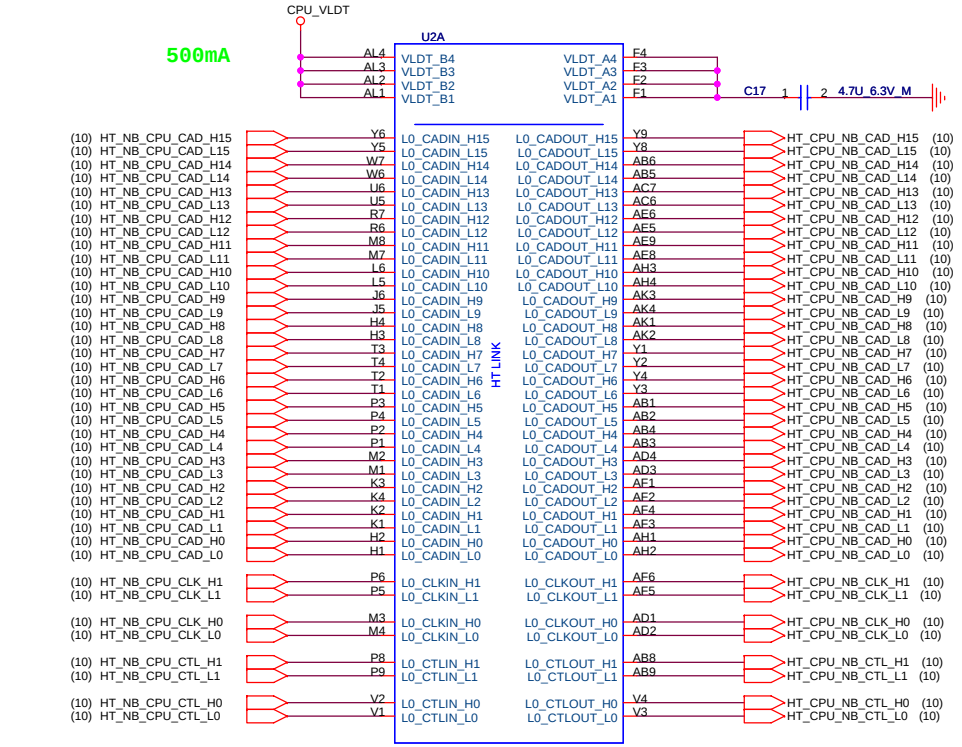
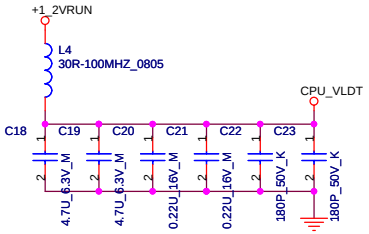


Place close to socket



DESIGN NOTE:
VLDT must be routed as a pour or a trace at least 200 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls.
Choose whichever makes routing simpler.
These six capacitors must be placed very near the selected balls.
The "other" set of balls must be decoupled with a 4.7uF cap.

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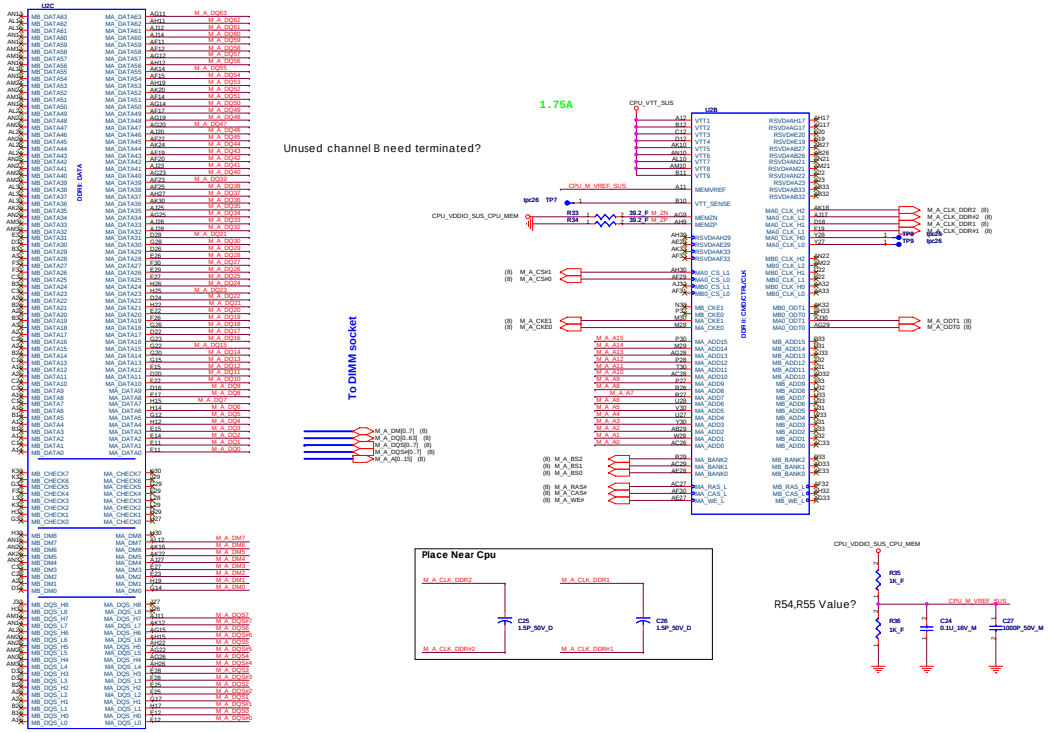

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.		
Size D	Document Number NBPC1220		Rev 1.0
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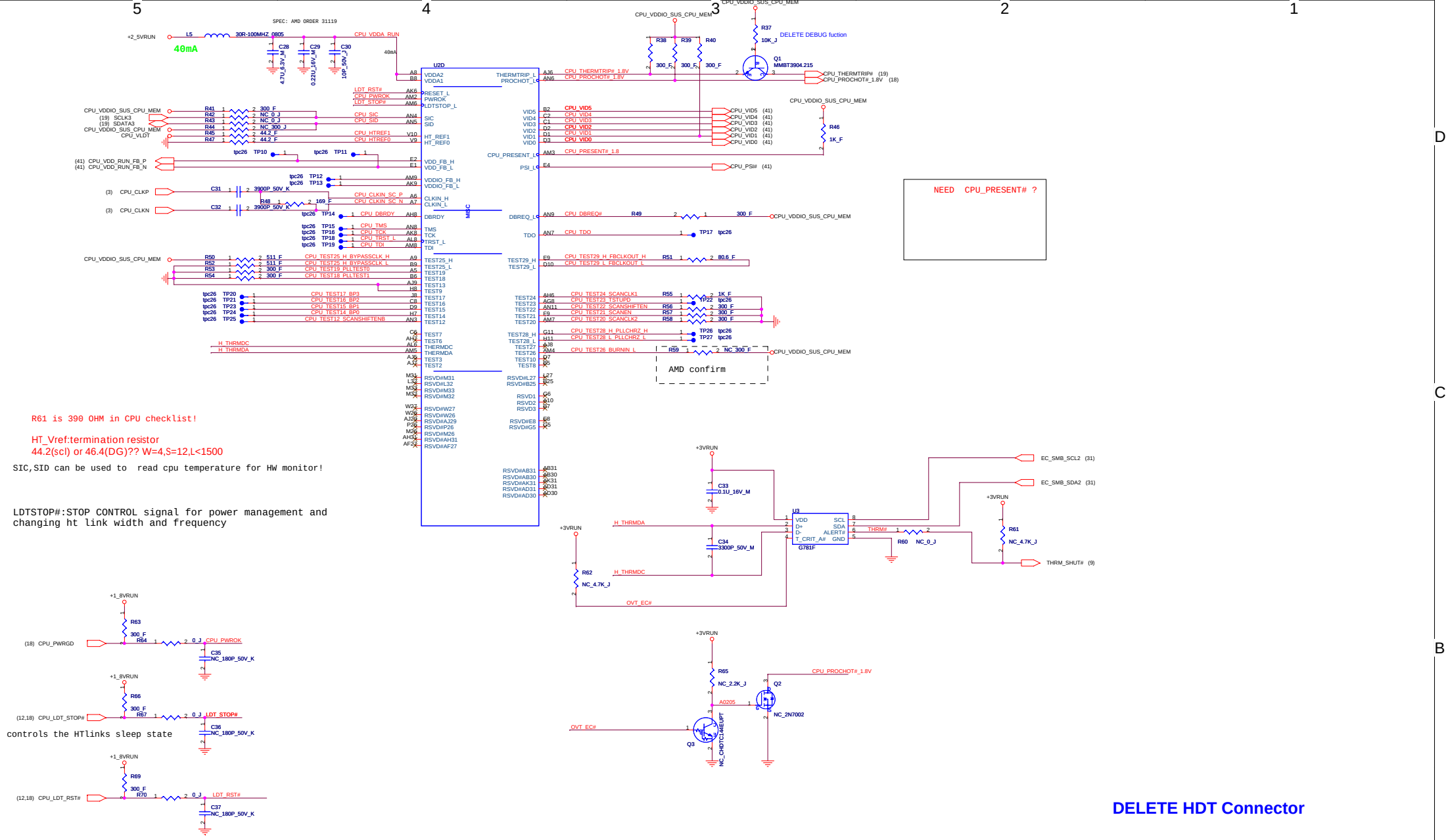

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
Size A2	Document Number NBPC1220	Rev 1.0
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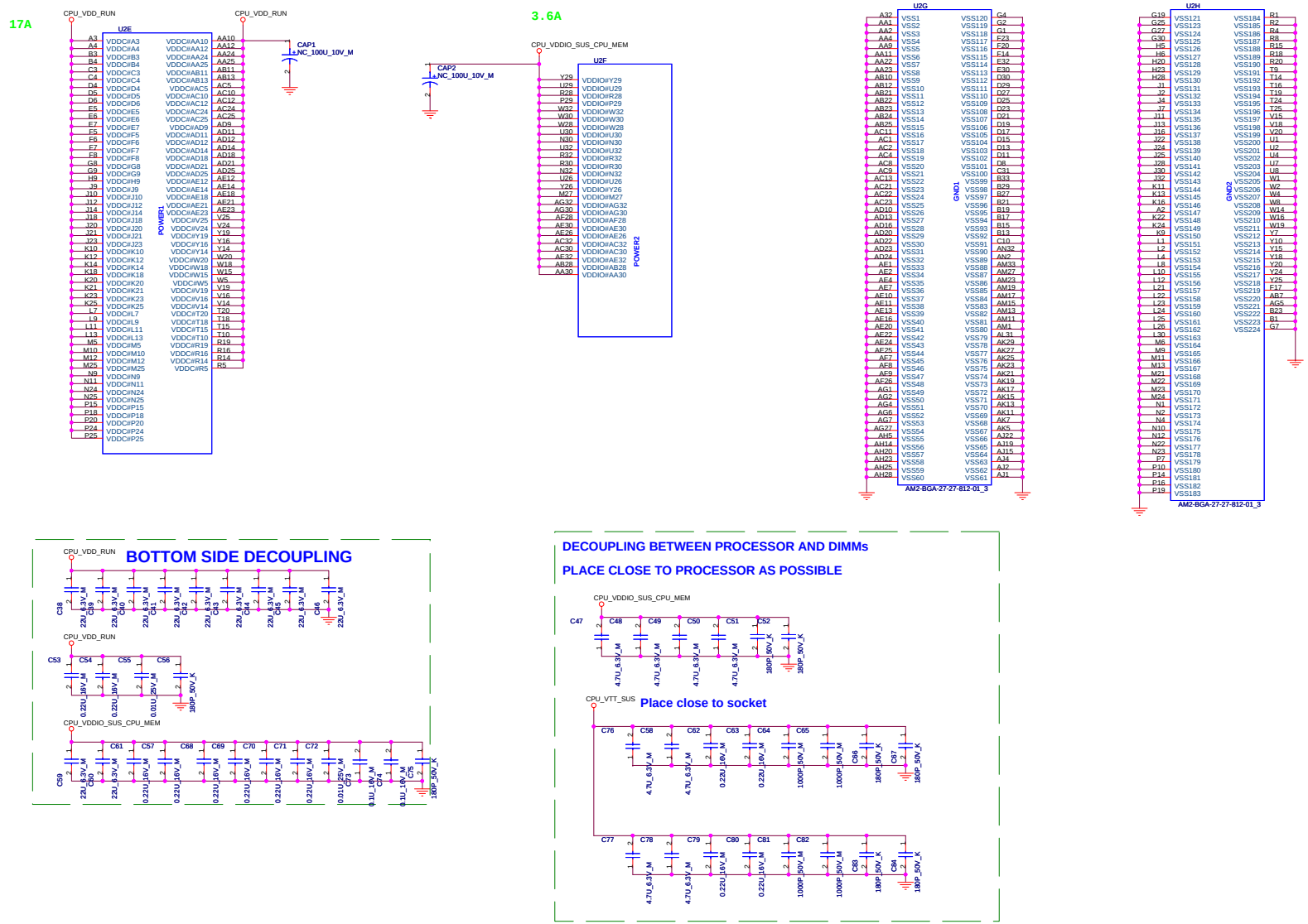

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
Size A2	Document Number NBPC1220	Rev 1.0
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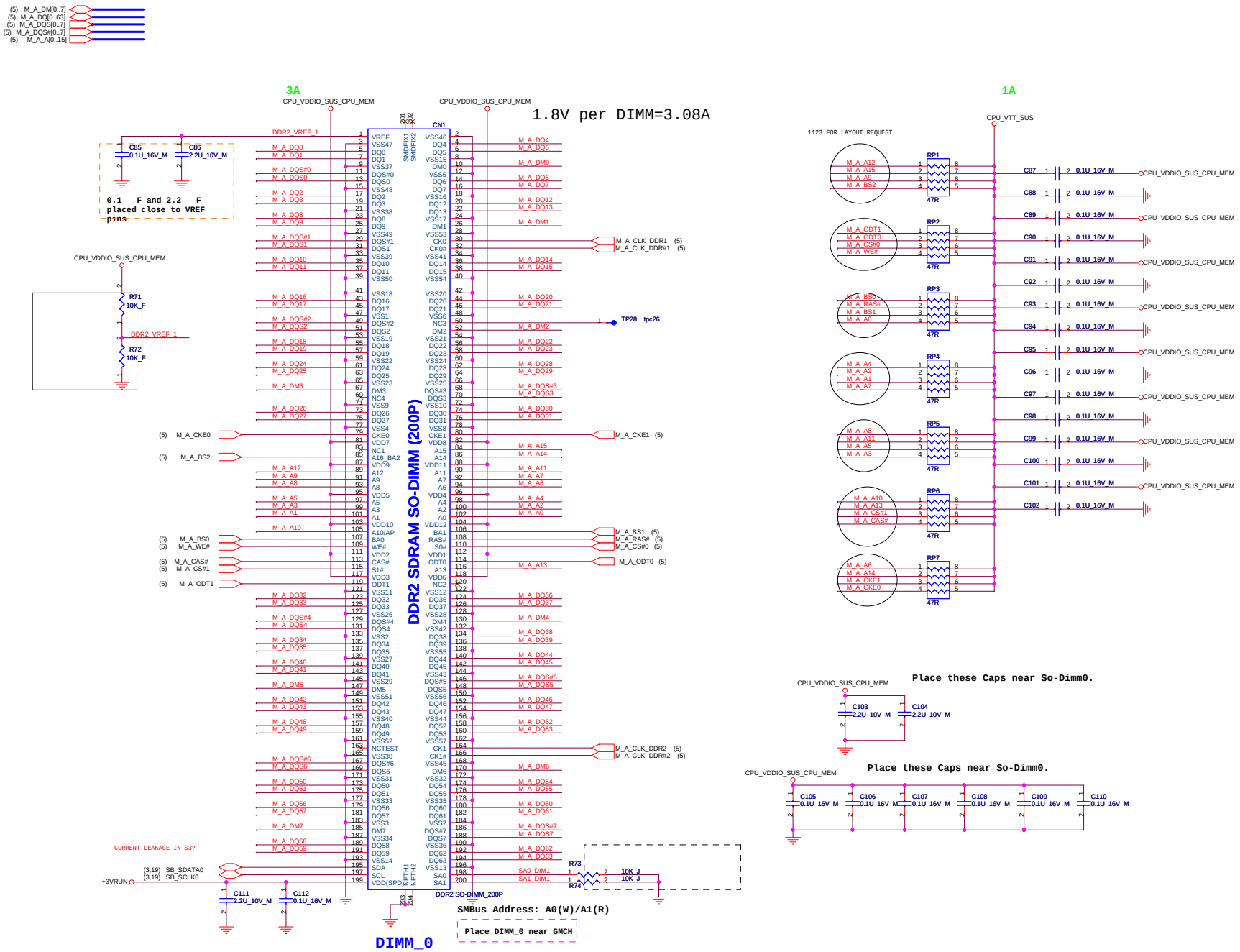

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.		
Size C	Document Number NBPC1220		Rev L0
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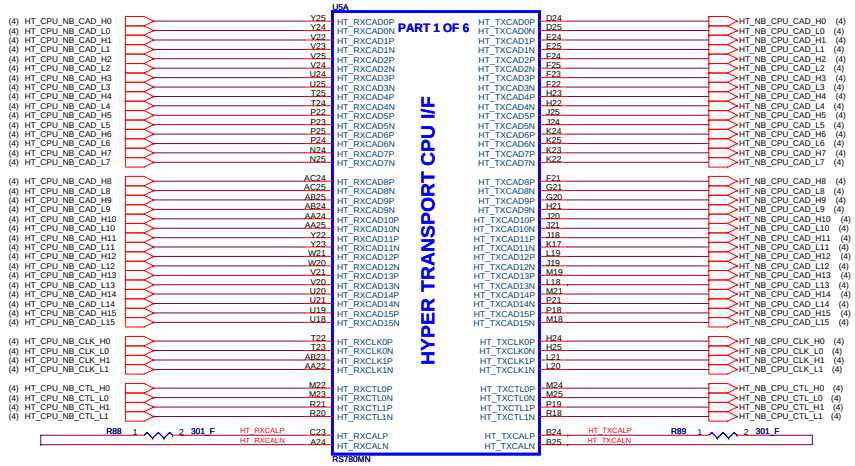

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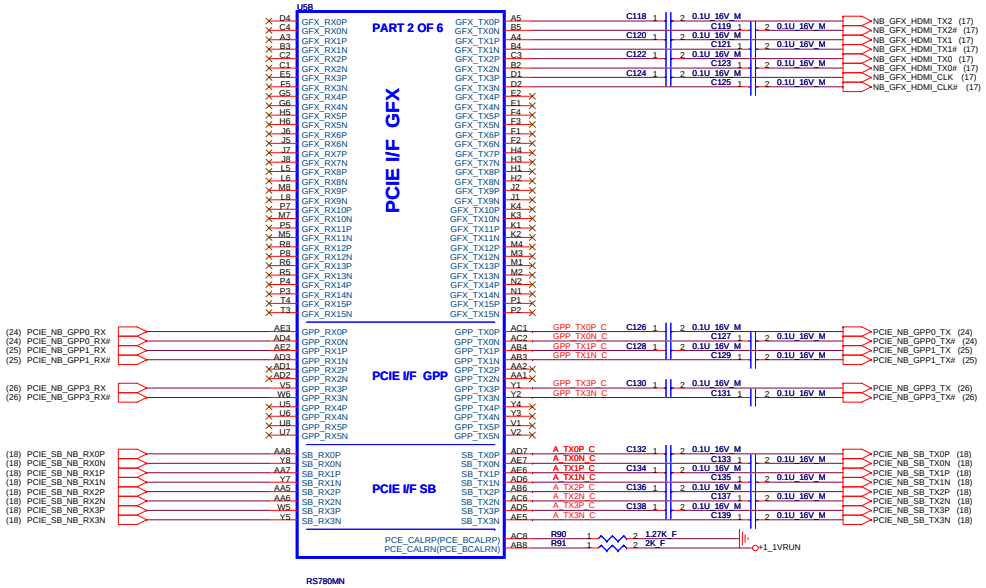

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.		
Size A2	Document Number NBPC1220		Rev 1.0
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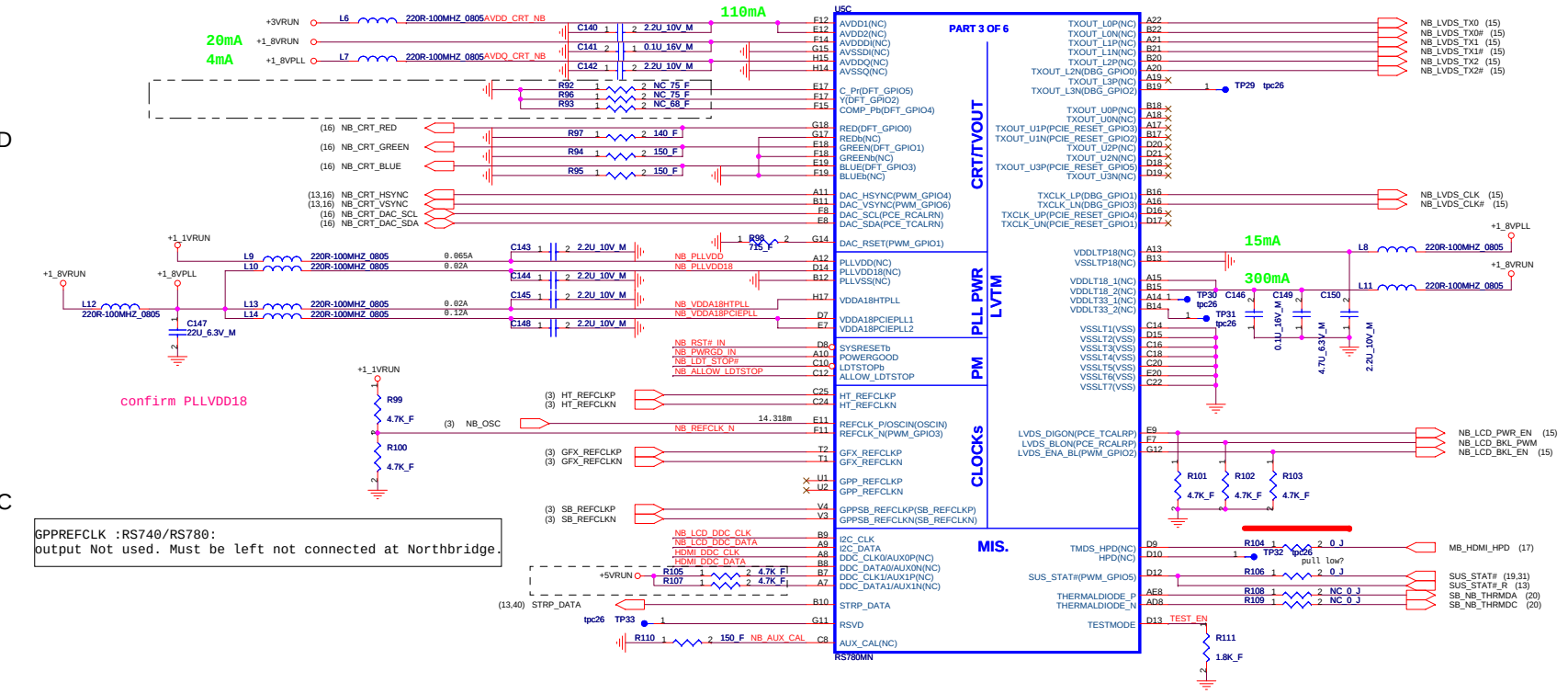
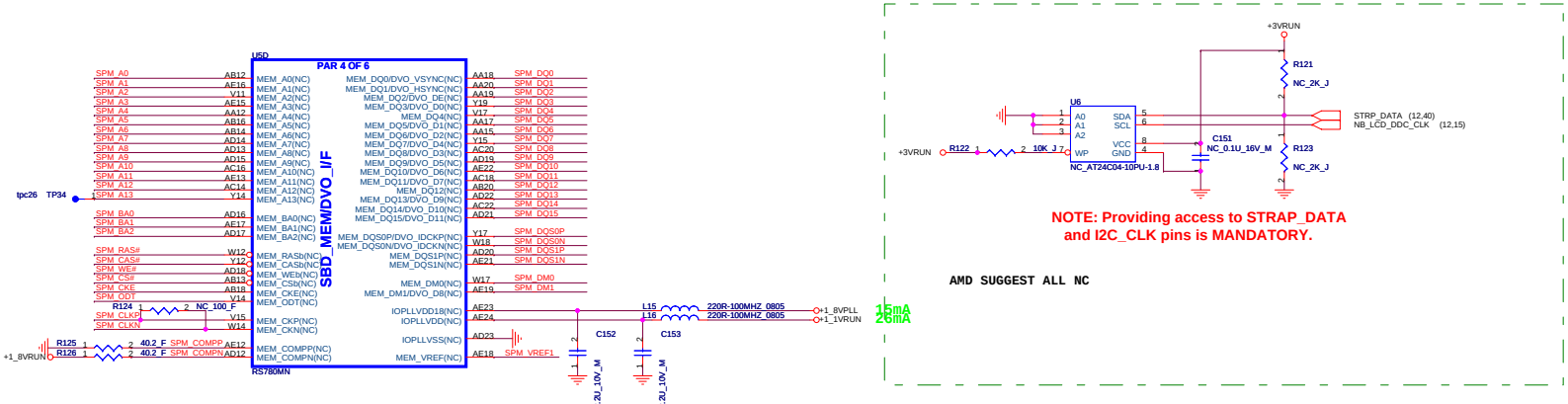
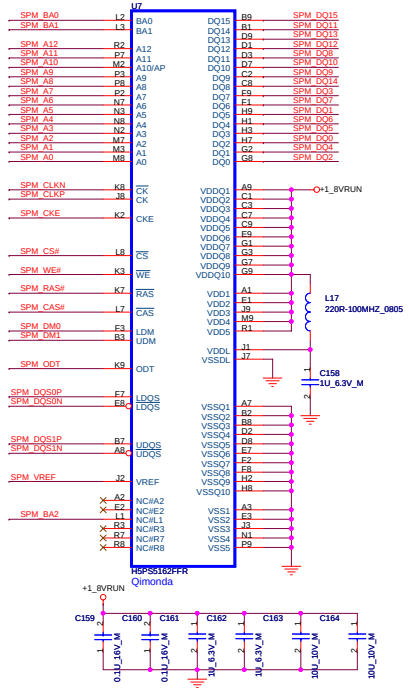
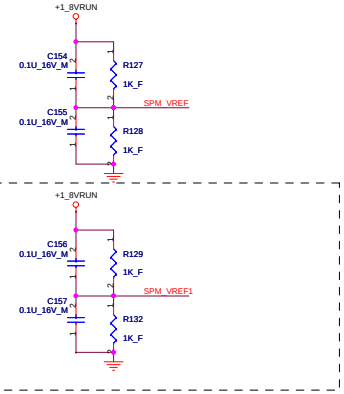


ALLOW_LDTSTOP	OC
LDT_STOP#	3.3V Input

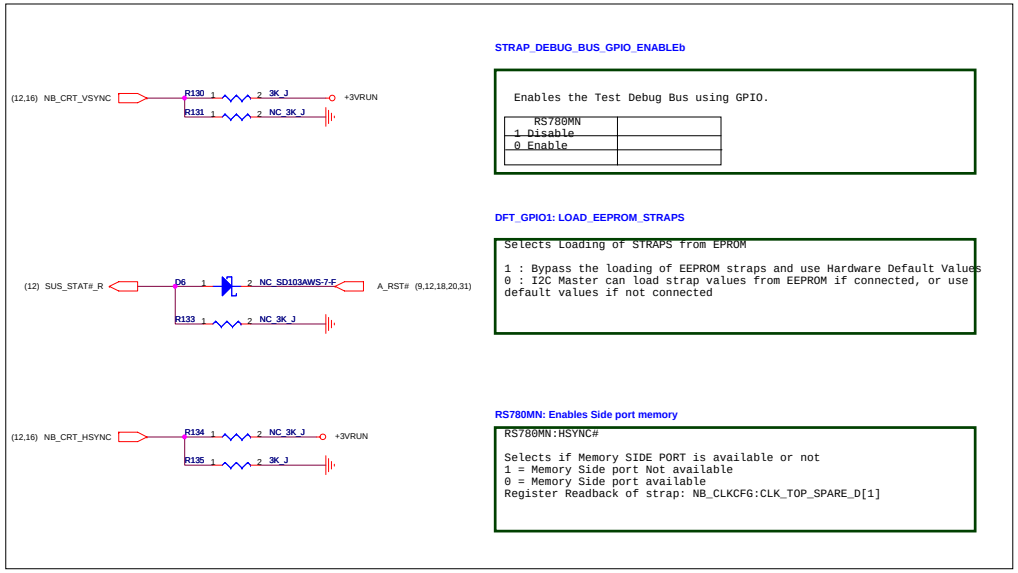
* Although defined as 3.3V I/Os, a 1.8V signaling level is supported on LDT_STOP#/ALLOW_LDTSTOP given that Vih is 1.4V.
3.3V to 1.8V level translation is not required.







MAX 400Mhz,128MB



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS780MN	
1 Disable	
0 Enable	

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS780MN: Enables Side port memory

RS780MN:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

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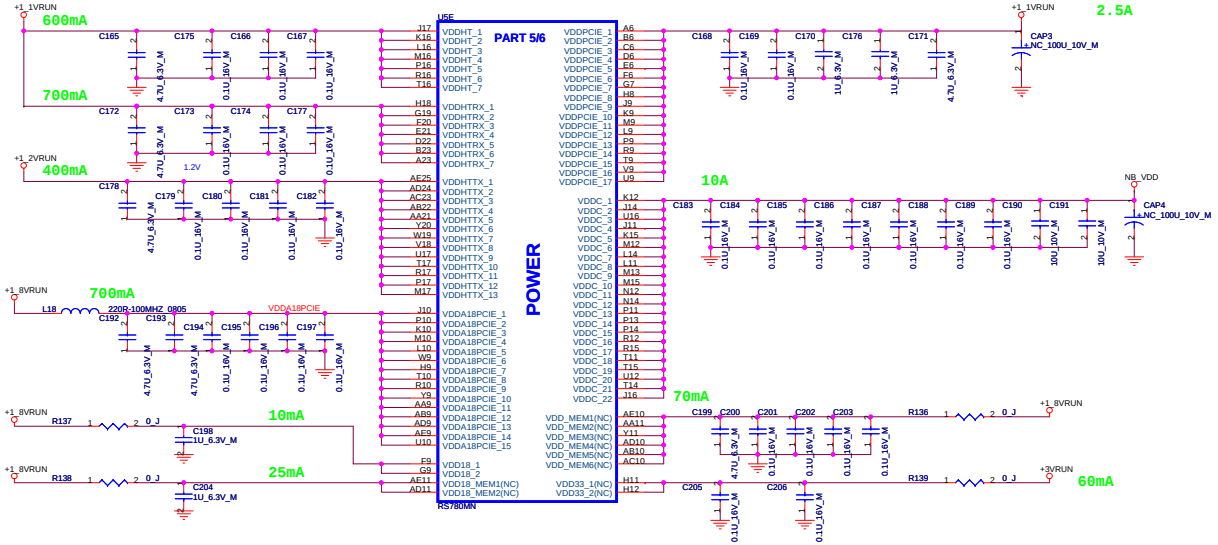

RS780MN POWER TABLE

PIN NAME	RS780MN	PIN NAME	RS780MN
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

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HSD121PHW2-A VLED:5V

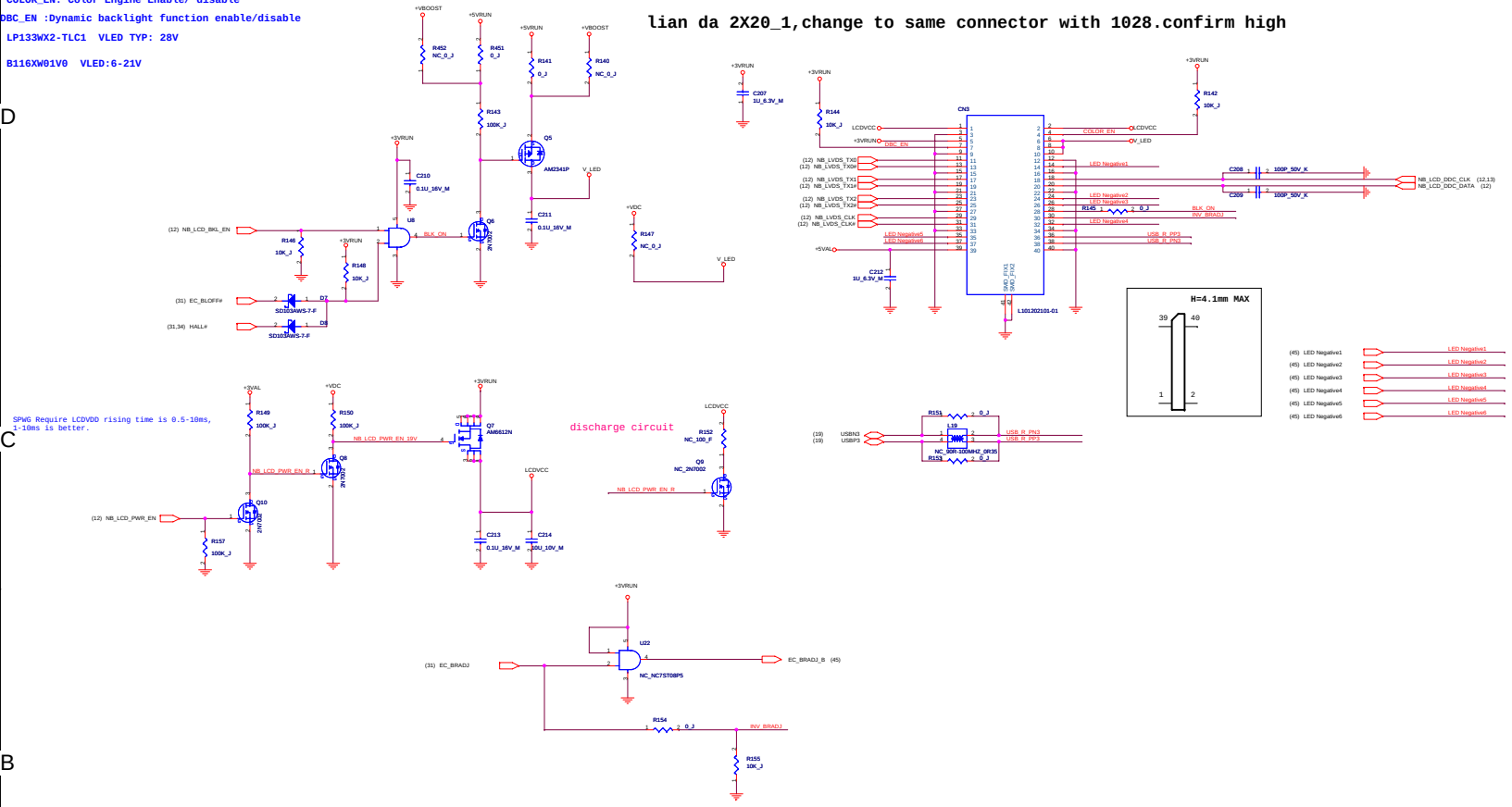
COLOR_EN: Color Engine Enable/ disable

DBC_EN :Dynamic backlight function enable/disable

LP133WX2-TLC1 VLED TYP: 28V

B116XW01V0 VLED:6-21V

lian da 2X20_1,change to same connector with 1028.confirm high



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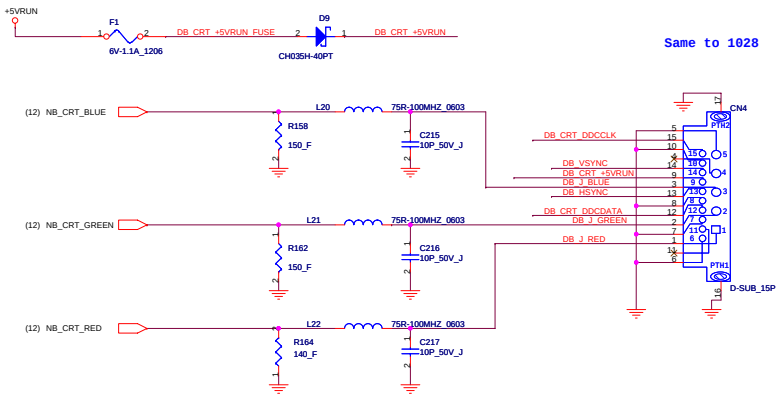

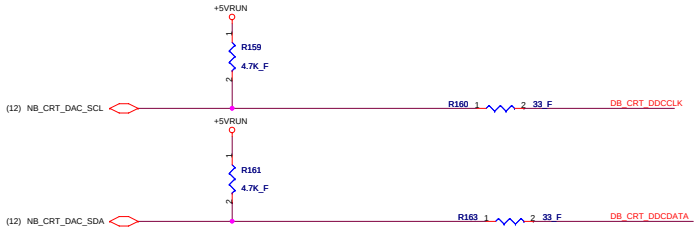

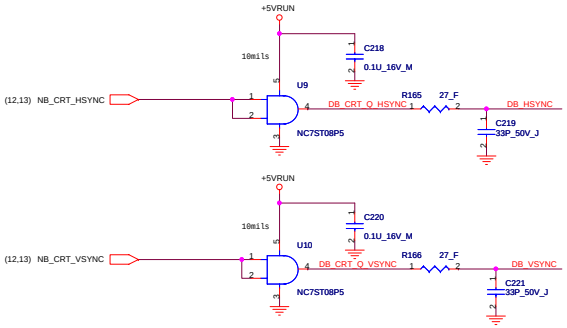

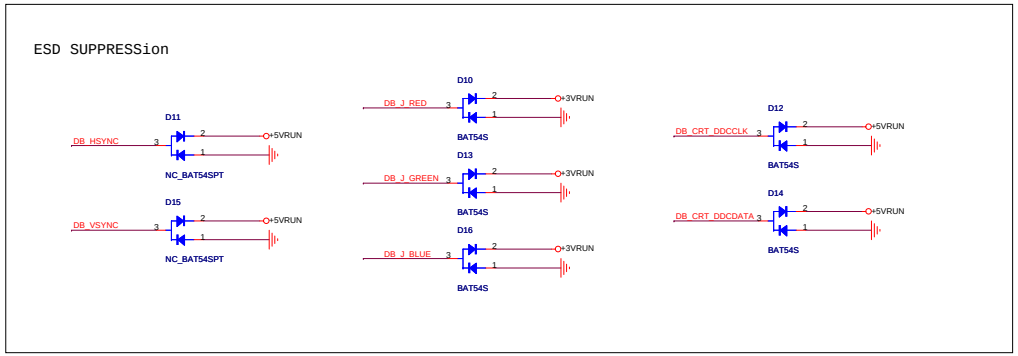

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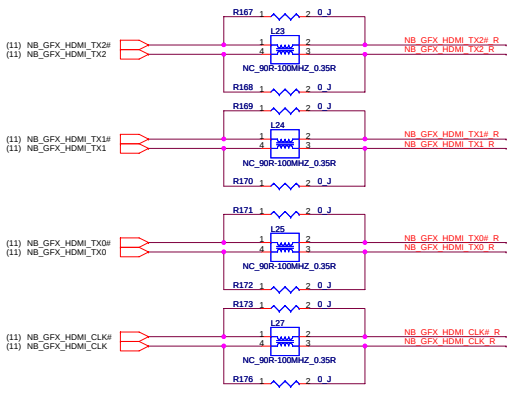
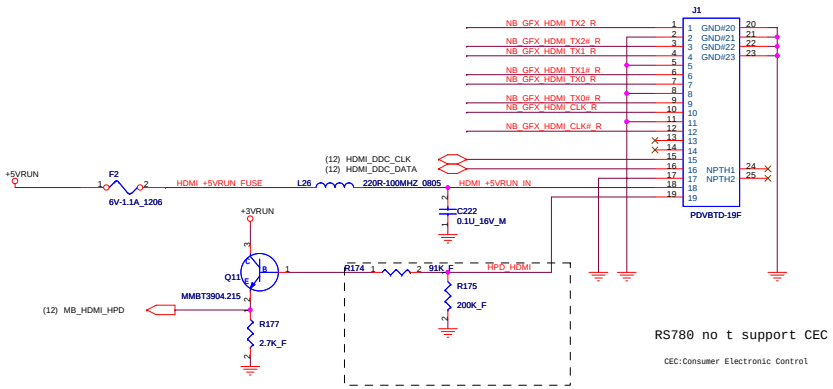


Level Shift is not required for
IGP(RS780MN) ONLY design

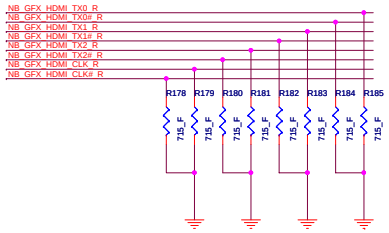
HDMI



2nd Source:LIANDA-HDMI

RS780 no t support CEC

CEC:Consumer Electronic Control



DELETE 2N7002 1016

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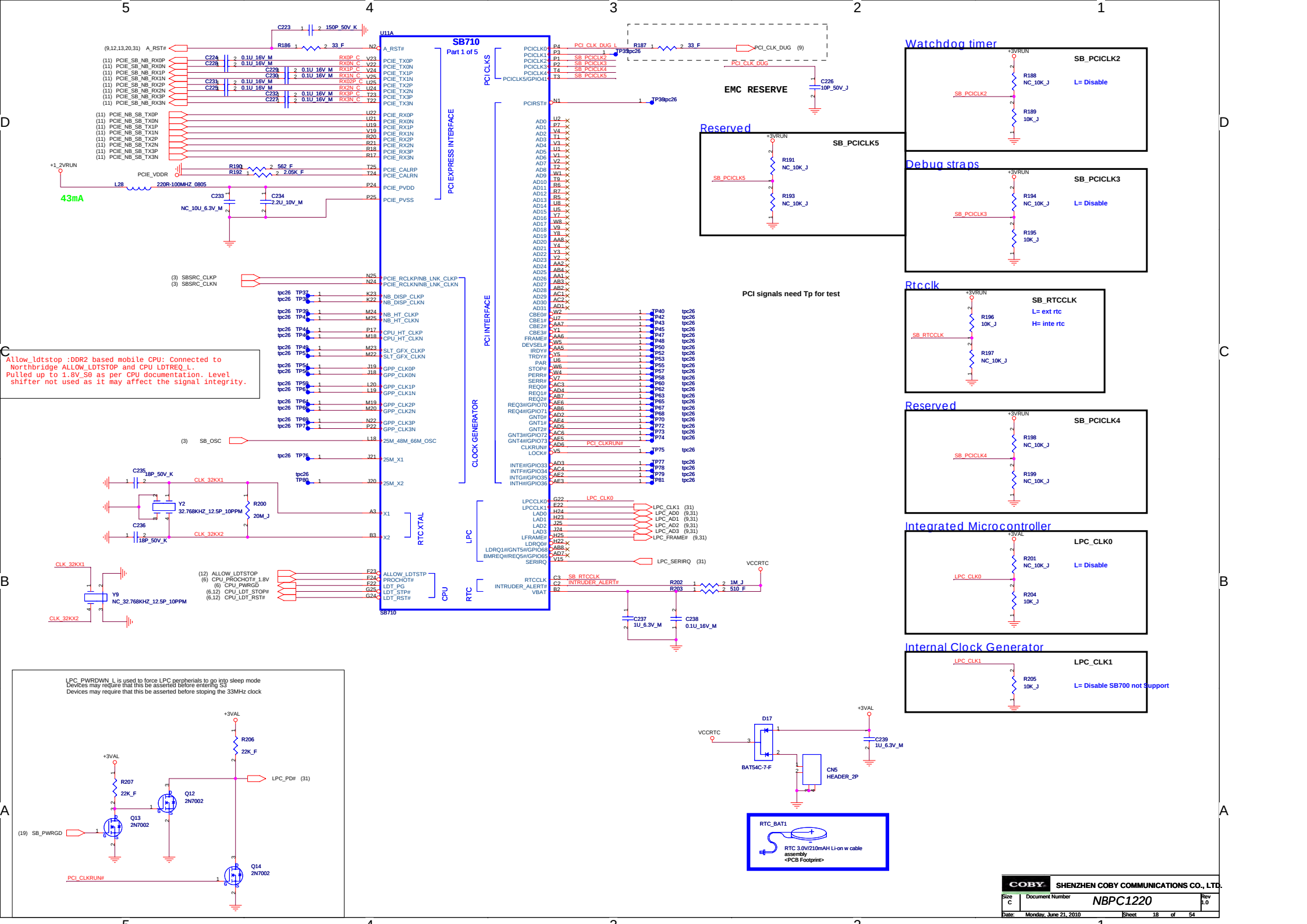
SB710
Part 1 of 5
U11A
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
PCI CLKS
LPC
RTC XTAL
CPU
RTC
EMC RESERVE
Watchdog timer
SB_PCICLK2
L= Disable
Reserved
SB_PCICLK5
Debug straps
SB_PCICLK3
L= Disable
Rtcclk
SB_RTCCLK
L= ext rtc
H= inte rtc
Reserved
SB_PCICLK4
Integrated Microcontroller
LPC_CLK0
L= Disable
Internal Clock Generator
LPC_CLK1
L= Disable SB700 not Support
PCI signals need Tp for test
Allow_ldtstop :DDR2 based mobile CPU: Connected to Northbridge ALLOW_LDTSTOP and CPU LDTREQ_L. Pulled up to 1.8V_S0 as per CPU documentation. Level shifter not used as it may affect the signal integrity.
43mA
LPC_PWRDWN_L is used to force LPC perpherials to go into sleep mode
Devices may require that this be asserted before entering S3
Devices may require that this be asserted before stoping the 33MHz clock
RTC_BAT1
RTC 3.0V/210mAH Li-on w cable assembly
<PCB Footprint>
COBY
SHENZHEN COBY COMMUNICATIONS CO., LTD.
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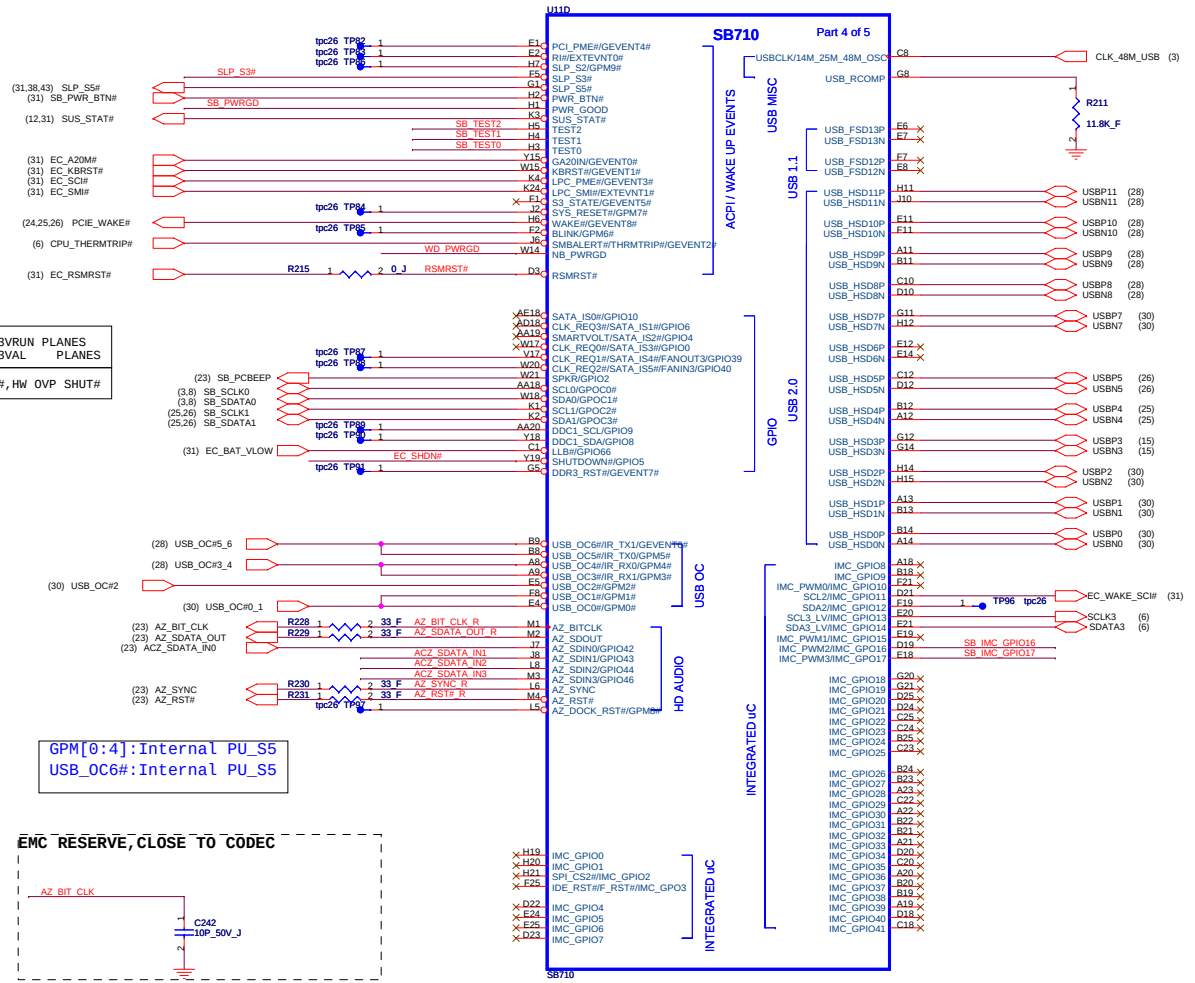


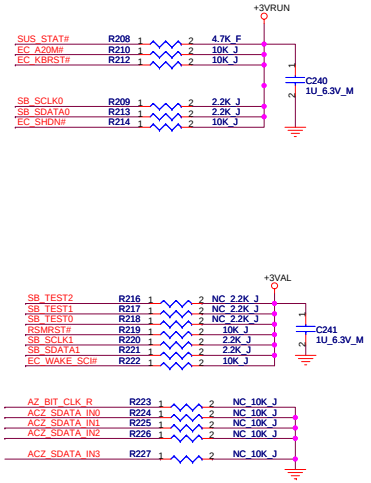
SM0---+3VRUN PLANES SM1---+3VAL PLANES
EC_SHDN#,HW OVP SHUT#

GPM[0:4]:Internal PU_S5
USB_OC6#:Internal PU_S5

EMC RESERVE,CLOSE TO CODEC

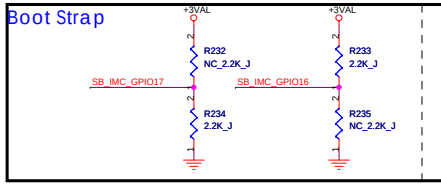
USB port table

Port0	D/B USB0
Port1	D/B USB1
Port2	M/B USB2
Port3	Camera module
Port4	WIFI&BT CARD
Port5	3G card
Port6	
Port7	CARD READER



ATE TEST

Boot Strap



IMC:GP17 GP16

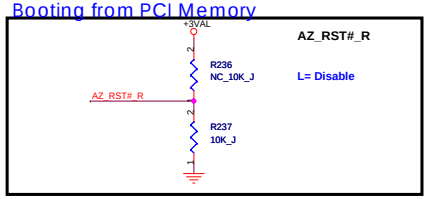
H,H = Reserved

H,L = SPI ROM

L,H = LPC ROM (Default)

L,L = FWH ROM

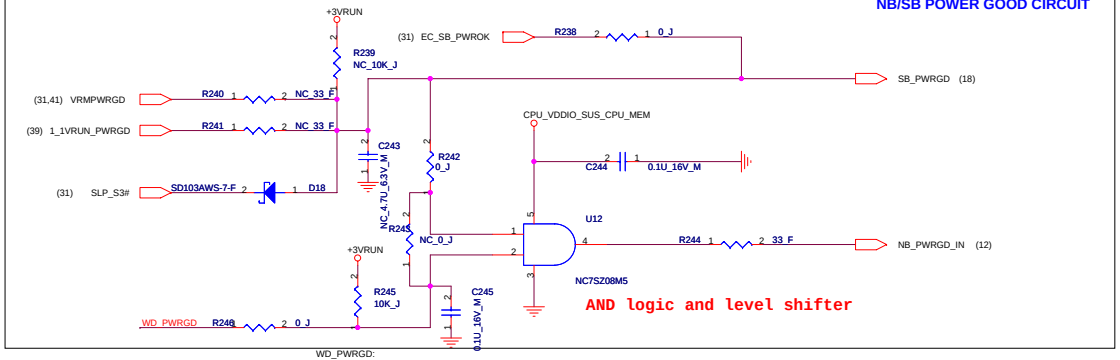
Booting from PCI Memory



AZ_RST#_R

L= Disable

NB/SB POWER GOOD CIRCUIT



AND logic and level shifter

WD_PWRGD:
Not glitch free, add gating on LVDS_BLON, BLEN and DIGON if WD_PWRGD is used

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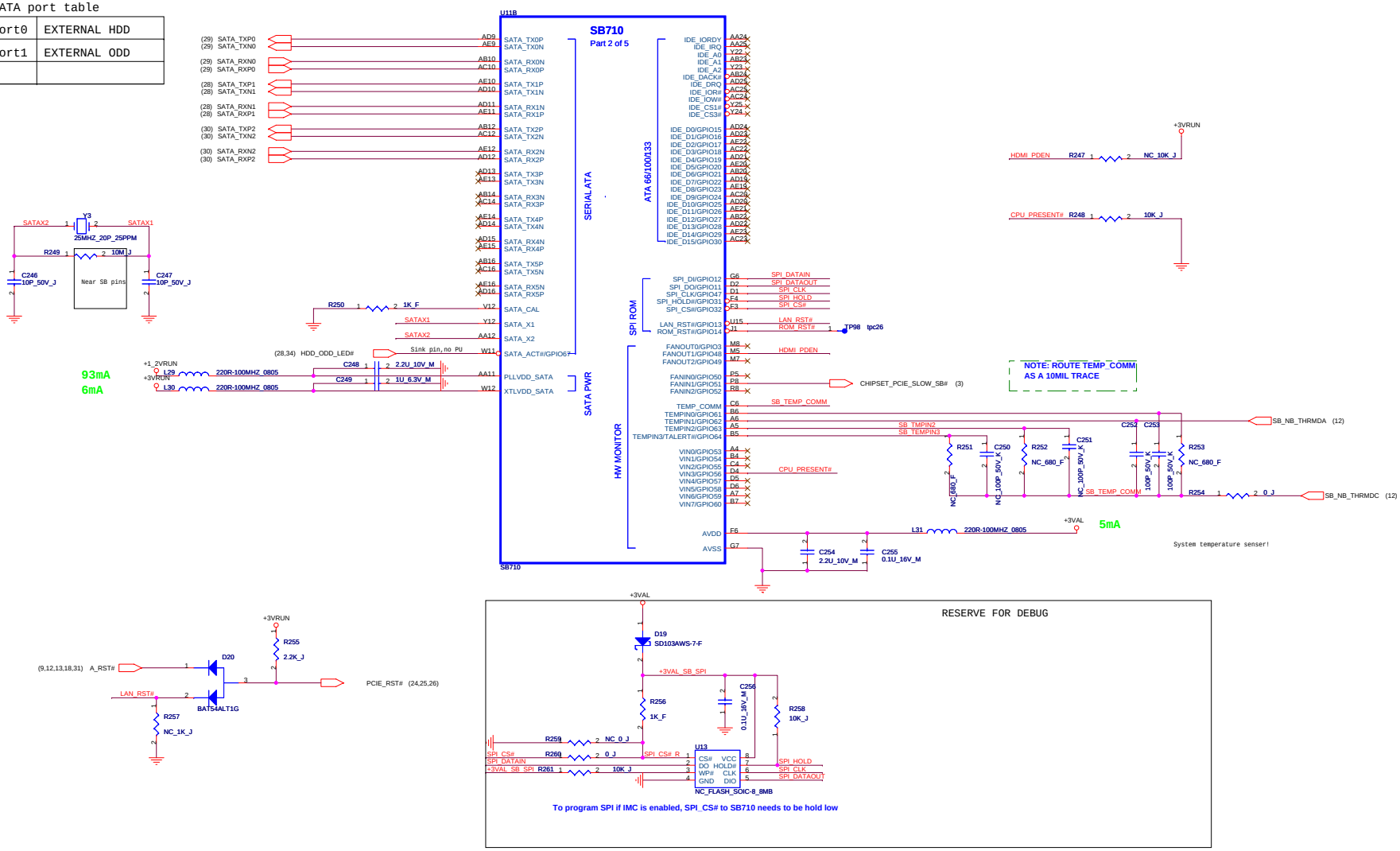
SATA port table

Port0	EXTERNAL HDD
Port1	EXTERNAL ODD



COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
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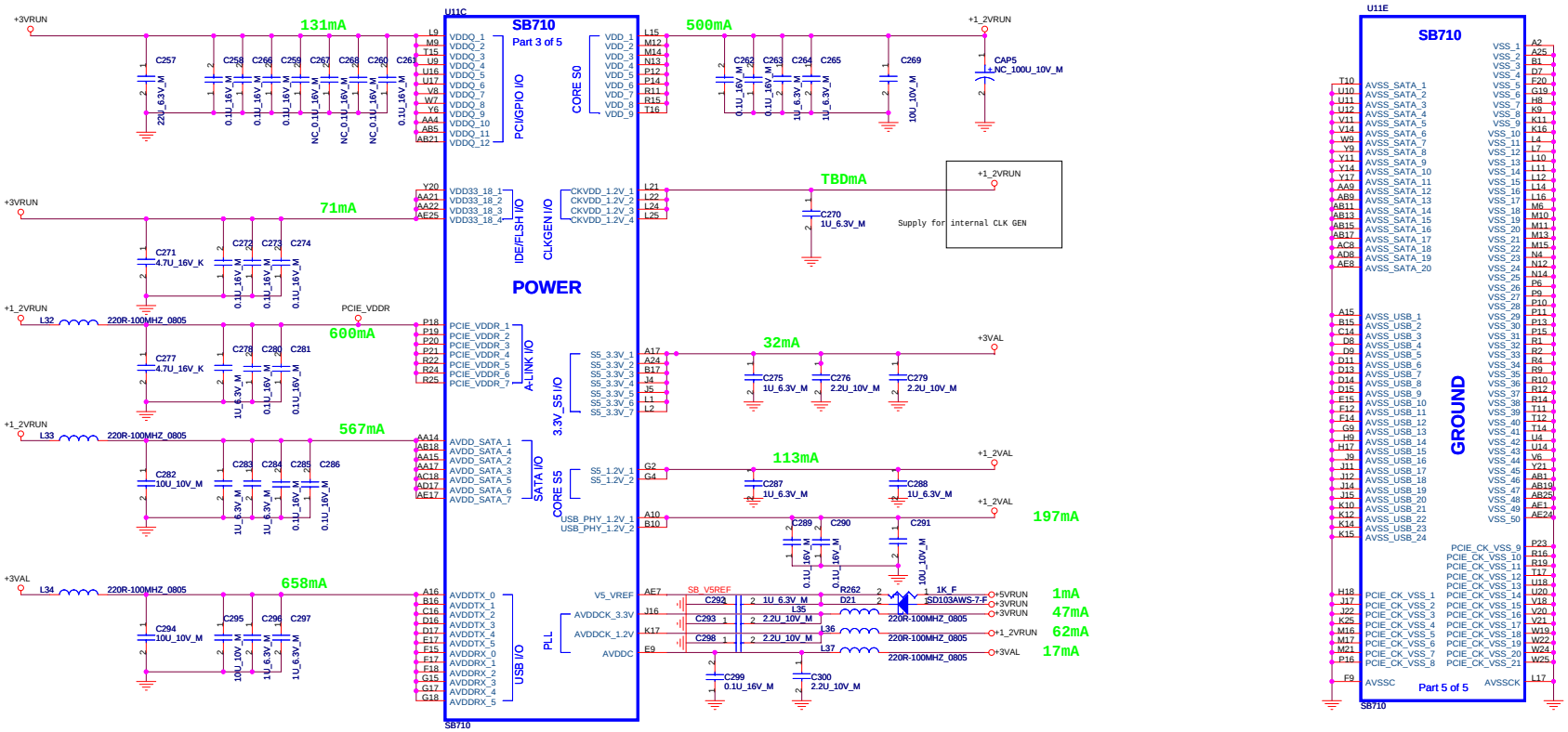

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COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
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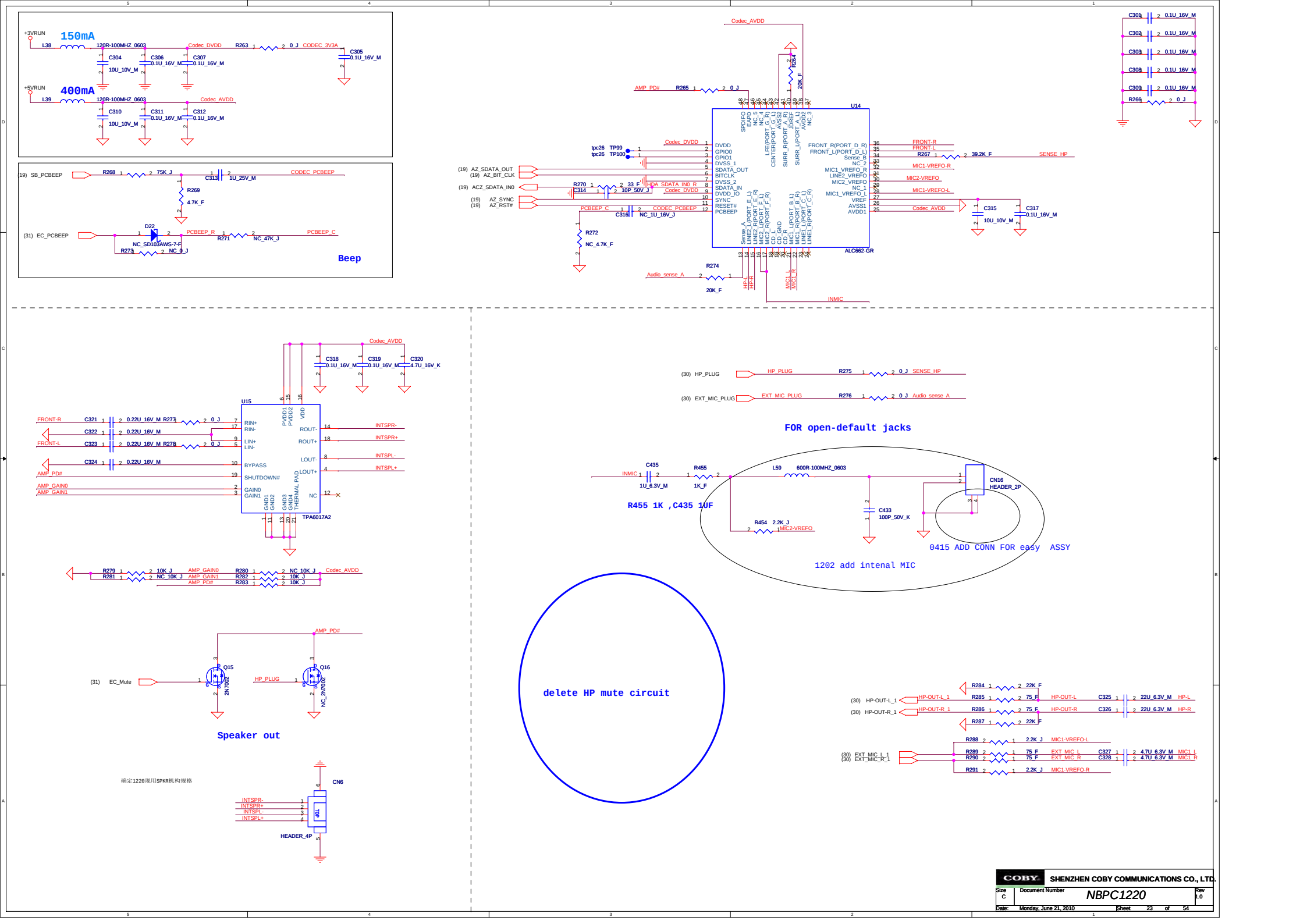
+3VRUN
150mA
L38
120R-100MHZ_0603
Codec_DVDD
R263
0_J
CODEC_3V3A
C304
10U_10V_M
C306
0.1U_16V_M
C307
0.1U_16V_M
C305
0.1U_16V_M
+5VRUN
400mA
L39
120R-100MHZ_0603
Codec_AVDD
C310
10U_10V_M
C311
0.1U_16V_M
C312
0.1U_16V_M
(19) SB_PCBEEP
R268
75K_J
C313
1U_25V_M
CODEC_PCBEEP
R269
4.7K_F
(31) EC_PCBEEP
D22
NC_SD103AWS-7-F
PCBEEP_R
R271
NC_47K_J
PCBEEP_C
R273
NC_0_J
Beep
Codec_AVDD
R264
20K_F
AMP_PD#
R265
0_J
U14
ALC662-GR
Codec_DVDD
tpc26 TP99
tpc26 TP100
(19) AZ_SDATA_OUT
(19) AZ_BIT_CLK
(19) ACZ_SDATA_IN0
(19) AZ_SYNC
(19) AZ_RST#
R270
33_F
C314
10P_50V_J
HDA_SDATA_IN0_R
PCBEEP_C
C316
NC_1U_16V_J
CODEC_PCBEEP
R272
NC_4.7K_F
Audio_sense_A
R274
20K_F
INMIC
FRONT-R
FRONT-L
R267
39.2K_F
SENSE_HP
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
C315
10U_10V_M
C317
0.1U_16V_M
C301
C302
C303
C308
C309
0.1U_16V_M
R266
0_J
U15
TPA6017A2
C318
0.1U_16V_M
C319
0.1U_16V_M
C320
4.7U_16V_K
FRONT-R
C321
0.22U_16V_M
R277
0_J
C322
0.22U_16V_M
FRONT-L
C323
0.22U_16V_M
R278
0_J
C324
0.22U_16V_M
AMP_PD#
AMP_GAIN0
AMP_GAIN1
INTSPR-
INTSPR+
INTSPL-
INTSPL+
R279
10K_J
R281
NC_10K_J
R280
NC_10K_J
R282
10K_J
R283
10K_J
(30) HP_PLUG
HP_PLUG
R275
0_J
SENSE_HP
(30) EXT_MIC_PLUG
EXT_MIC_PLUG
R276
0_J
Audio_sense_A
FOR open-default jacks
C435
1U_6.3V_M
R455
1K_F
INMIC
R455 1K ,C435 1UF
L59
600R-100MHZ_0603
CN16
HEADER_2P
C433
100P_50V_K
R454
2.2K_J
MIC2-VREFO
0415 ADD CONN FOR easy ASSY
1202 add intenal MIC
Q15
Q16
2N7002
NC_2N7002
(31) EC_Mute
HP_PLUG
Speaker out
delete HP mute circuit
R284
22K_F
(30) HP-OUT-L_1
HP-OUT-L_1
R285
75_F
HP-OUT-L
C325
22U_6.3V_M
HP-L
(30) HP-OUT-R_1
HP-OUT-R_1
R286
75_F
HP-OUT-R
C326
22U_6.3V_M
HP-R
R287
22K_F
R288
2.2K_J
MIC1-VREFO-L
(30) EXT_MIC_L_1
(30) EXT_MIC_R_1
R289
75_F
EXT_MIC_L
C327
4.7U_6.3V_M
MIC1_L
R290
75_F
EXT_MIC_R
C328
4.7U_6.3V_M
MIC1_R
R291
2.2K_J
MIC1-VREFO-R
确定1220现用SPKR机构规格
CN6
INTSPR-
INTSPR+
INTSPL-
INTSPL+
HEADER_4P
COBY
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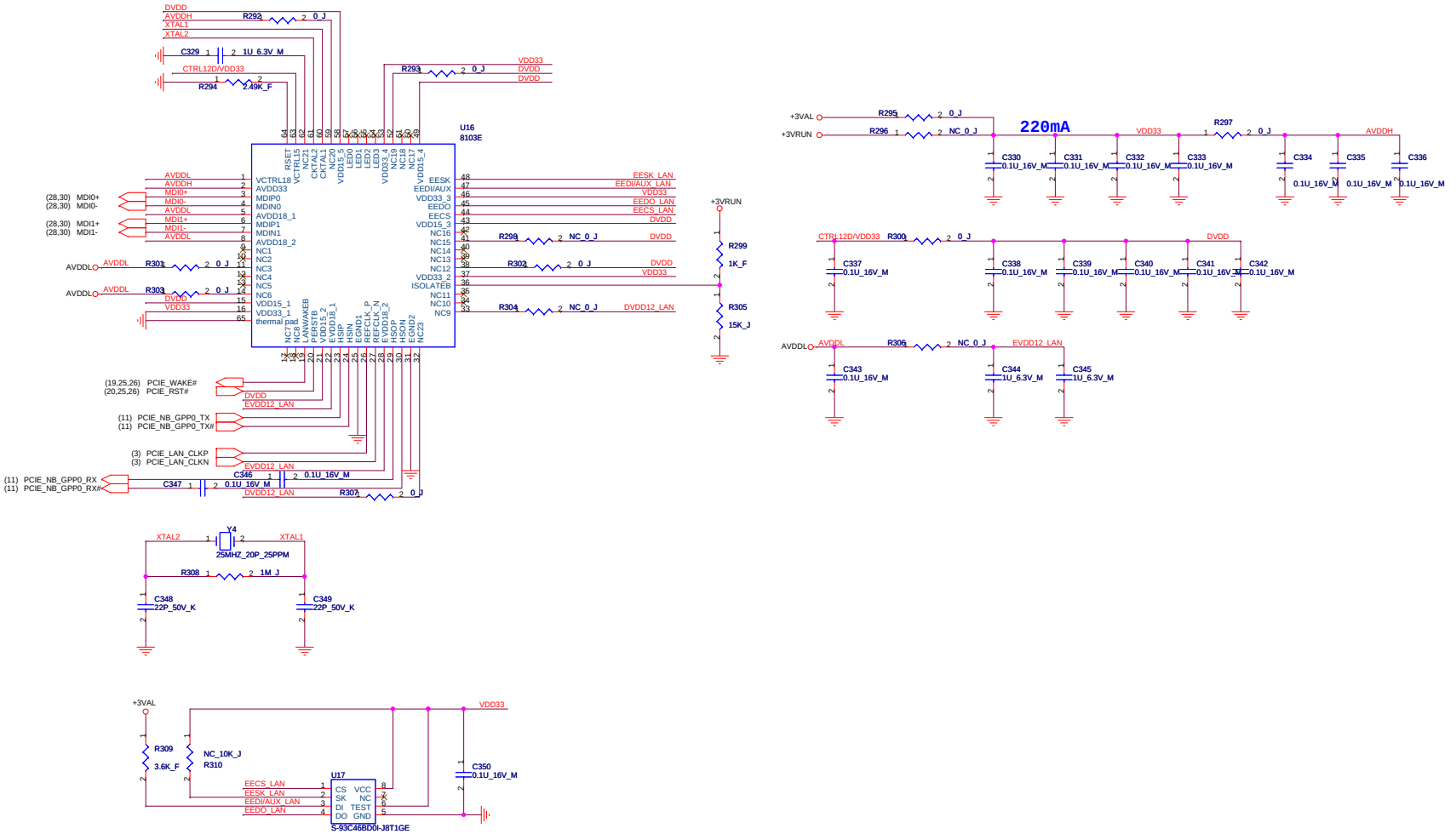

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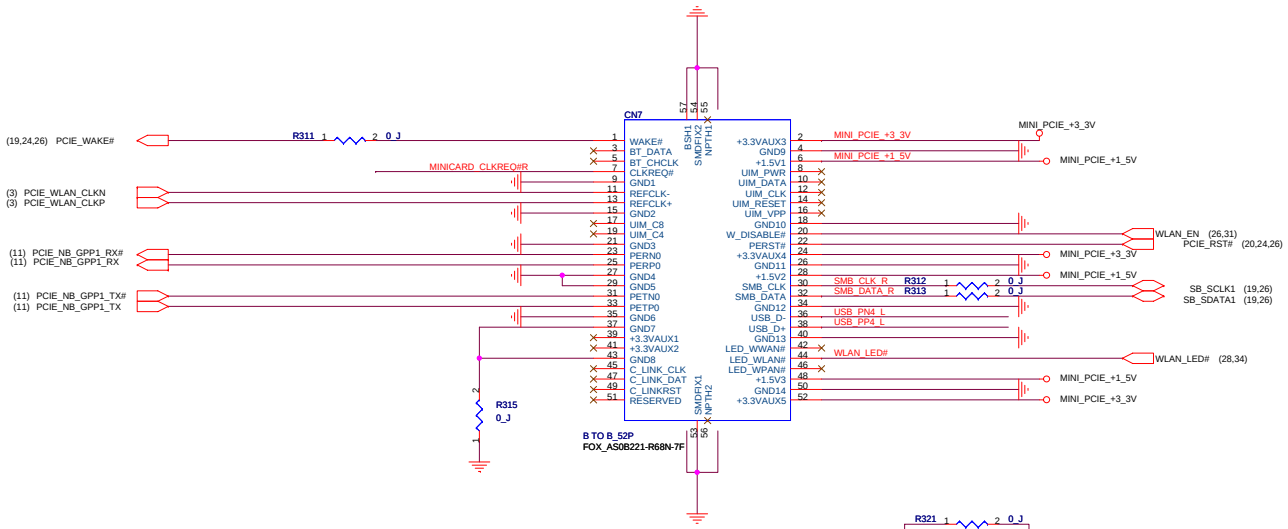

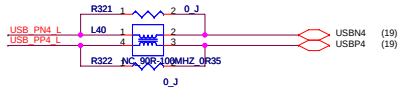

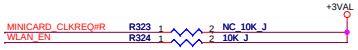

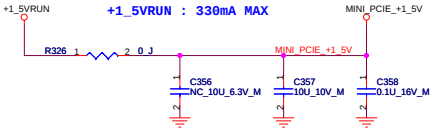

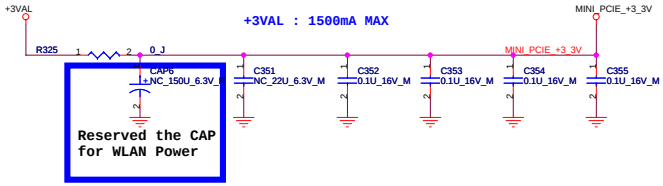

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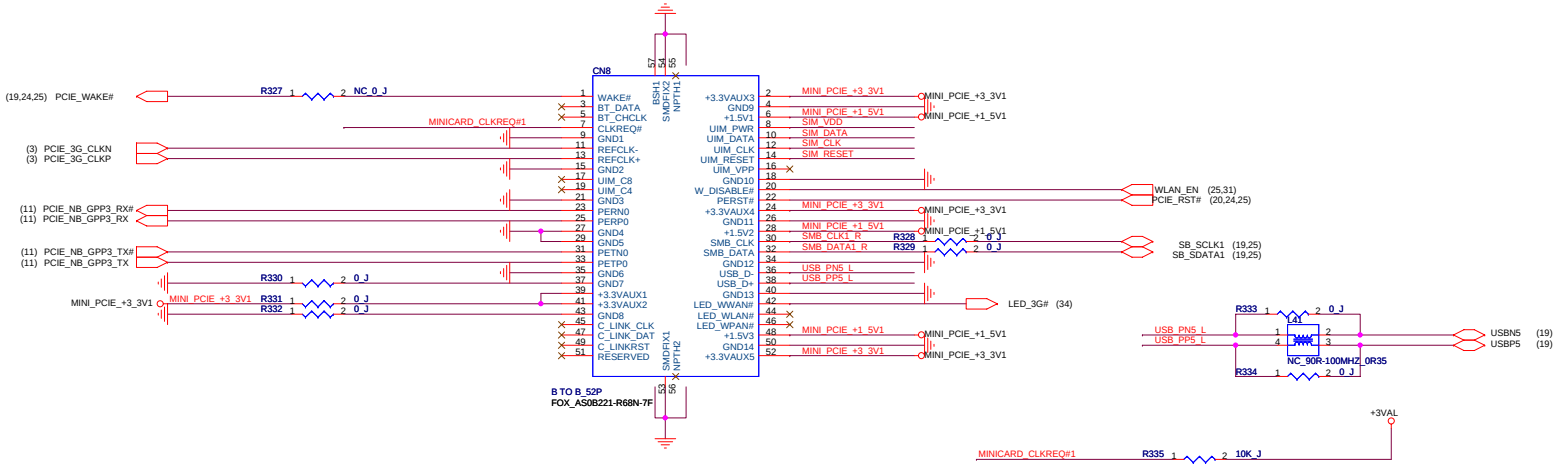
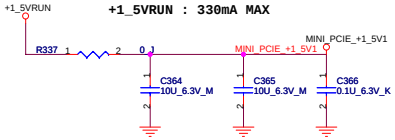
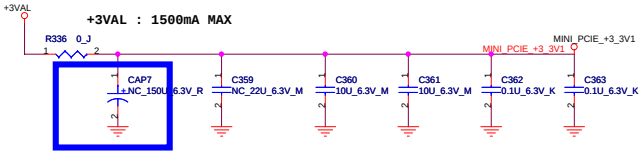
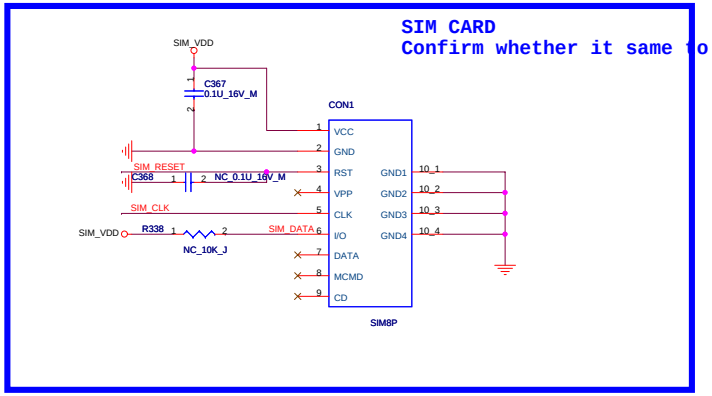
colayout with express card!usb sigbal pin copins with express card







Reserved the CAP
for WLAN Power



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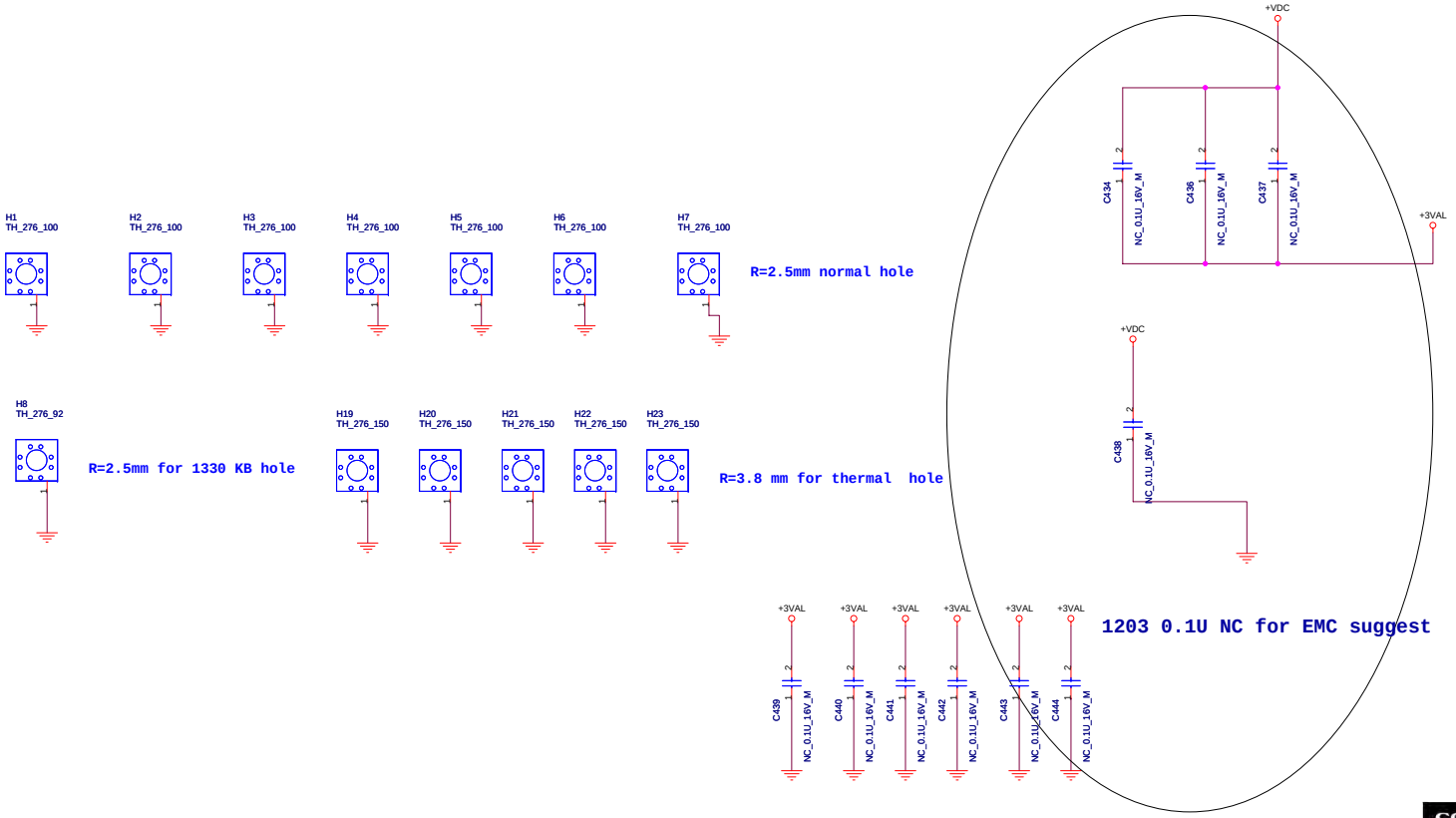

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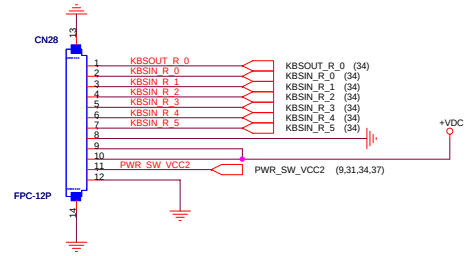
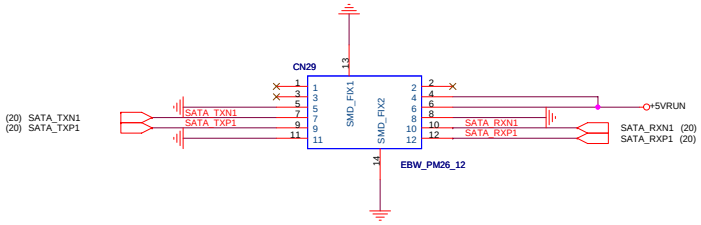


ALL IN ONE SWITCH BOARD CONN



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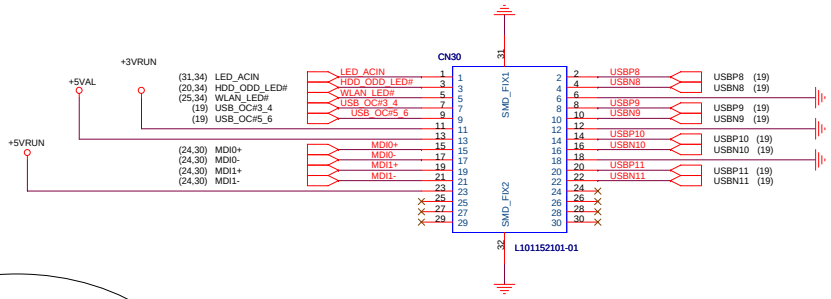
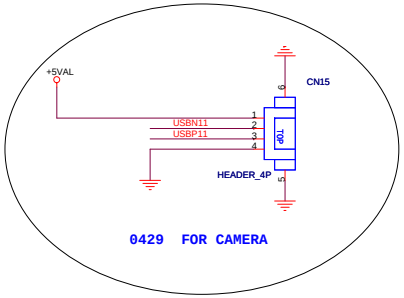


ALL IN ONE BACK IO CONN



0429 FOR CAMERA

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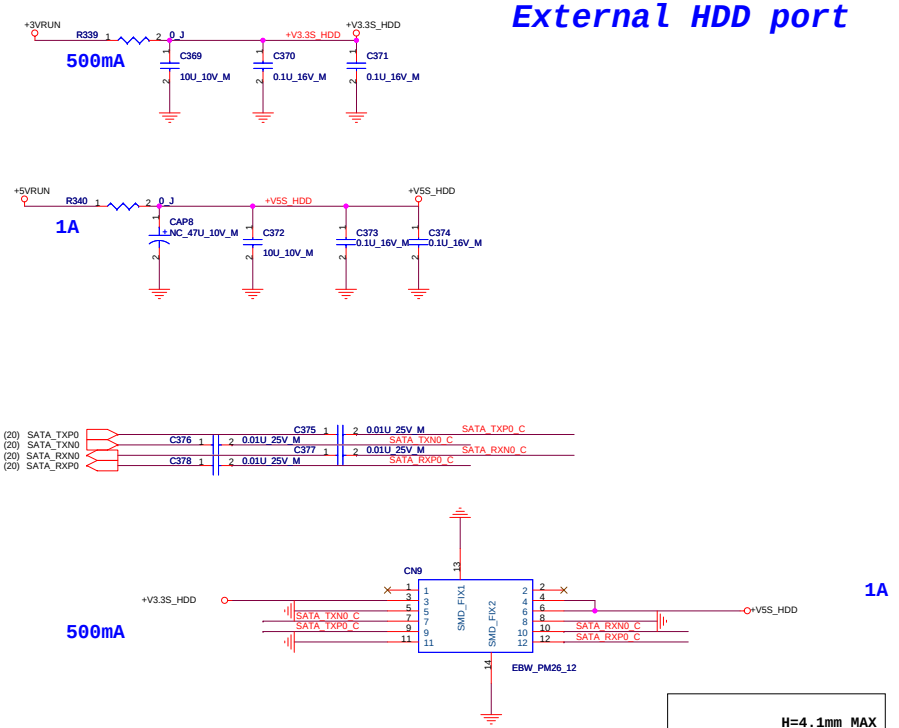
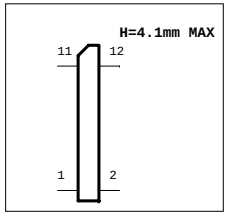
External HDD port



CONNECTOR same to 1028



DELETE SATA ODD CONN

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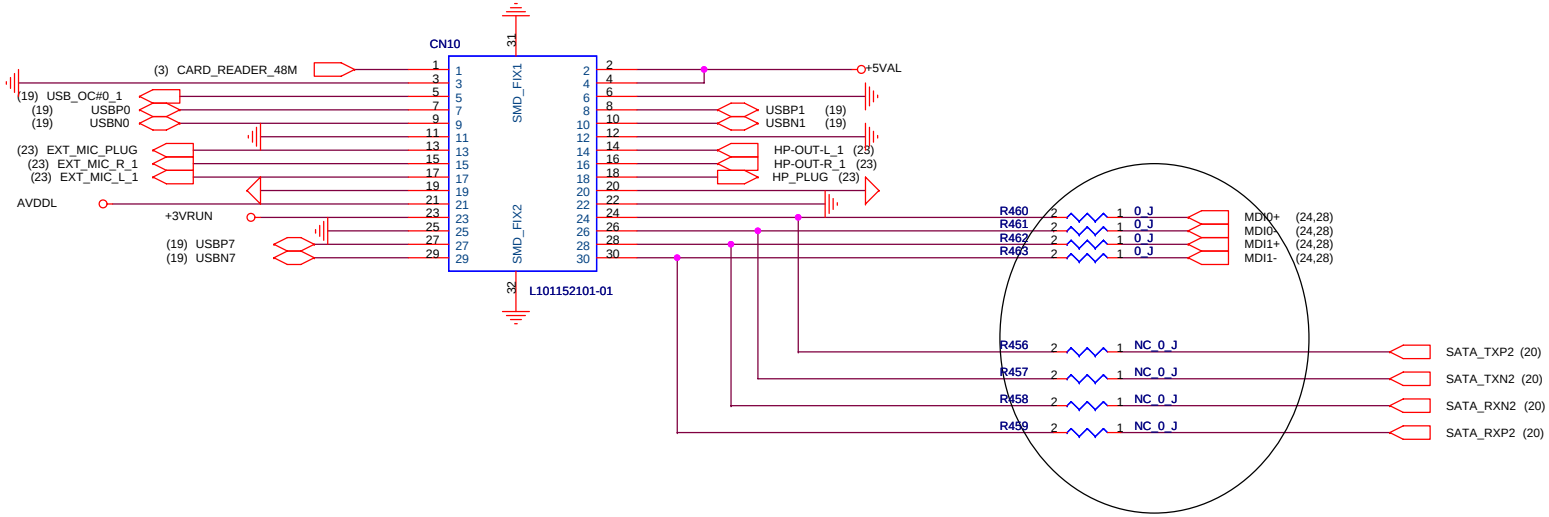
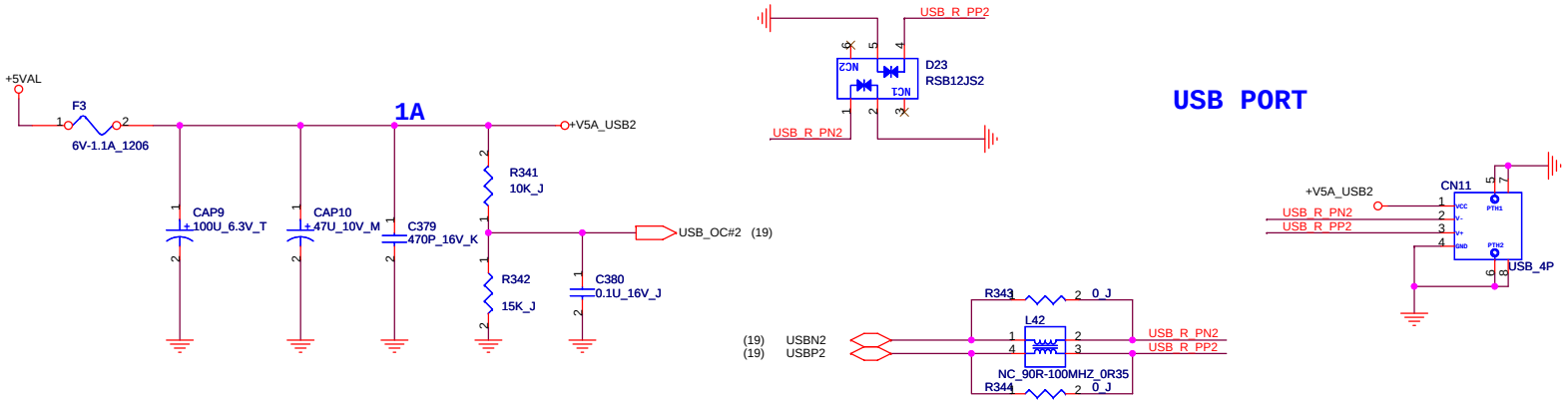


NOTBOOK WITH ALL IN ONE COLAY



USB PORT

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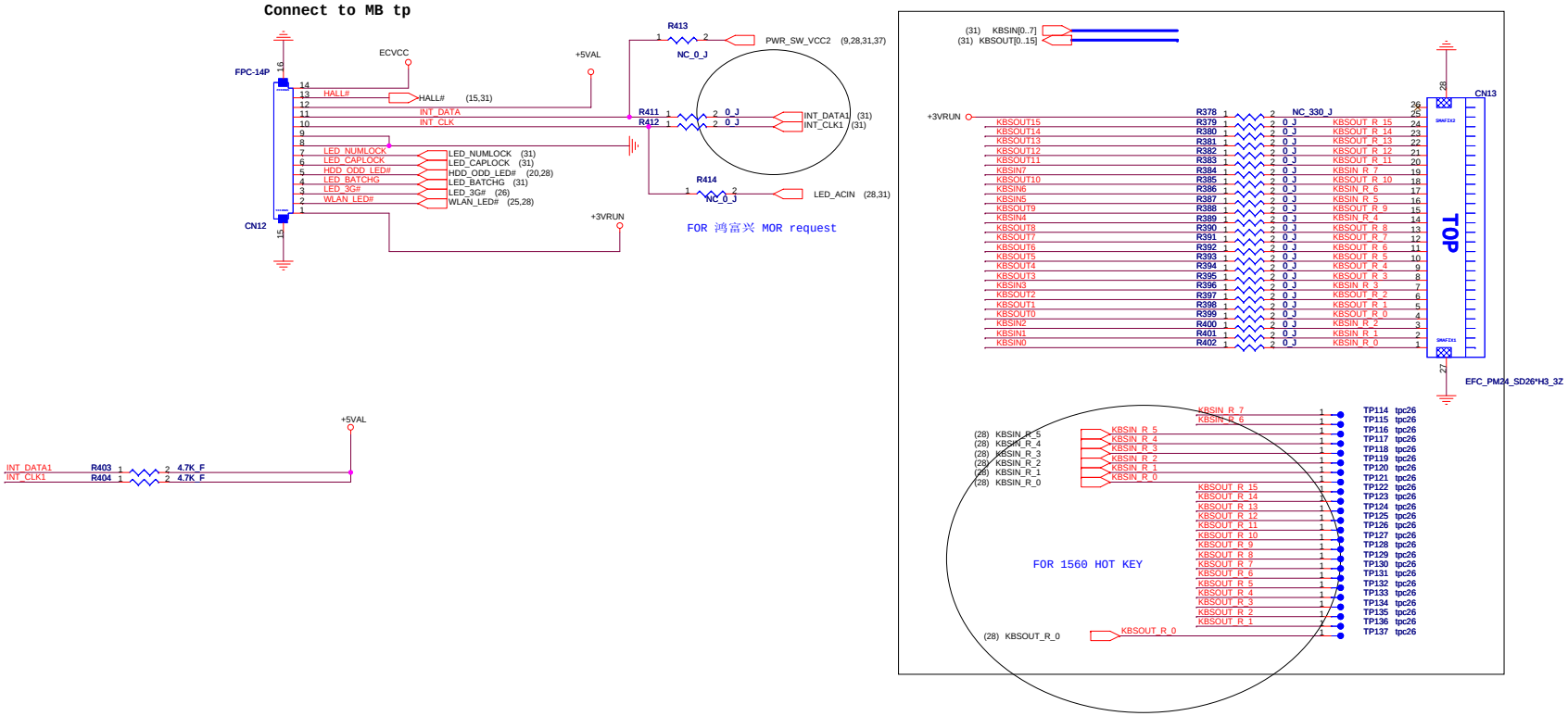
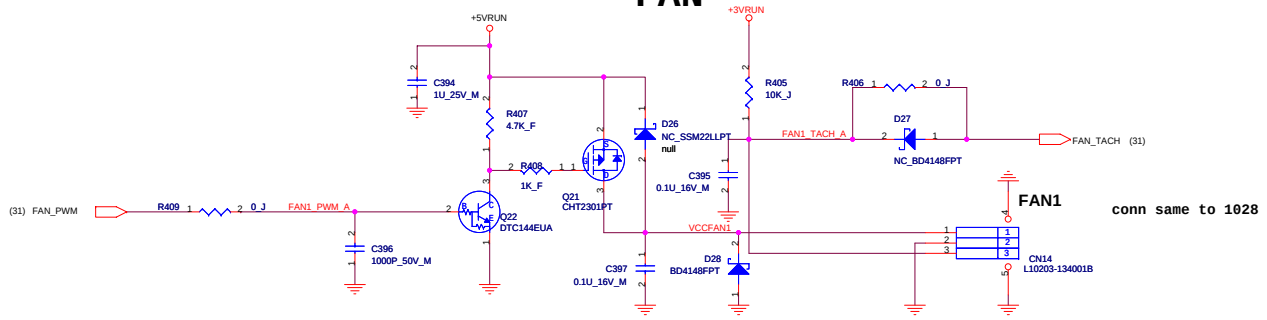
Connect to MB tp



FAN



COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.	
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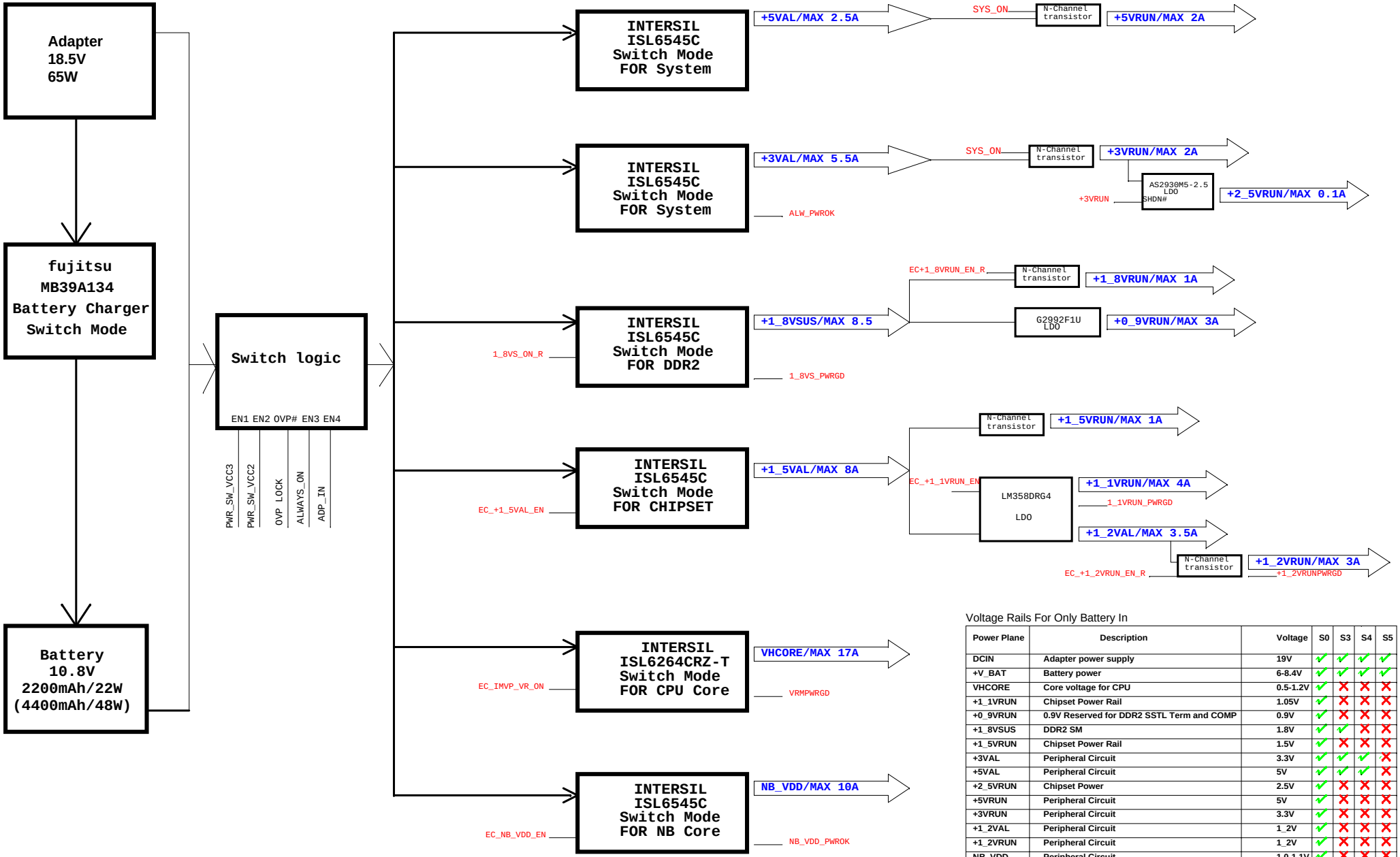

Voltage Rails For Only Battery In

Power Plane	Description	Voltage	S0	S3	S4	S5
DCIN	Adapter power supply	19V	✓	✓	✓	✓
+V_BAT	Battery power	6-8.4V	✓	✓	✓	✓
VHCORE	Core voltage for CPU	0.5-1.2V	✓	✗	✗	✗
+1_1VRUN	Chipset Power Rail	1.05V	✓	✗	✗	✗
+0_9VRUN	0.9V Reserved for DDR2 SSTL Term and COMP	0.9V	✓	✗	✗	✗
+1_8VSUS	DDR2 SM	1.8V	✓	✓	✗	✗
+1_5VRUN	Chipset Power Rail	1.5V	✓	✗	✗	✗
+3VAL	Peripheral Circuit	3.3V	✓	✓	✓	✗
+5VAL	Peripheral Circuit	5V	✓	✓	✓	✗
+2_5VRUN	Chipset Power	2.5V	✓	✗	✗	✗
+5VRUN	Peripheral Circuit	5V	✓	✗	✗	✗
+3VRUN	Peripheral Circuit	3.3V	✓	✗	✗	✗
+1_2VAL	Peripheral Circuit	1_2V	✓	✗	✗	✗
+1_2VRUN	Peripheral Circuit	1_2V	✓	✗	✗	✗
NB_VDD	Peripheral Circuit	1.0-1.1V	✓	✗	✗	✗

✗ OFF
✓ ON

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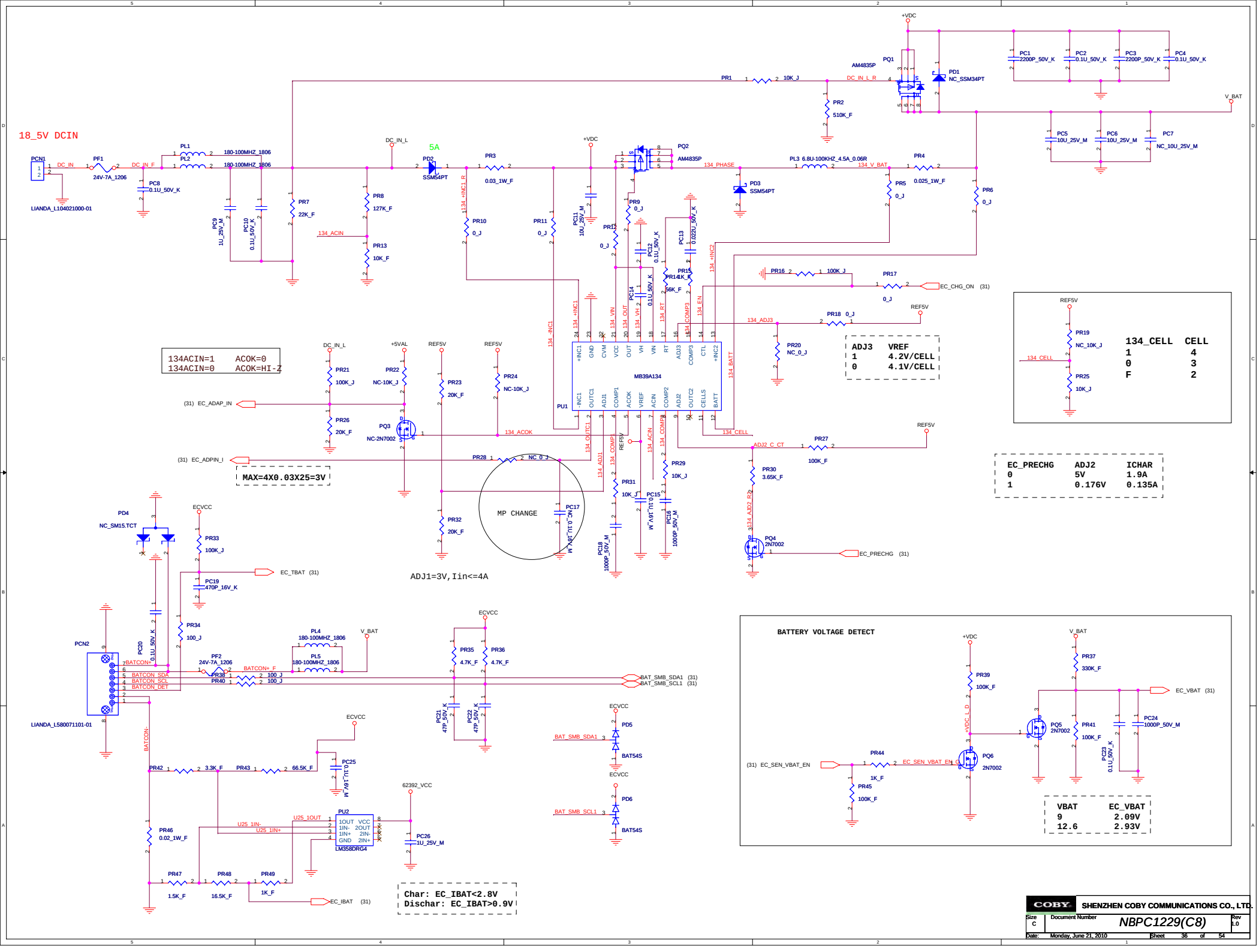
18_5V DCIN
PCN1
DC_IN
LIANDA_L104021000-01
PF1
24V-7A_1206
PL1
PL2
180-100MHZ_1806
PC8
0.1U_50V_K
PC9
1U_25V_M
PC10
0.1U_50V_K
PR7
22K_F
PR8
127K_F
PR13
10K_F
134_ACIN
DC_IN_L
5A
PD2
SSM54PT
PR3
0.03_1W_F
PR10
0_J
PR11
0_J
PC11
10U_25V_M
+VDC
PQ2
AM4835P
PR9
0_J
PR12
0_J
PC12
0.1U_50V_K
PC13
0.022U_50V_K
PR14
56K_F
PR15
1K_F
PC14
0.1U_50V_K
134_PHASE
PD3
SSM54PT
PL3 6.8U-100KHZ_4.5A_0.06R
134_V_BAT
PR4
PR5
0.025_1W_F
0_J
PR6
0_J
PQ1
AM4835P
PR1
10K_J
DC_IN_L_R
PR2
510K_F
PD1
NC_SSM34PT
PC1
2200P_50V_K
PC2
0.1U_50V_K
PC3
2200P_50V_K
PC4
0.1U_50V_K
V_BAT
PC5
10U_25V_M
PC6
10U_25V_M
PC7
NC_10U_25V_M
PR16
100K_J
PR17
0_J
EC_CHG_ON (31)
REF5V
PR18 0_J
134_ADJ3
PR20
NC_0_J
ADJ3 VREF
1 4.2V/CELL
0 4.1V/CELL
134_CELL CELL
1 4
0 3
F 2
PR19
NC_10K_J
PR25
10K_J
134_CELL
134 +INC1
134 -INC1
134 +INC2
134 -INC2
134 VIN
134 OUT
134 VH
134 RT
134 COMP3
134 EN
134 BATT
134 OUTC1
134 ADJ1
134 COMP1
134 ACOK
134 ACIN
134 COMP2
134 ADJ2
134 CELLS
134 ACOK=1 ACOK=0
134ACIN=0 ACOK=HI-Z
DC_IN_L
+5VAL
REF5V
PR21
100K_J
PR22
NC-10K_J
PR23
20K_F
PR24
NC-10K_J
PU1
MB39A134
(31) EC_ADAP_IN
PR26
20K_F
PQ3
NC-2N7002
134_ACOK
(31) EC_ADPIN_I
PR28
NC_0_J
MAX=4X0.03X25=3V
MP CHANGE
PC17
NC_0.1U_16V_M
PR29
10K_J
PR31
10K_J
PC15
0.1U_16V_M
PC16
1000P_50V_M
PC18
1000P_50V_M
ADJ2_C_CT
PR27
100K_F
PR30
3.65K_F
134_ADJ2_R
PQ4
2N7002
EC_PRECHG (31)
EC_PRECHG ADJ2 ICHAR
0 5V 1.9A
1 0.176V 0.135A
ADJ1=3V,Iin<=4A
PD4
NC_SM15.TCT
ECVCC
PR33
100K_J
EC_TBAT (31)
PC19
470P_16V_K
PR34
100_J
PCN2
LIANDA_L580071101-01
PC20
0.1U_50V_K
7BATCON+
BATCON_SDA
BATCON_SCL
BATCON_DET
PF2
24V-7A_1206
BATCON+_F
PR38
PR40
100_J
PL4
180-100MHZ_1806
PL5
180-100MHZ_1806
V_BAT
PR35
4.7K_F
PR36
4.7K_F
BAT_SMB_SDA1 (31)
BAT_SMB_SCL1 (31)
PC21
47P_50V_K
PC22
47P_50V_K
BATCON-
PR42
3.3K_F
PR43
66.5K_F
PC25
0.1U_16V_M
PR46
0.02_1W_F
U25_1IN-
U25_1IN+
U25_1OUT
PU2
LM358DRG4
1OUT VCC
1IN- 2OUT
1IN+ 2IN-
GND 2IN+
62392_VCC
PC26
1U_25V_M
PR47
1.5K_F
PR48
16.5K_F
PR49
1K_F
EC_IBAT (31)
Char: EC_IBAT<2.8V
Dischar: EC_IBAT>0.9V
BAT_SMB_SDA1
BAT_SMB_SCL1
PD5
PD6
BAT54S
BATTERY VOLTAGE DETECT
PR39
100K_F
VDC_L_D
PR37
330K_F
EC_VBAT (31)
PQ5
2N7002
PR41
100K_F
PC24
1000P_50V_M
PC23
0.1U_50V_K
(31) EC_SEN_VBAT_EN
PR44
1K_F
PR45
100K_F
EC_SEN_VBAT_EN
PQ6
2N7002
VBAT EC_VBAT
9 2.09V
12.6 2.93V
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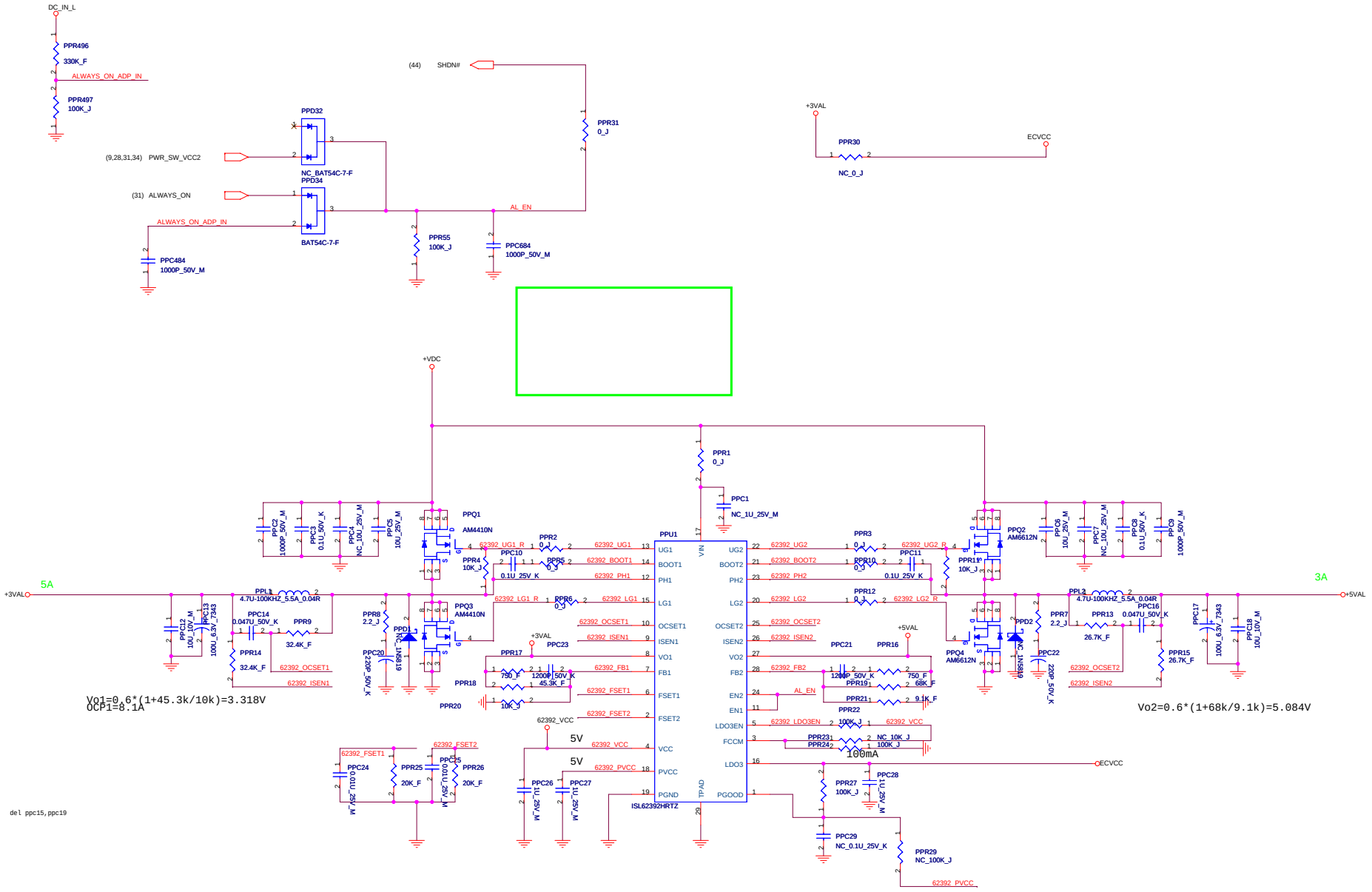

COBY	SHENZHEN COBY COMMUNICATIONS CO., LTD.		
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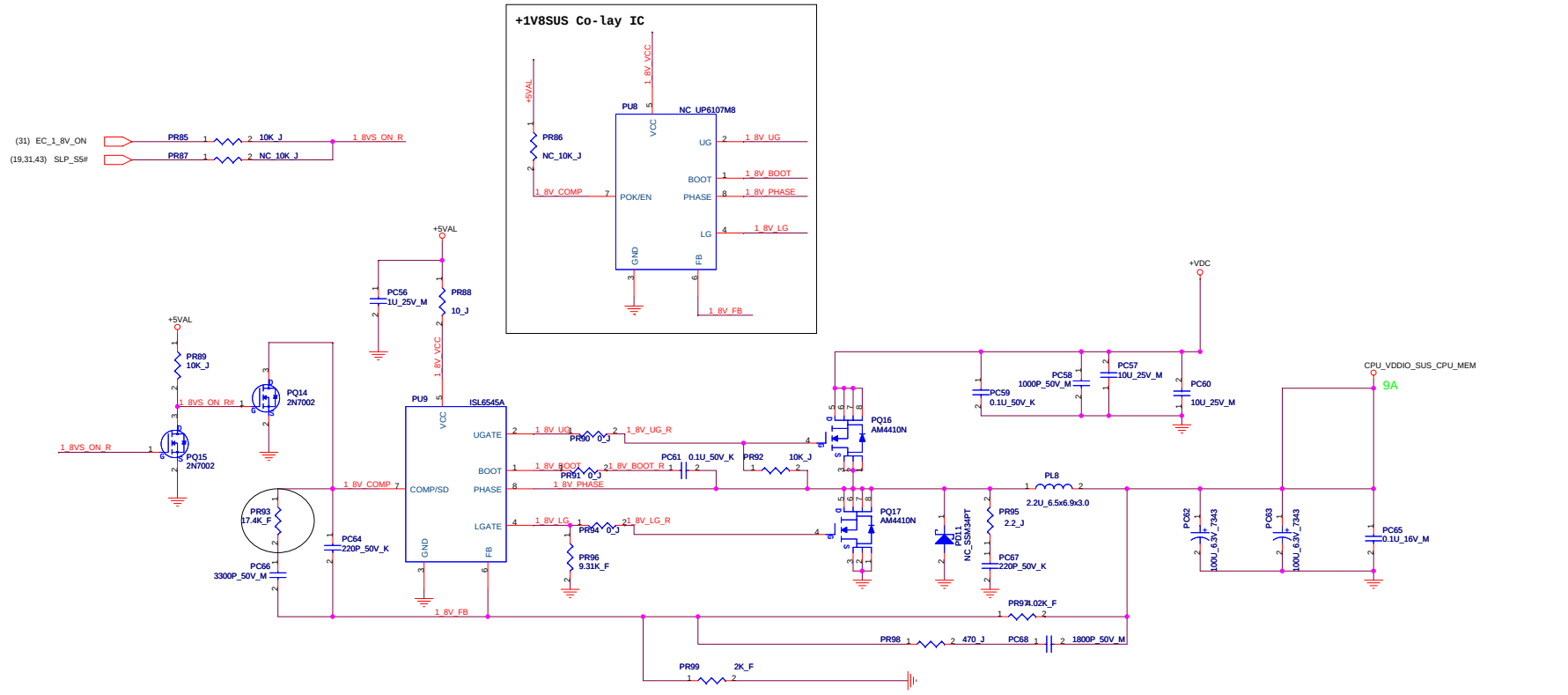

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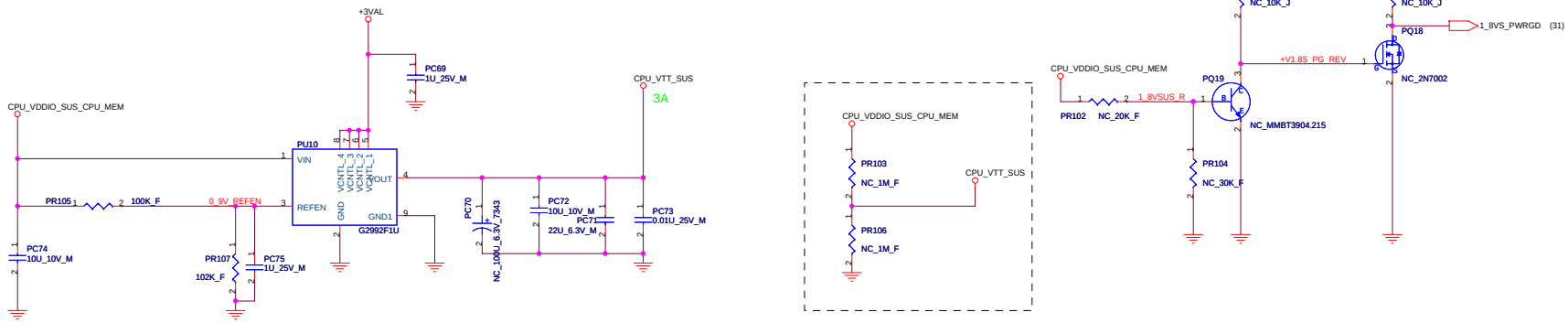

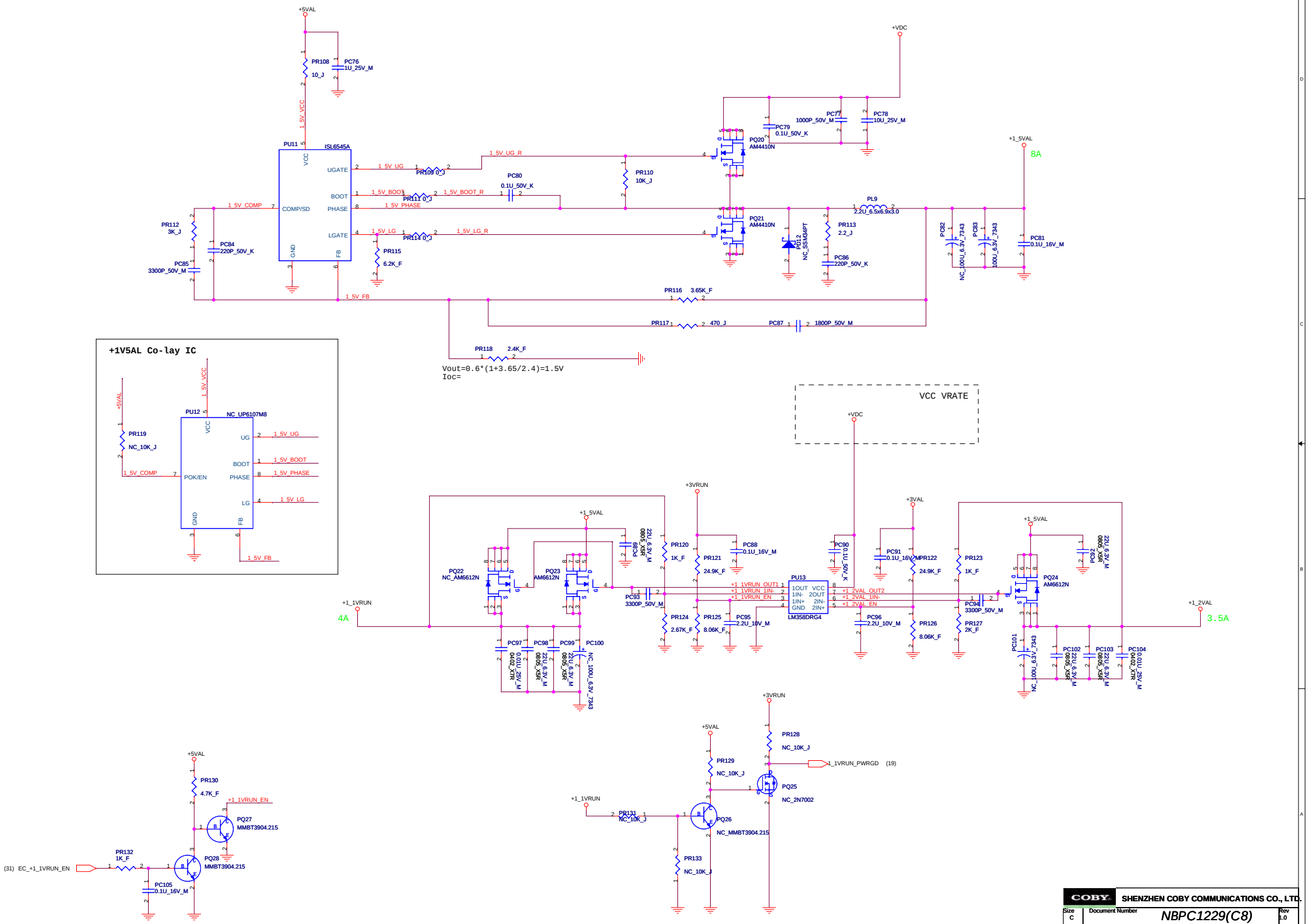

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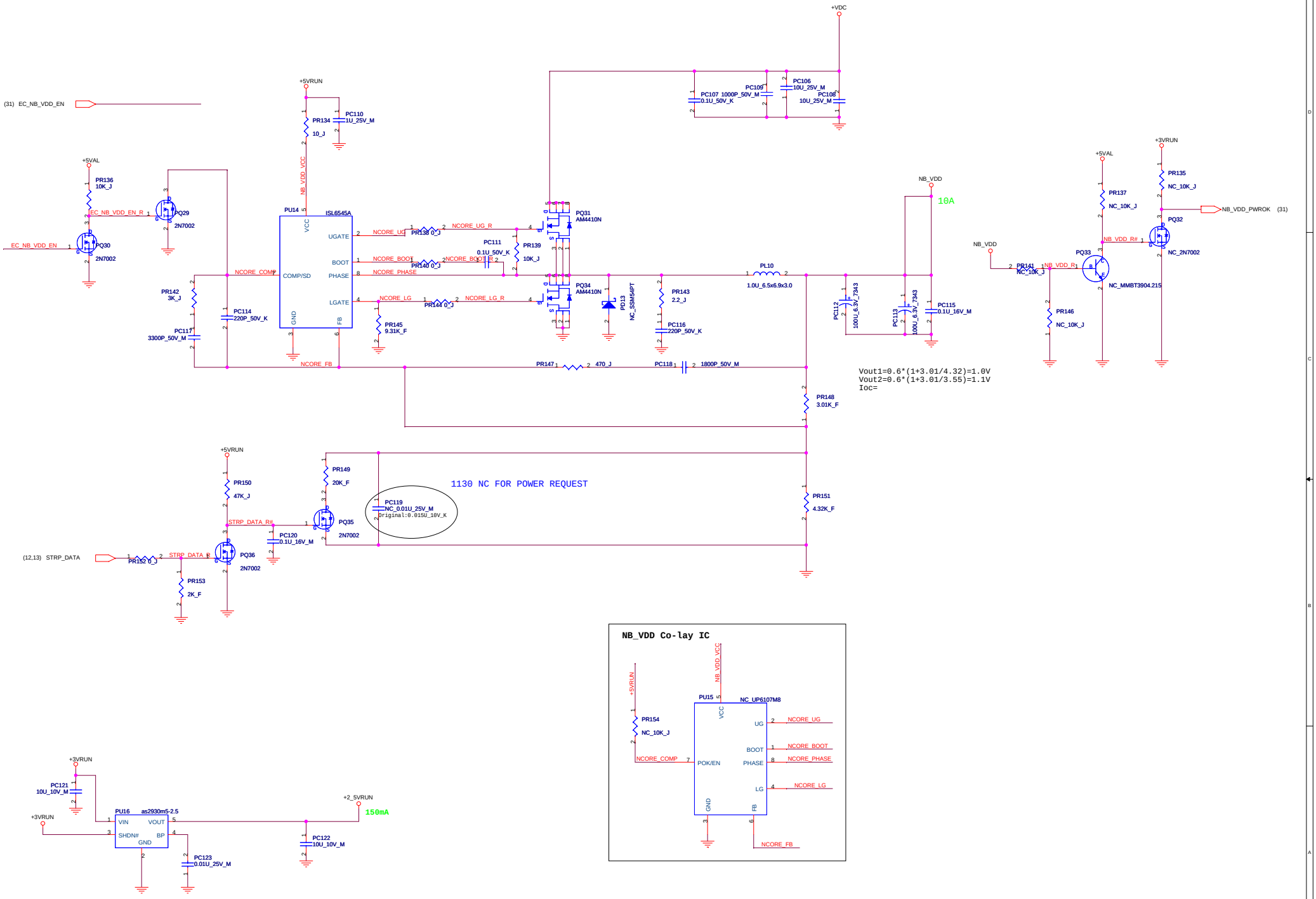

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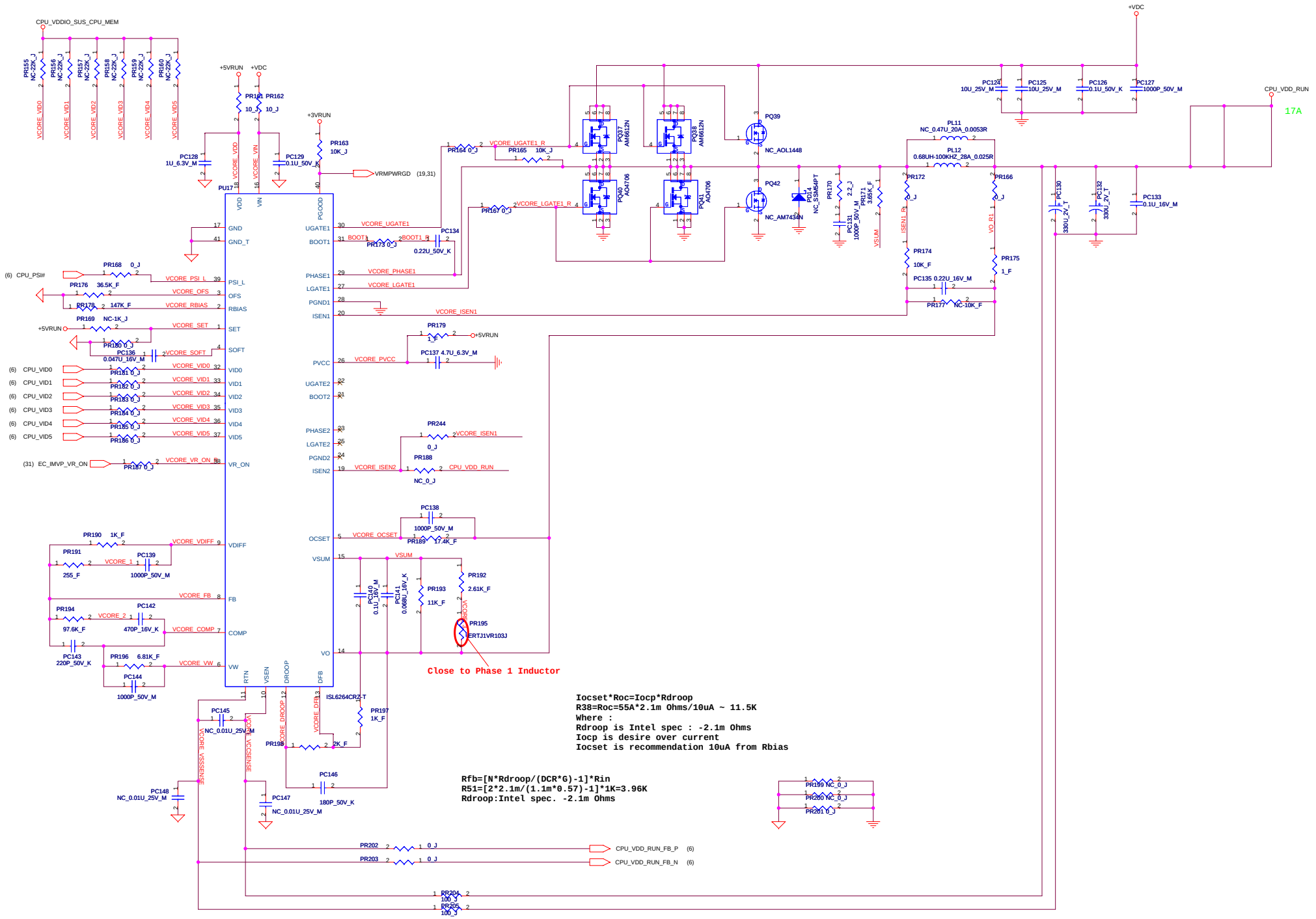

Iocset*Roc=Iocp*Rdroop
R38=Roc=55A*2.1m Ohms/10uA ~ 11.5K
Where :
Rdroop is Intel spec : -2.1m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from Rbias

Rfb=[N*Rdroop/(DCR*G)-1]*Rin
R51=[2*2.1m/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms

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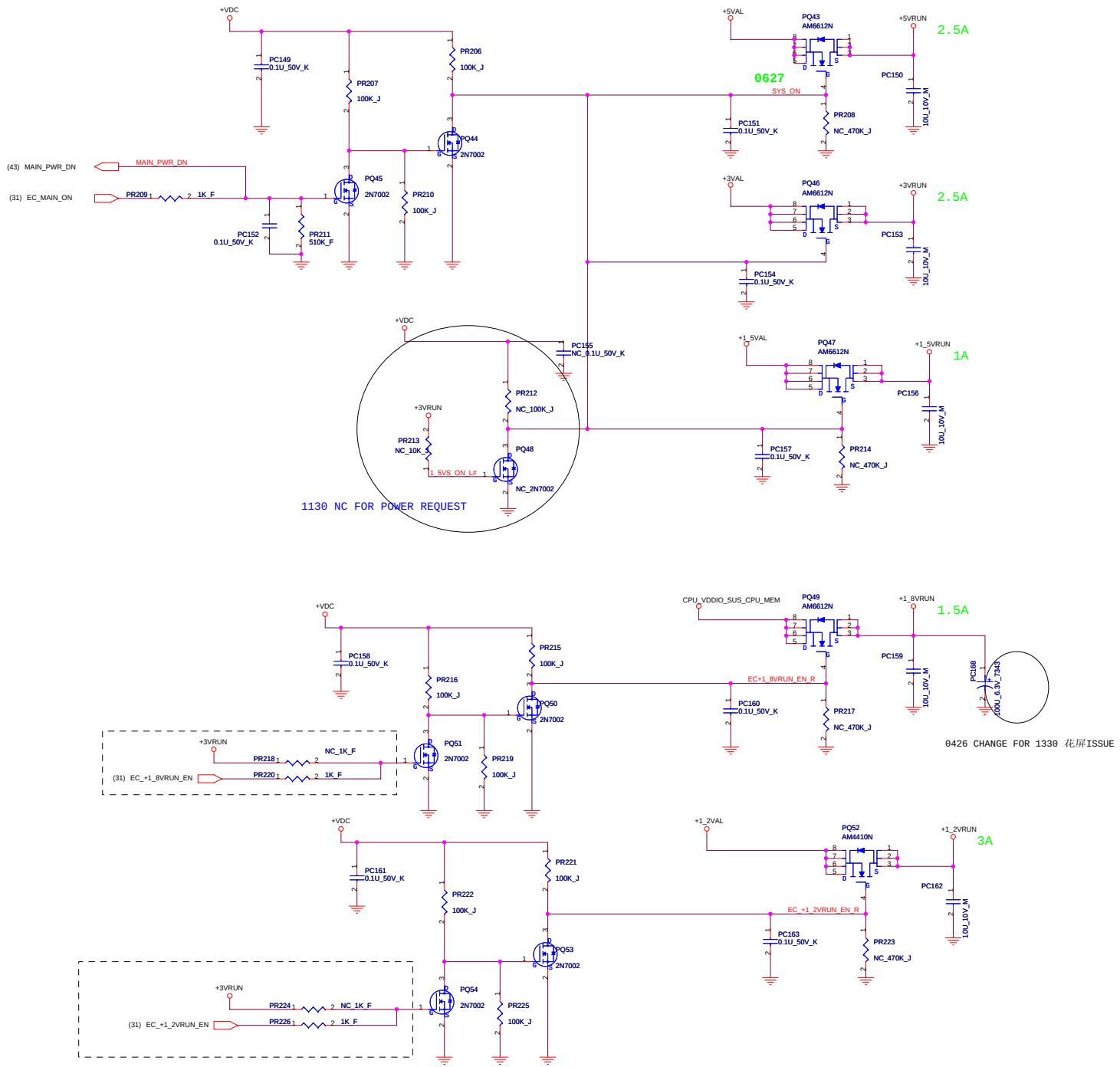

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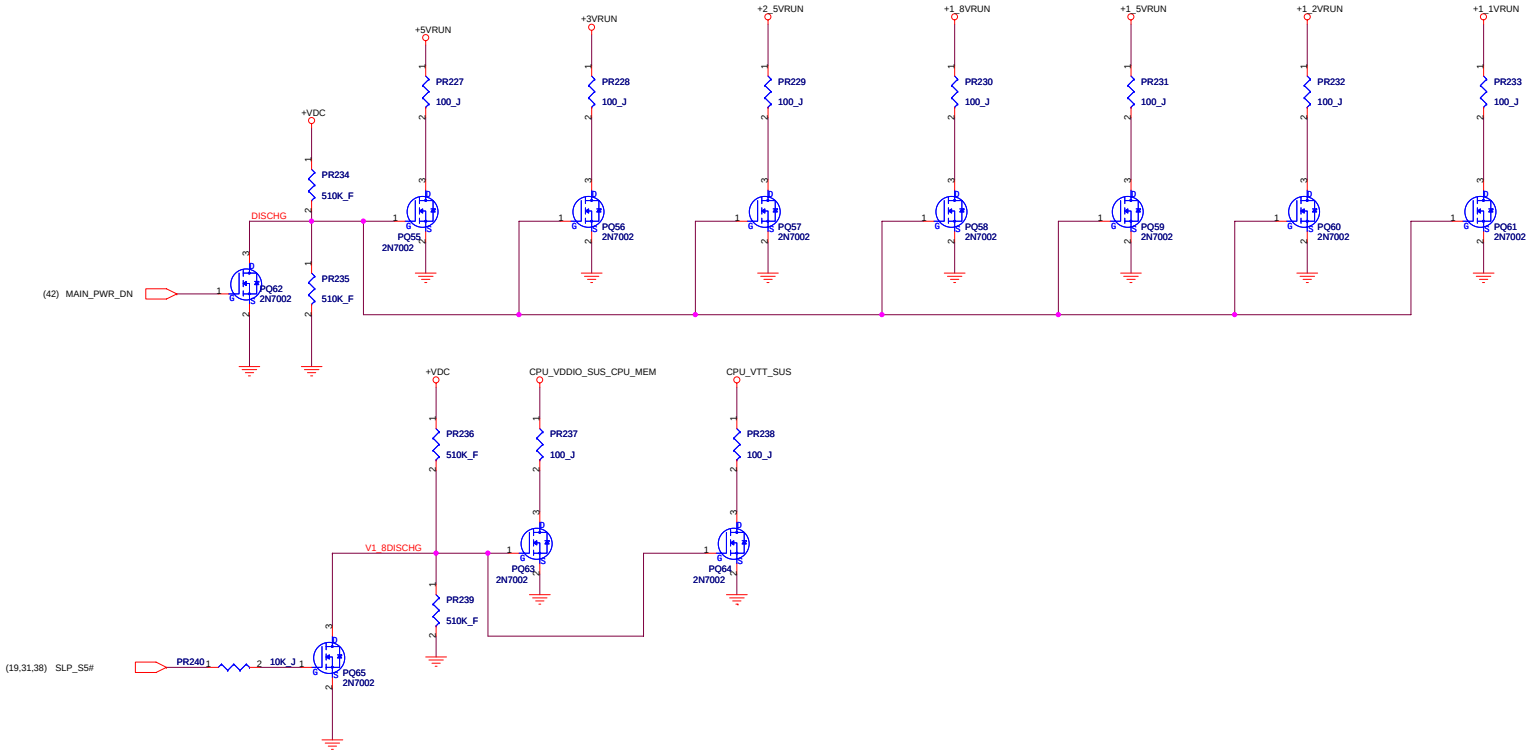

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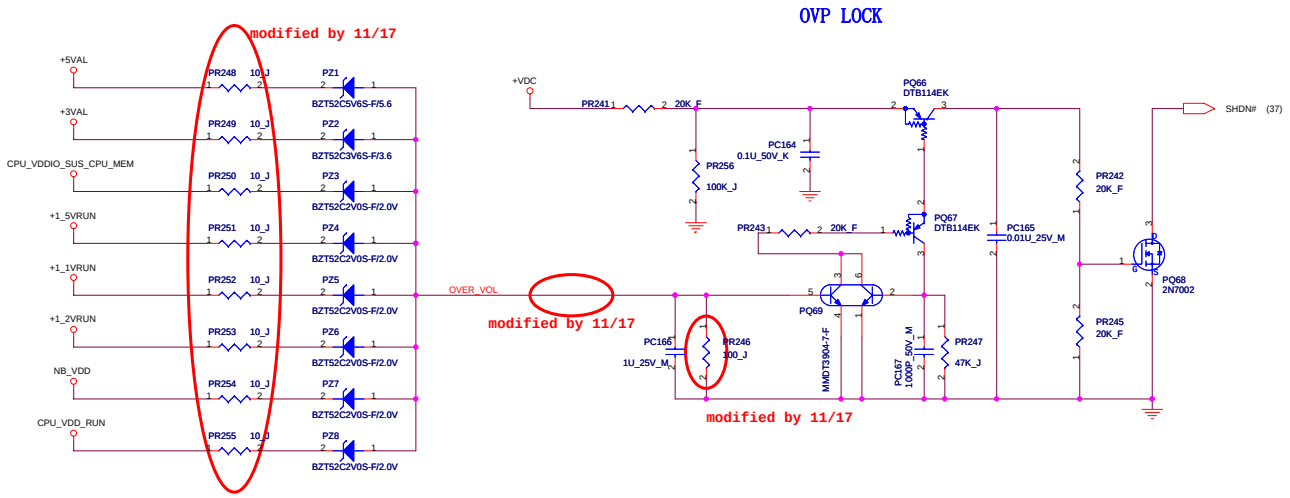

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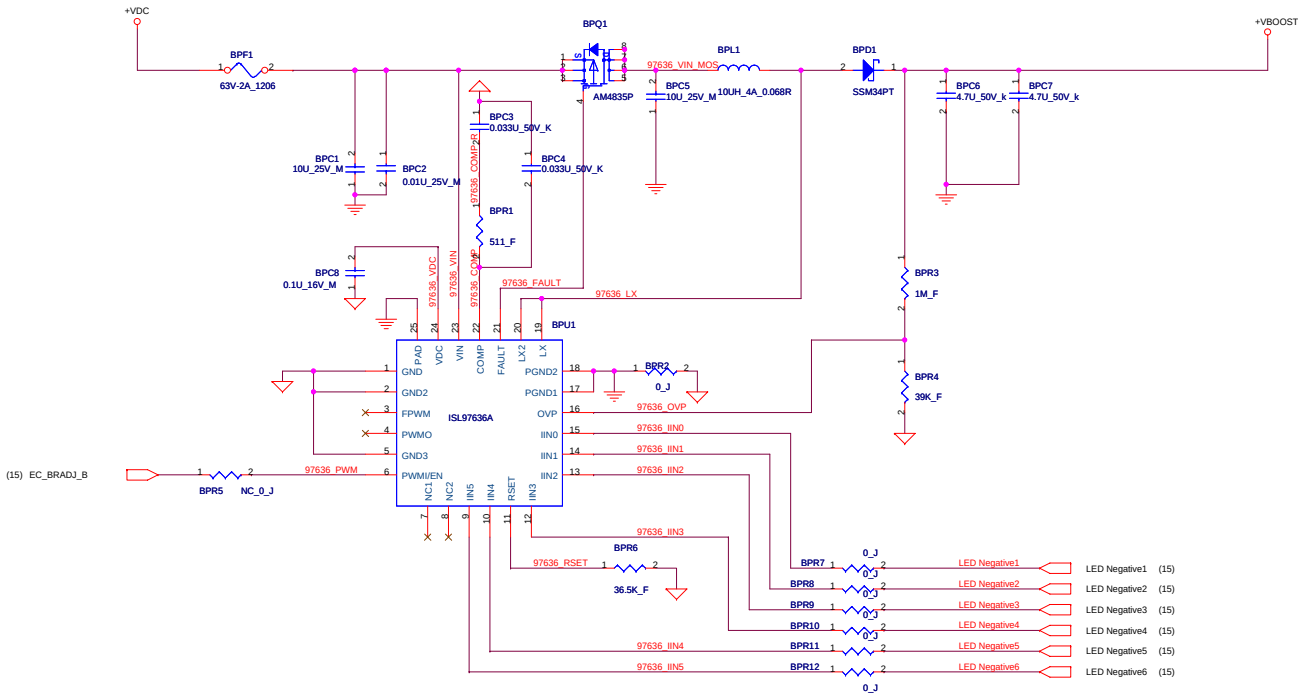

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1109 DELETE Q25 FOR AC IN LED CHANGE TO M/B
1109 ADD LED7 and R449 for AC IN LED CHANGE TO M/B
1111 ADD Y6,R450,R431,R432 ALL NC FOR EMI SUGGEST
1112 delete R68,D2 FOR DELETE HDT CONN
1112 modify LED boost circuit for change to intersil solution
1117 delete PR2441,ADD PR248---PR255 FOR OVP CIRCUIT CHANGE
1117 PR246 FORM 20K CHANGE TO 100 ohm for OVP CIRCUIT CHANGE
1120 change cn17 footprint same to 1028
1123 ADD R451,R452 FOR BOOST Control
1123 CHANEG DDR2 PIN DEFINITION FOR LAYOUT REQUEST
1124 add LED8,R453 for ME REQUEST 2 POWER LED
1125 CHANGE Q5 TO ANALOG POWER AM2341P
1125 CHANGE U3 FOOTPRINT
1130 PR213,PR212,PC155,PQ48 NC FOR POWER REQUEST
1130 PC119 NC FOR POWER REQUEST
1130 ADD PR244 FOR POWER REQUEST
1202 add C435,R455,L59,R454,C433 FOR new add internal MIC function
1207 PR2 FORM 100K CHANGE TO 510K FOR POWER REQUEST

2010,0120 DELETE D 触发器
2010,0120 ADD ALL IN ONE CONN
2010,0120 Q16 NC
2010,0120 +3V,5V POWER CHANGE
2010,0120 R316,R317,R318,R319,R320 NC
2010,0120 ADD ECVCC SIGNAL
2010,0120 POWER RESISTOR MODIFY
2010,0120 POWER RESISTOR MODIFY
2010,01208 delete DB CIRCUIT

Title <Title>		
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