iNode Rev 03 PCB Justification

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1 Overview

This document summarizes modifications made to the Rev 02 iNode PCB assemblies for simulating Rev 03 boards. It also provides justification as to why these modifications accurately simulate expected FCC testing results.

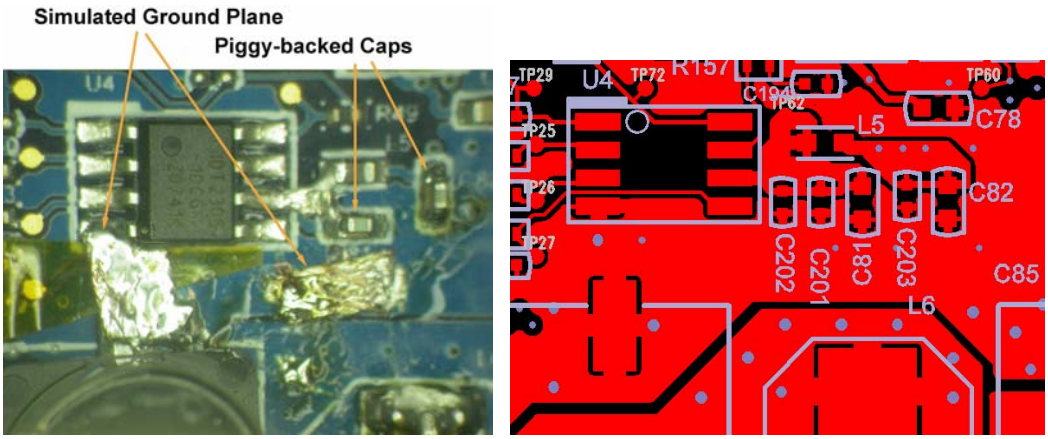
2 Xscale PCB Modifications

This section spells out modifications made to the Xscale PCB. Each sub-section lists an individual mod and compares the modification to the actual layout change.

2.1 *Grounding Scheme at Clock Buffer*

The main offender regarding spurious emissions <1GHz was the PCI clock buffer chip and it's power/grounding scheme. This was modified to utilize solid ground plane connection back to the power supply, extra supply and ground vias, and extra bypass capacitors.

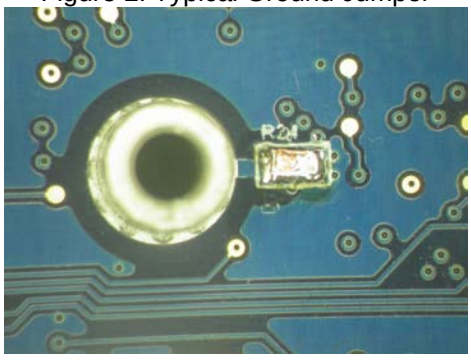
Figure 1: Ground Plane Changes – Simulation vs. Layout



2.2 *Combine Digital Ground with Chassis Ground*

Footprints were in place (rev 02) to add shorting resistors between digital and chassis ground. Adding these in helped reduce spurious emissions. ESD and EFT were tested and passed after this addition.

Figure 2: Typical Ground Jumper



2.3 *Additional Bypass Caps in Power Supplies*

The 1.3V power supply had some spurious noise at the output of the switcher. Two small capacitors were added to remove this. Also, added two small capacitors at the end of the distribution trace, where the net crosses back to the power plane.

Figure 3: +1.3V output – simulation vs. layout

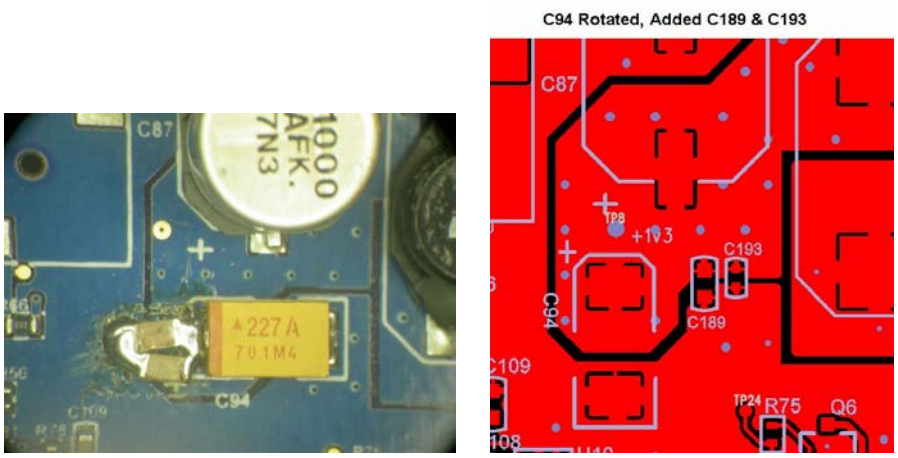


Figure 4: +1.3V at plane connection – simulation vs. layout

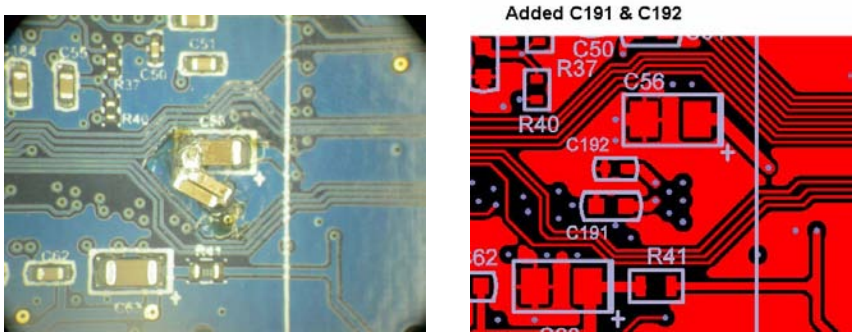
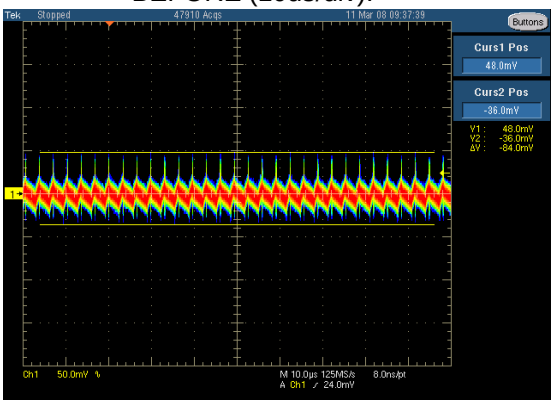


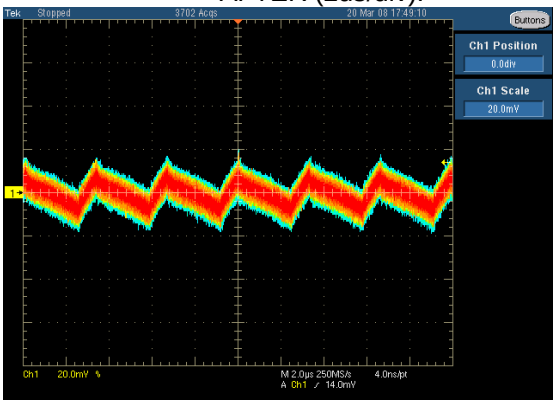
Figure 5, below, shows oscilloscope waveforms before and after the additional +1.3V bypass caps. These were taken with infinite persistence, the color differential shows intensity. The “after” picture is zoomed in just a bit to show that the spikes are definitely gone.

Figure 5: Improved +1.3V signal

BEFORE (10us/div):



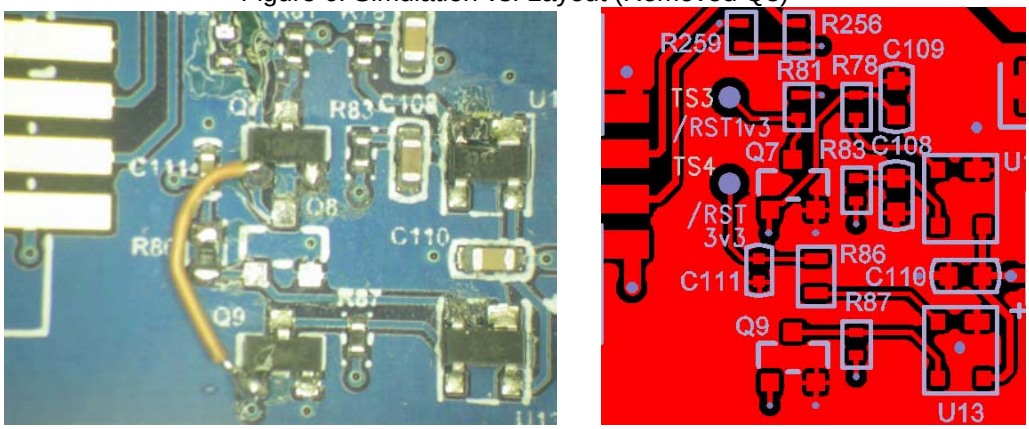
AFTER (2us/div):



2.4 *Power Up Sequencing Change*

Delay sequences were modified to guarantee the SDRAM power up sequencing would operate properly.

Figure 6: Simulation vs. Layout (Removed Q8)



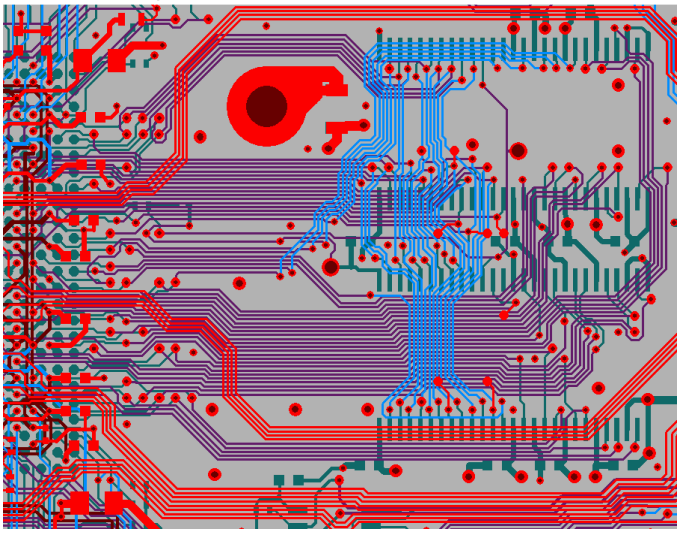
2.5 *SDRAM Routing Changes*

The Rev 02 board's main issue was with 132MHz spurious emissions, which is the frequency of the SDRAM. Testing showed some emissions coming from this area off the Xscale board. These traces were not routed as controlled impedance on Rev 02 and many traces were run on outside layers. Therefore, we modified this area to route these signals as controlled impedance, with traces on inner layers and copper poured on all surrounding layers.

Although the modified Rev 02 modules passed emissions tests with plenty of margin, having these traces routed as controlled impedance will be an improvement over the Rev 02 boards. Figure 7 shows a view of these traces with the copper pour removed.

Figure 7: Modified SDRAM Layout

Planes flooded on Layers 6, 4, 3, and 1
SDRAM Traces on Layer 5 (purple) and Layer 2 (blue)
Controlled impedance ~97 ohms

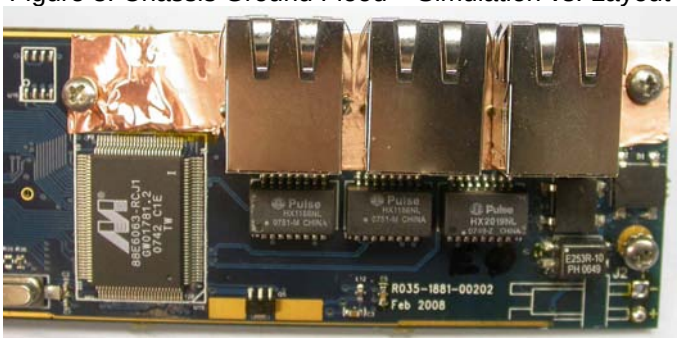


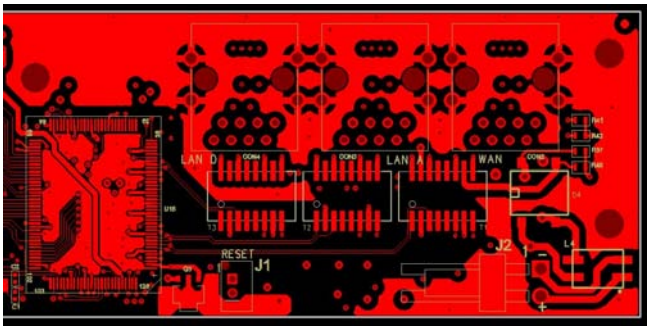
3 Personality Board Modifications

3.1 *Flood Chassis Ground Under RJ-45 Jacks*

In order to more closely model an interface panel and shield emissions from the Ethernet cables, chassis ground was flooded underneath RJ-45 jacks. This was simulated with copper tape on the Rev 02 boards.

Figure 8: Chassis Ground Flood – Simulation vs. Layout



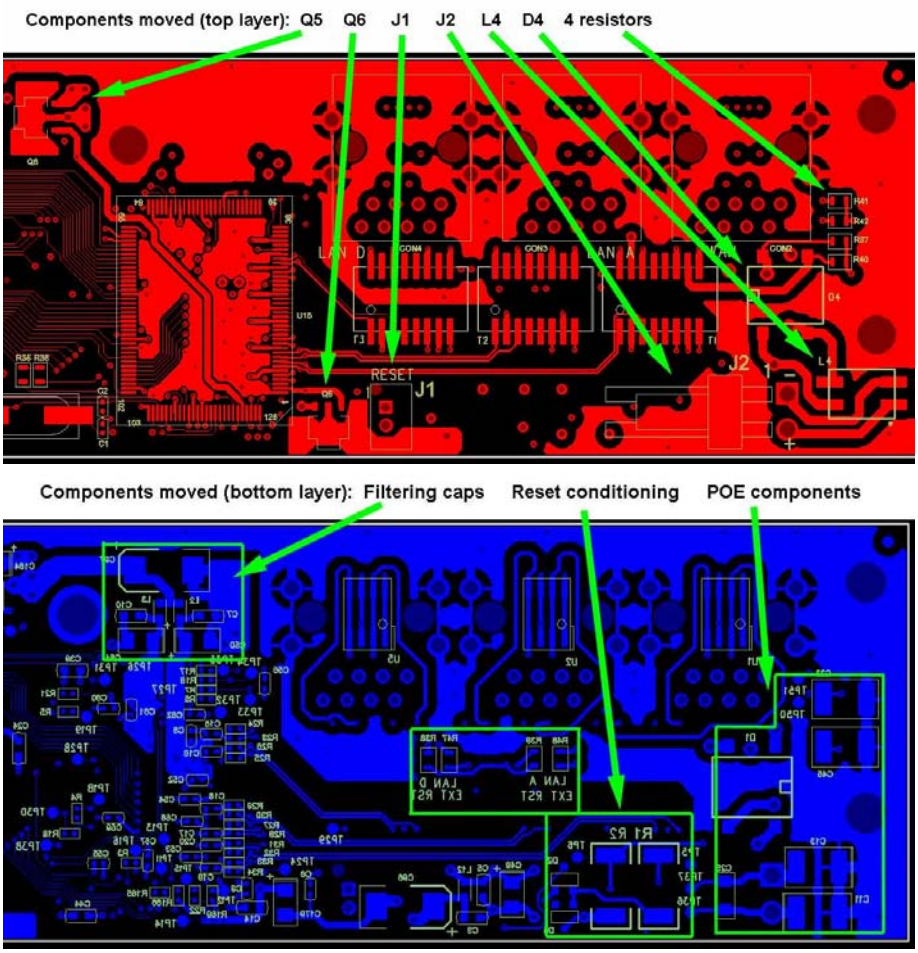


In order to pour copper completely to the center mounting hole, some components were shifted to the left. See Figure 9.

3.2 *Re-worked External Reset Circuitry*

Reset circuits were also moved in order to prevent long traces around the outside of the board that could potentially carry ESD voltages (induced onto the external cables). This should help guard against ESD if the external reset circuit is ever used. This change also required POE circuits to shift (these circuits are not used on iNode).

Figure 9: Shifted Components for Improved ESD

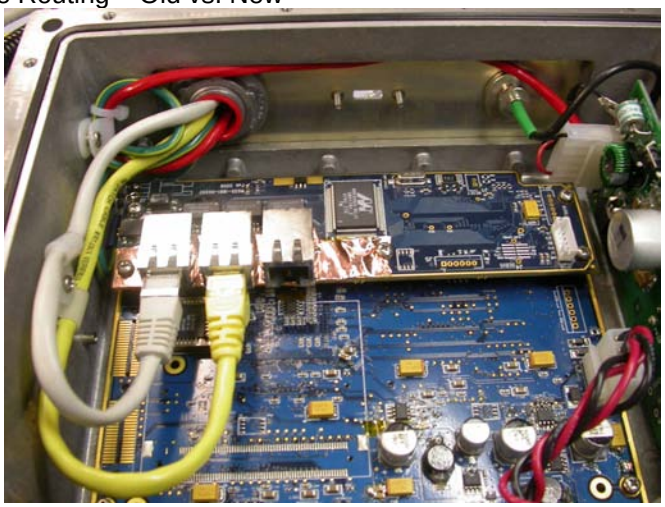


4 Assembly Modifications

4.1 *Routing Less Ethernet Inside of Case*

Much of the offending frequencies were found to be emitting from the Ethernet cables leaving the case. Minimizing the amount of cable inside the case helped.

Figure 10: Modified Cable Routing – Old vs. New



4.2 *Remove Paint Between Antenna Connector and Chassis*

Improve grounding bond between N connector and chassis. Production case will have this section masked, simulated by scraping paint off of this area. The figure shows a typical view, this masking is to be done on all antenna ports.

Figure 11: Masked Paint at Antenna Ports

4.3 *Improve Grounding Between Xscale and Personality Boards*

The initial design used plastic standoffs for two mounting holes, and connectors that were specified to 0.250" board stacking height. The actual connector, when assembled, measured around 0.262" between PCB surfaces. This forced the use of captive nylon washers between the metal standoff and PCB to prevent stressing the PCB.

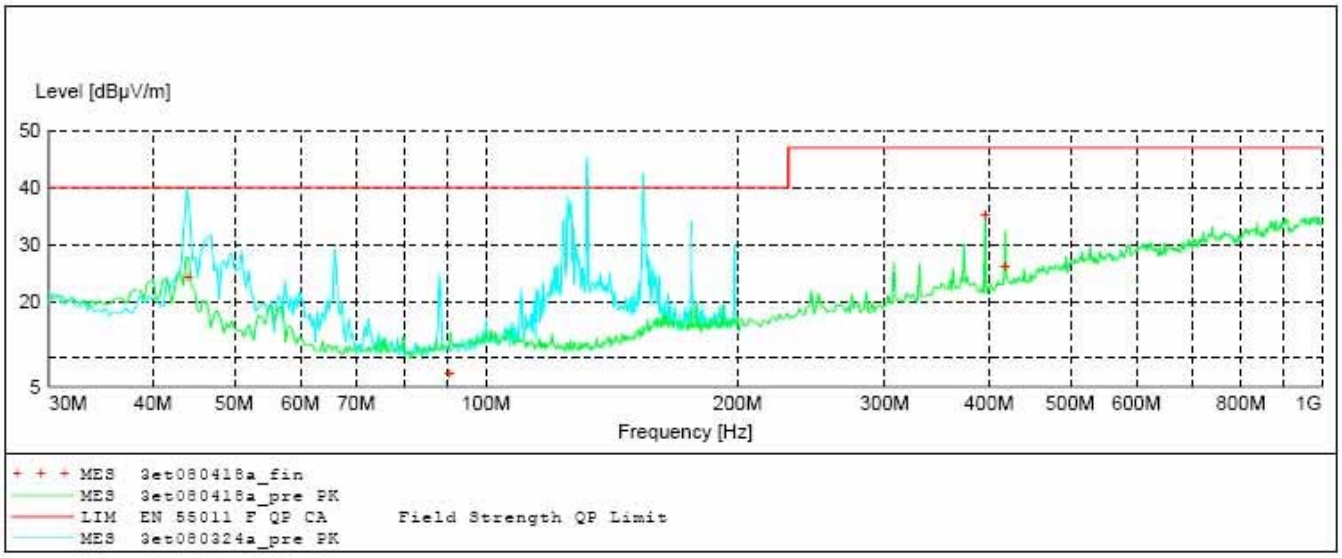
Rev 03 boards are using a different connector that allows for the 0.005" tolerance of the metal standoffs plus variances in solder paste thickness. Also, metal standoffs will be used for the two mounting holes that used the nylon standoffs on Rev 02 assemblies.

5 Testing Results

The modified Rev 02 boards were re-tested at the NCEE labs, and verified to pass the same tests that had been done on the original Rev 02 boards. The remainder of the tests were also run and found to be passing, including ESD, EFT, Radiated Immunity, other ETSI tests, etc. At the time this document was written, 3eTI had only verbal verification, formal documents are in process.

The only known failure of the unmodified Rev 02 boards was unintentional emissions <1GHz. The figure below is a clip from the laboratory printout showing the Rev 02 emissions before and after the modifications listed above.

Figure 12: FCC Scans – Before vs. After



We have every reason to believe that the Rev 03 boards will pass the same as the modified Rev 02 boards, as described above.