1. Processor and RS232:

ICI is a micro controller clocked with 7,3728 MHz, whose internal quarz osillater are driven in parallel resonance with Q1, C1 and C2, as well as R1 and R50.

The reset circuit of IC 10 resets the micro controller, after switching on the power supply. IC1 is driven with an external program storage of IC2. IC5 places the processor signals E and R/WB into the signals/OB and / WE around. If / OE=0, this recieves through the / CSROM of the selected storage program, program data from the processor over PF0.. PF7 and PB0.. PB7 of the chosen address. By means of JP1 and JP2, two different terminal assignments of IC2 can be chosen, 27C256 (EPROM) and 62256, static RAM. JP1 and JP2 are by default in the position 12 (EPROM) and after mounting, IC2 can no longer be altered.

By means of JP3, the boat mode is fixed. JP3 is open per default. This setting should not be altered.

By means of RN1, the level at the processor management PA1, RX, becomes TX. PA3PA0 and MODA weak potential, are put on High-Potential.

With SW1 and RN2, the logic levels of all eight PE - Port pins of IC1 can be put on any values.

IC11 serves the level change for the RS232-Interface. IC11 has integrated feed charges, with which standard levels are generated, at their disposal. The processor signals TX, RX, PA3 and PA0 are driven through IC11 or are received. PA0 receives the CTS signal PA3 sends the RTS while TX and RX guarantee the bidirectional communication.

The condensers C29.. C33, as well as C44, C58, C61 and C62 smooth the electricity on the Vcc-Pins through the integrated hookup situated on the circuit board.

2. Power supply and display elements:

The ARE 002 is provided through X5 with 24V DC. S11, together with D9, D11 L7 and F11 serves for the safeguarding of the supply entrance against surge over voltage, pole change, interferance voltage and sturgeon tension. Particularly C48, C60, L7 and F11 suppress sturgeon frequencies, that penetrate into the ARE 002 or that try to get out. The constant voltage regulators IC 9 and IC6, together with the supression elements C41, C59, C39 C42 R2, C37 and C40, regulate and provide the +12 V and +5 V for the reading appliance circuit.

Over X4, the Optic coupler O1 can be switched on by supplying a +24V DC current. By means of the parts D15, R14, R3 and C5 the level is changed via the X4 signal, to a Low pass filtered DC current, that is memorized in the Optic coupler entrance. The Open Collector Schmitt-Trigger exit of the Optic coupler O1 is in the resistance network RN3 terminated, with a pull up resistance and controls the micro controller entrance PA1, as well as the light diode driven by means of IC3A D1.

The signals of the serial interface are available at X3. All four data points RTS, TXD, CT and RXD are by means of the spools L8, L9, L10 and L12 protected against radiated interference from outside. If JP4 is closed, the RS232 hand shake hardware-wise is no longer carried out. In this case the ARE 002 can only execute communication with the Host over three wires.

Two seperate galvanic consumers can be connected at X2 to the ARE 002 hardware. The relais K1 and K2 act as turnkeys for closed and and open contacts ready. The switch condition of the two relais is steered by the processor signal PG0 and PG1 over IC3F and IC3E. Over D3 and D8, voltage peaks are destroyed, that are generated in the switch off moment of K1 and K2.

X1 is the Antenna port. The antenna is fed over the pins 2 and 4 with earth, and over pin 5 with switched 12 V DC. T3 is used for turning the antenna on and off. T3 is controlled over IC3D of the processor circuits of PG2. The antenna delivers the data signal, in which a higher carrier signal exists, and the Sync-Signal, that has the same phase as that of the carrier, are sent back to the ARE 002. Both signals are evaluated in the filter and synchronization step.

The light diodes D1, D2, D4, D5, D6, D12, D22, D23 and D24 serve the visual supervision of the processor signals of PG0.. PG2, PA1, PA3, PA6, RX, TX and the interference level detector around the comparator U6A.
The individual indications of the LEDs:

LED1:	Antenna on = reading process active, (solid-wired with ANT-PWR)
LED2:	last reading process NoRead, (solid-wired - functionality like QN1)
LED3:	last reading process successfull, (solid-wired - functionality like QR1)
LED4:	Status dig. Entrance (solid-wired)
LED5:	Error - at the moment only antenna mistakes (program-controlled)
LED6:	Opperating system and Life indication, blinks, (program-controlled)
LED7:	RxD (solid-wired)
LED8:	TxD (solid-wired)
LED9:	Interference levels (solid-wired)

3. Filter und Synchronisation:

The filter circuit of the ARE 002 consists of the 128 kHz-carrier frequence with the following steps with passive amplification and two identical consequence steps, that amplify every spectral component in the 64kHz-Frequency range for itself, but suppresses the 128kHz carrier signal.

Over C6 the antenna signal with stronger carrier component in the 64kHz-Bandpass with C7 and L1, and the 64kHz-Serial switching of C12, C13, and L2 are coupled with signal heightening. Additionally C12, L2 and C13 form a deep pass. The filtered signal at the beginning is coupled into U1 into the operation intensifier switched as Impedence converter over C14. R13, R20 and C21 generate a high frequency-free advance signal, that defiy through R22 the work point of U1. C15, together with R24 and R25, form a RC-Heigh pass filter with an Corner frequence of approximately 6.5kHz. The amplification of U1 becomes exclusive through the relationship.