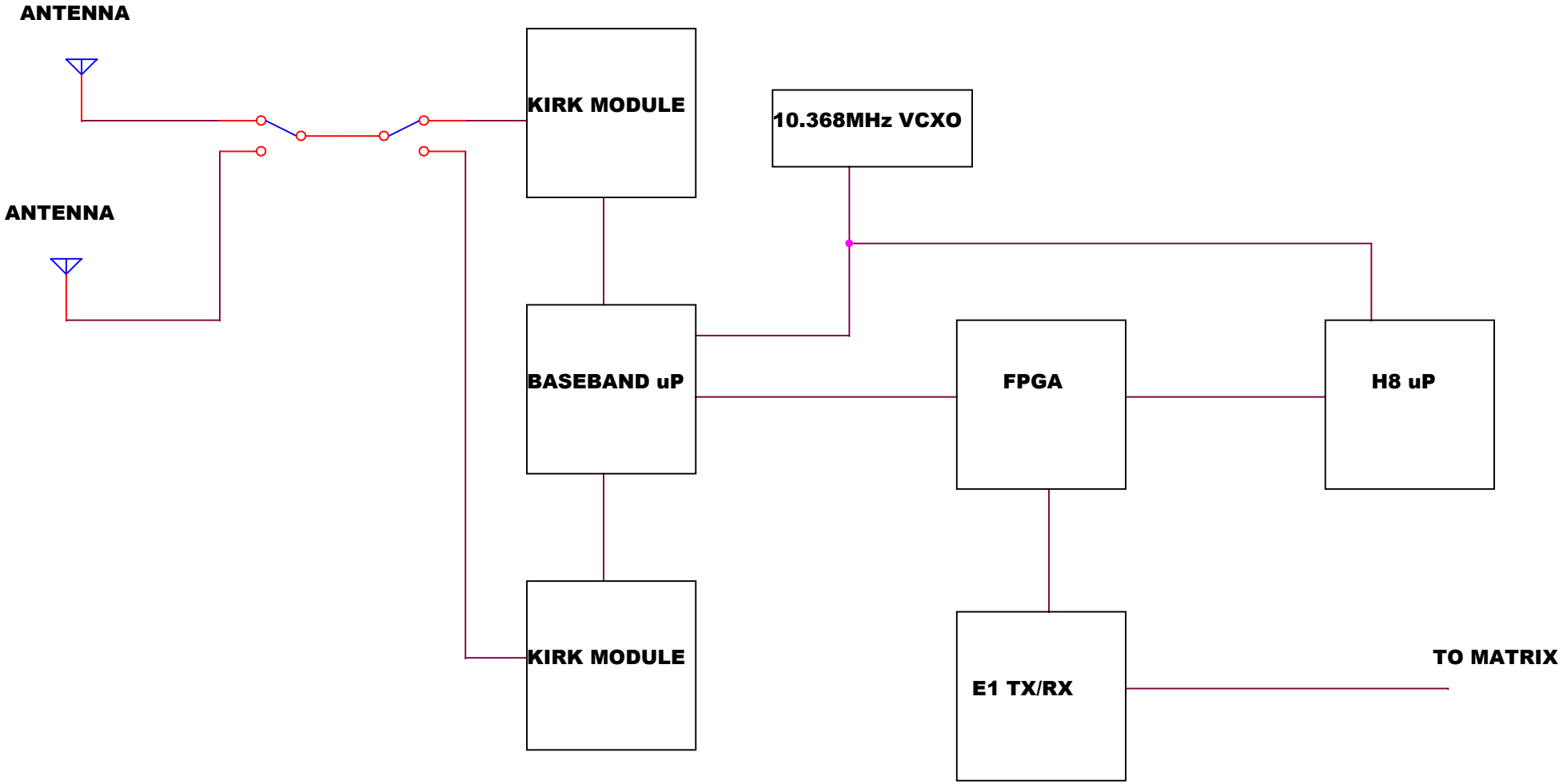
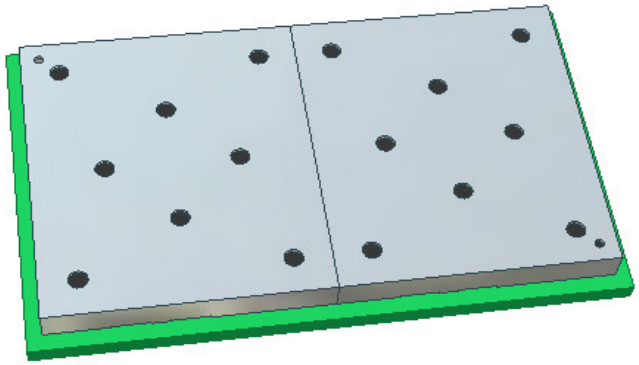
CEL-TA BLOCK DIAGRAM



The Kirk module is the DECT RF part which is controlled by a National SC14425 processor.
This synchronises the 10.368MHz crystal which is the main clock device used for driving the bus & audio codec.
It does this by using a 100Hz DECT sync waveform which is distributed centrally from the basestation via one of the unused pairs in the E1 cable.
The H8 processor handles the E1 communication with the basestation via a PCM4351 transceiver & communicates to the SC14425 through an interrupt
driven mailbox within a Xilinx FPGA.
The audio is passed from the E1 transceiver (PCM30) to a separate mailbox within the FPGA to the SC14425.

Product description
for
KRM1800 V2.0



1. Related Documents

Test specifications: K:\PROJEKTJOURNAL\KRM 1800 AVANTEC\Pre_spec\141008XX_QT_000.doc
Generisk testspecifikation**:** **G:\Arbejdsgrupper\HF_teknologi_gruppe\Generisk_test_spec\Dect1G8_001_QS.doc**

2. Introduction

KIRK Radio Modul

As a spin-off from our R&D efforts, we have created a new radio module for DECT. The module is intended for use in KIRK telecom products, but at the request of our business partners we now offer the module for sale.

The KIRK radio module (KRM) represents frontline technology, and is unique in several ways:

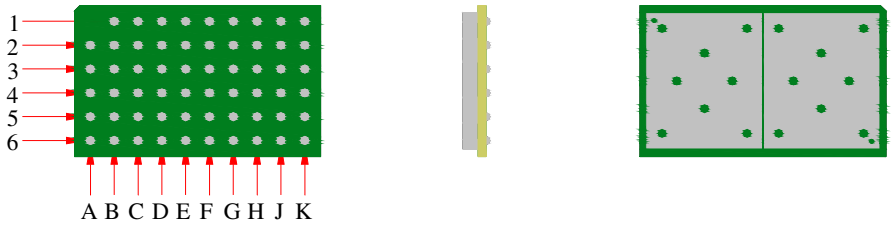
- They are smaller than any existing radio modules with the same facilities
- They have outstanding performance
- They are mounted with the use of Ball Grid Array technology
- They are priced lower than existing, larger and less performing modules

The DECT module comply with ETSI (ETS 300 175) requirements and meet the Generic Access Profile (GAP) requirements.
KRM 1800 V2 is based on DECT technology from National Semiconductor (NSC) and PA technology from MURATA.

3. Features

RF range	1870 – 1930 MHz
Radio receiver sensitivity	Typ.-95 dBm [BER 10-3]
Transmit Power (NTP)	Typ. 24 dBm (VCCLMX=2.6V, VCCPA=3.6V)
Power supply range	2.5-2.7V (VCCLMX), 3.24-4.50V (VCCPA)
Temp. range	0C to +40C
Reference clock freq.	10.368 MHz
Programming	NSC timing concept for LMX 4169

4. Pin connection



KRM 1800 V2.0

1D	RFPORT 1	5D	PAON (RESERVED PIN)
1J	VCCLMX	5E	VCCOPA
2H	PORT 0n	5F	OPAO
2J	PORT 0	5H	PORT 4
2K	RSSI	5J	RXDATA
3K	REFCLK	5K	CLOCK
4J	LE	6A	VCCPA
4K	DATA	6H	TXDATA
		6J	RST

ALL OTHER BGA: GND

5. Pin description

Detailed information about all Pin's except for the under need mentioned Pins see Data sheet for LMX4169 version 0.5
All pins are decoupled by 10 pF except for the RFPORT.

RFPORT

VCCLMX

VCCPA

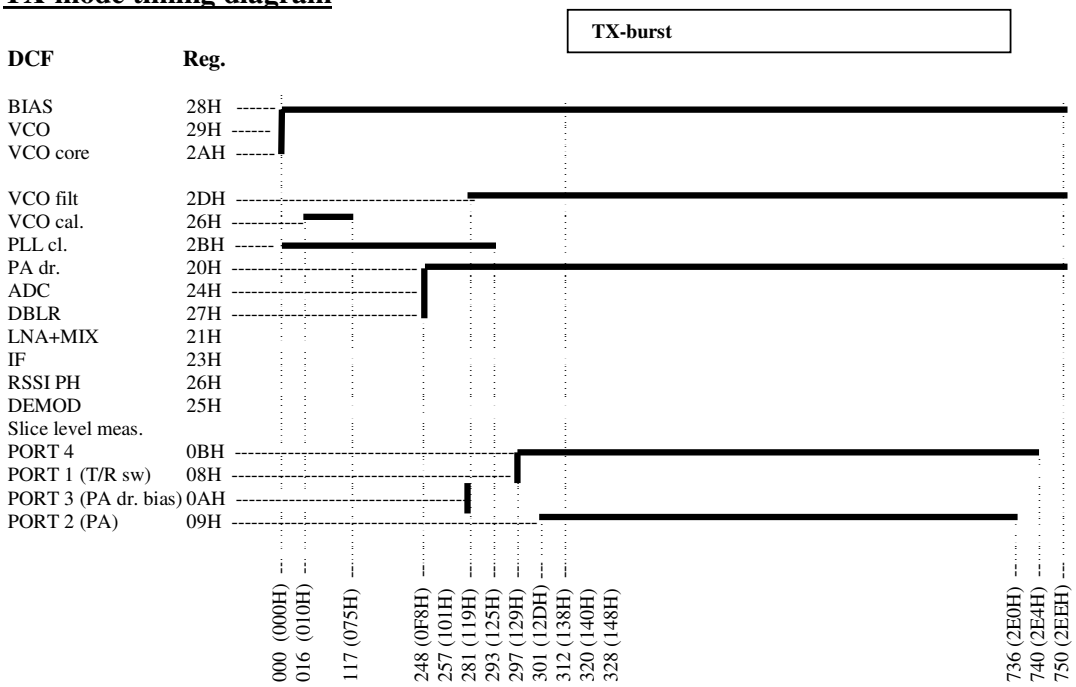
VCCOPA

OPA

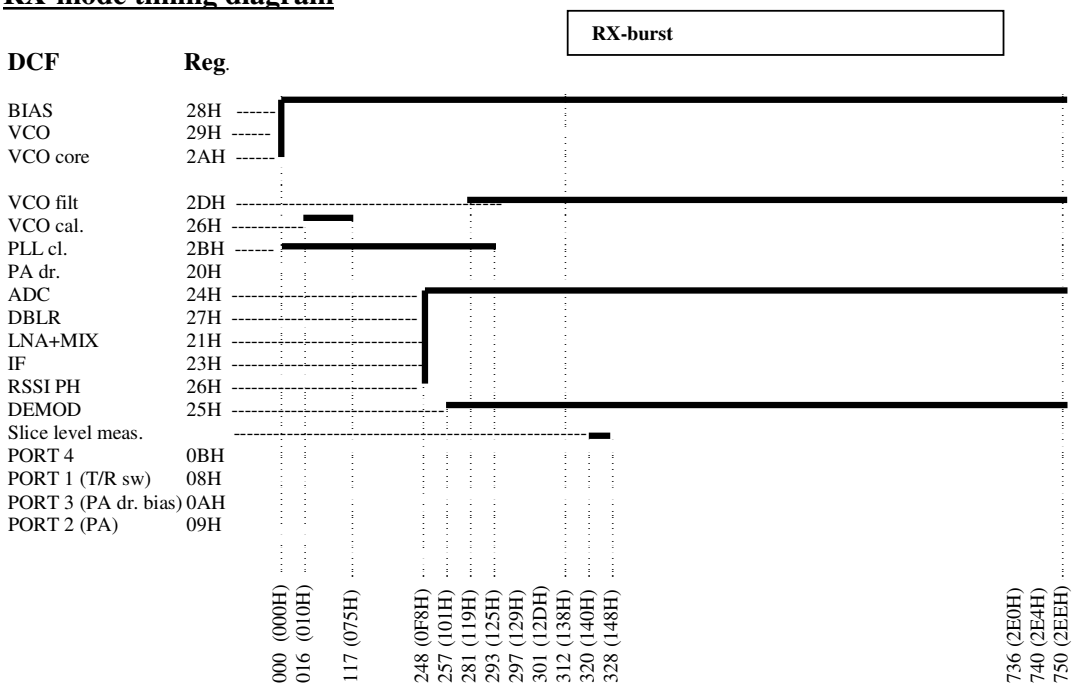
6. Programming description

In reference to the programming description in the datasheet version 0.50 for LMX4169 the following TX/RX timing is used to obtain the specifications for the module.

TX-mode timing diagram



RX-mode timing diagram



Register settings

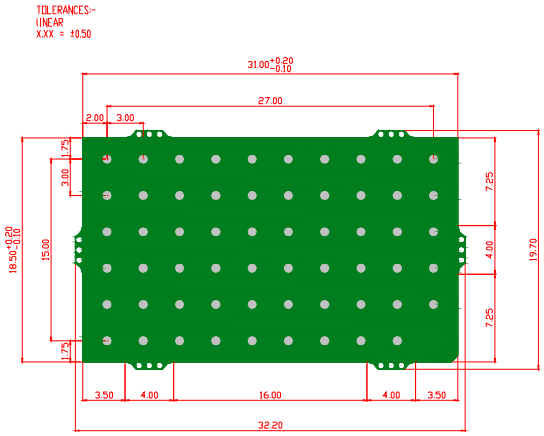
04 03 80	20 05 80	28 05 80	30 20 18	38 00 03	**Calibration**
08 13 33	21 05 80	29 05 80	31 06 0F	39 00 3F	28 05 80
09 12 35	22 00 00	2A 05 80	32 00 28	3A 00 00	12 35 0A
0A 13 21	23 05 80	2B 0B 40	33 00 13	3B 3F C0	04 72 00
0B 13 33	24 05 80	2C 00 10	34 03 FE	3C 3E 20	03 00 00
10 5B 1F	25 05 89	2D 05 A1	35 73 1A	3D 00 20	04 00 00
11 5B 1F	26 05 80	2E 00 00	36 00 38	3E FF E1	**Search mode**
12 5B 1F	27 05 80		37 E3 B0		05 77 D0

Alternating bit before preample: 7E5AAAAAAAAAAAA

Remarks:

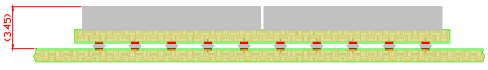
1. FAD is not active (port 0/0n forced to “high”).
2. LNAW is not active. LNA gain is set to fixed gain (max. =FH).
3. VCO, VCO core and BIAS is enabled all the time. If the these reg. is controlled by DSF the freq. Drift will rise to about –30 kHz/slot.
4. Alternating bit before preample is used. If not the freq. offset vil rise to about –30 kHz .

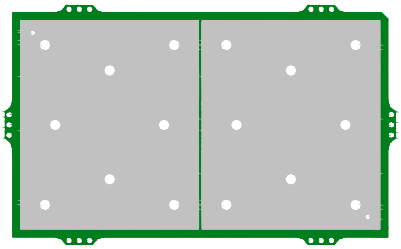
7. Mechanical dimensions



Side view before reflow

Side view after reflow

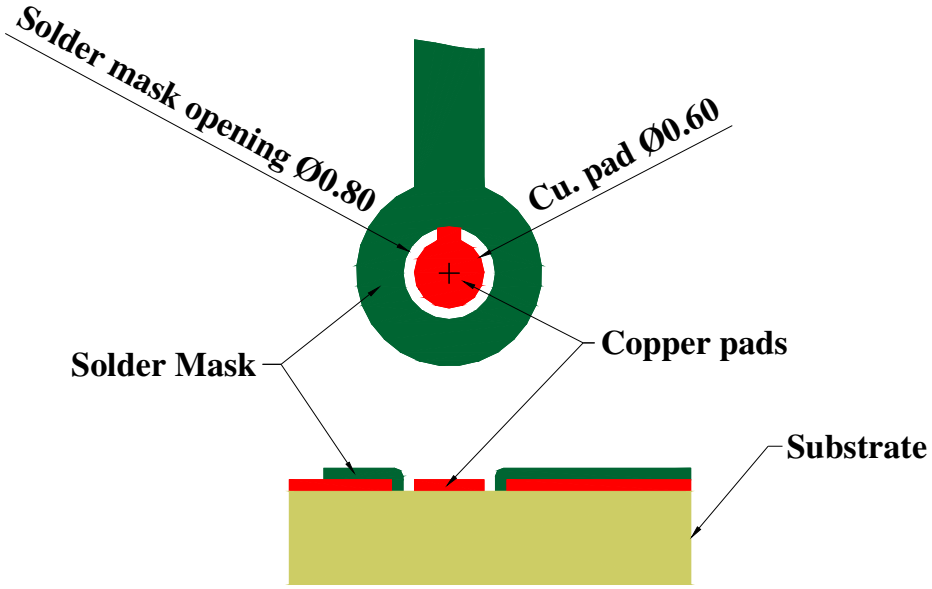




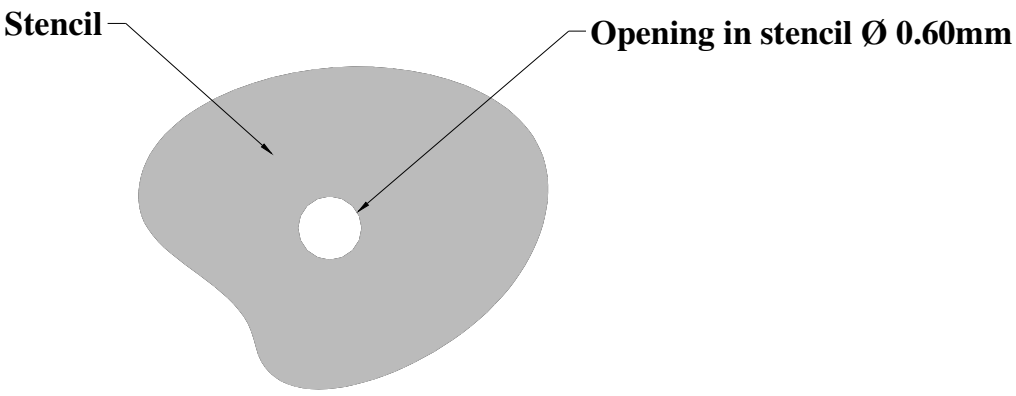
8. PCB integration

The following recommendations is given for the integration on the main PCB.

8.1. Recommended copper pad and solder mask opening (NSMD)



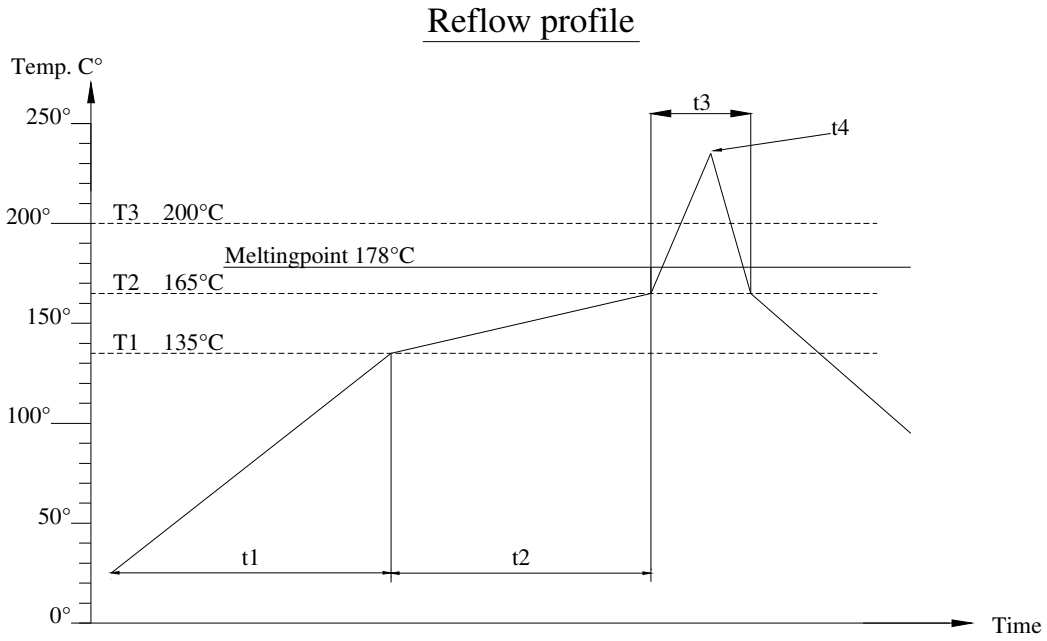
8.2. Recommended stencil design (stencil thickness 0.120 – 0.150 mm)



8.3. Solder ball alloy composition and flux type

Solder alloy	**SN**	**62%**
	Pb	**36%**
	Ag	**2%**
Melting temperature	**178-192°C**	
Flux Composition	**RO**	**J-STD-004-3.2.2**
Flux activity	**RMA**	

8.4. Recommended reflow profile



t1: Max. Change in temperature 4°C/second
t2: Time in preheat (135°C < temp. < 165°C) 60 - 150 second
t3: Time in reflow zone (temp. > 200°C) 30 - 120 second
t4: Peak temperature max. 235°C

T1 Preheat zone bottom 135°C
T2 Preheat zone top 165°C
T3 Reflow zone 200°C

9. Revisions historie

Rev.	Dato	Init	Staus	Decription
0.0	2004-01-27	HBR	closed	Preliminary draft
0.1	2004-02-24	HBR	closed	SW and mechanical update