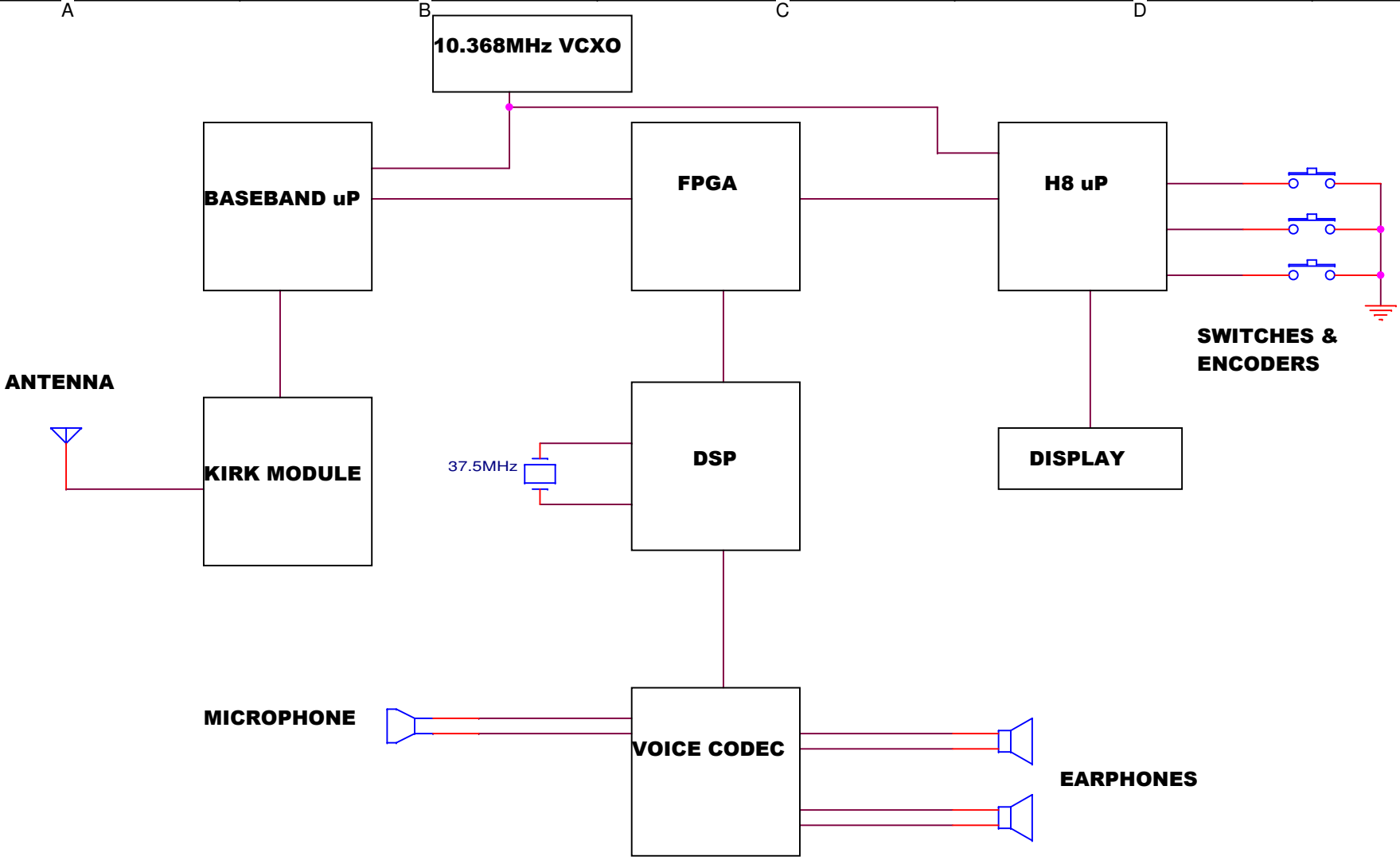

The Kirk module is the DECT RF part which is controlled by a National SC14425 processor.
This synchronises the 10.368MHz crystal which is the main clock device used for driving the bus & audio codec.
The H8 processor handles the local i/o (switches & display) functions & communicates to the SC14425 through an interrupt driven mailbox within a Xilinx FPGA.
The audio is passed from the SC14425 (8 bit parallel) to a separate mailbox within the FPGA to an AD2185 DSP (PCM30) which handles G722 compression/decompression & passes the audio data back to the FPGA where it it configured into a serial datastream suitable for the audio codec sampling at 16KHz.

CEL-BP BLOCK DIAGRAM