ISSUE	DESCRIPTION OF CHANGES	DATE
O	Initial Release	8th April 2013

Table of Contents

1.0 DESCRIPTION AND APPLICATION

1.1 DESCRIPTION

AT357 module is based on the Ember EM357 ZigBee compliant SOC IC. The IC is a 2.4GHz, IEEE 802.15.4 compliant transceiver, 32-bit ARM® Cortex™-M3 microprocessor, 192 KB of embedded flash and 12 KB of integrated RAM memory. The module is 17.9mm x 24.9mm x 2.75mm in dimensions with 51 I/O edge castellated interconnect.

1.2 APPLICATION

The custom module support user-defined applications, peripherals include UART, SPI, TWI, ADC and general-purpose timers, as well as up to 24 GPIOs. The target applications include Smart Energy, Building automation and control, Home automation and control, Security and monitoring and General ZigBee wireless sensor networking.

1.3 Module Block Diagram

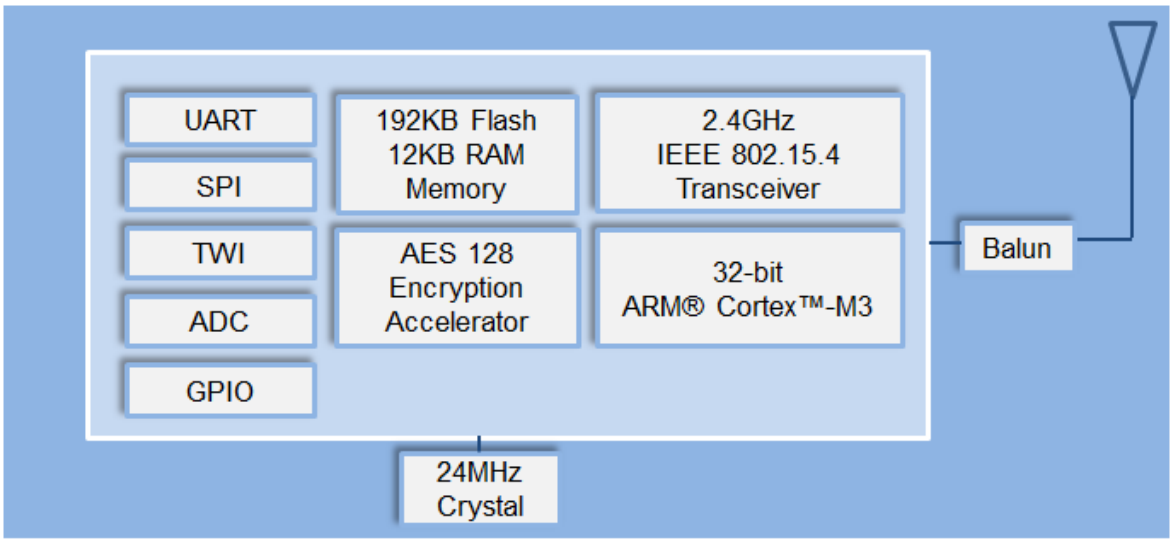


Figure 1: Module Block Diagram

2.0 MECHANICAL SPECIFICATIONS

2.1 Module Dimensions (mm)

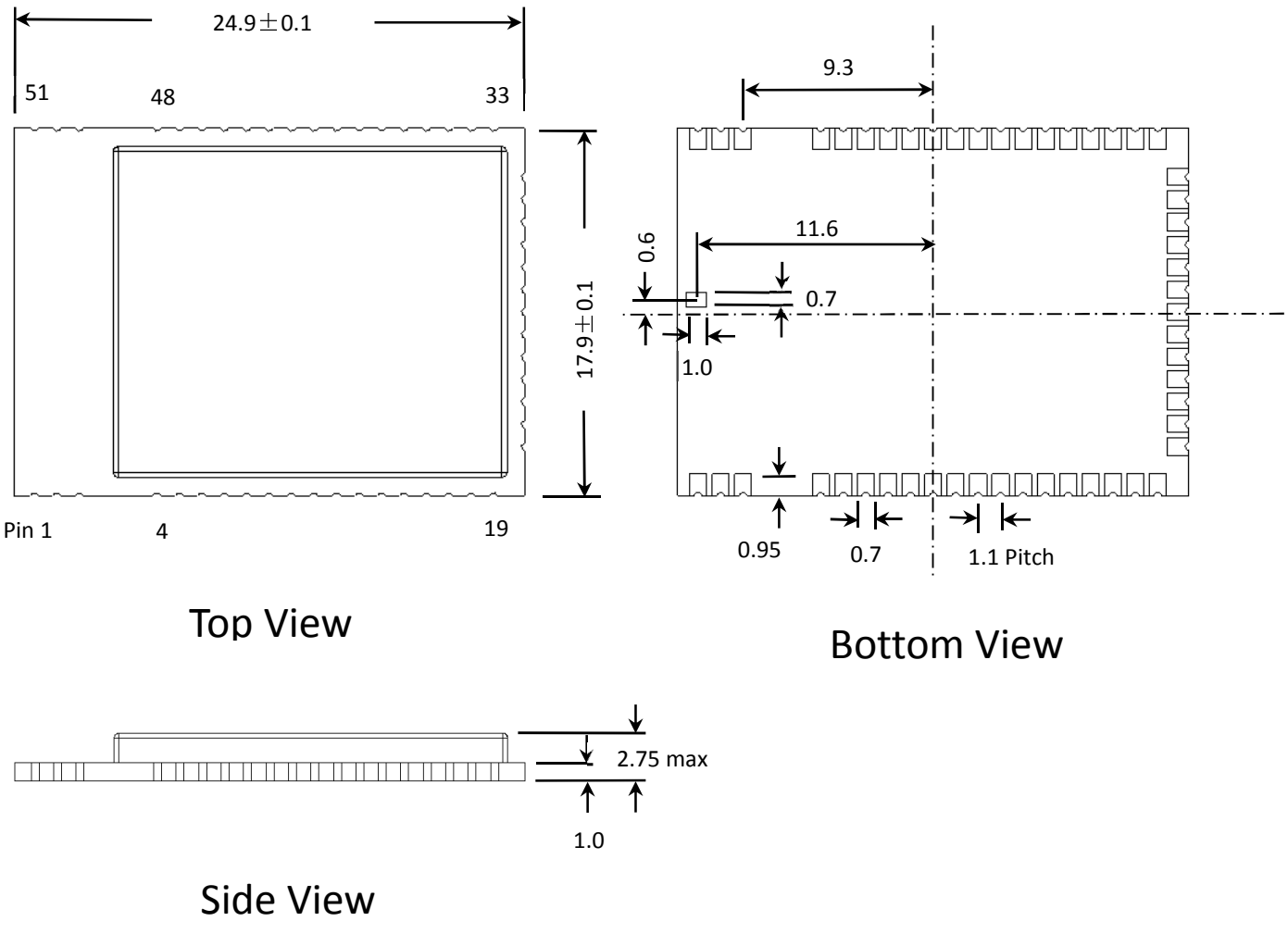


Figure 2: Module Top, Bottom and Side View

2.2 Module Footprint – Top "see through" View (mm)

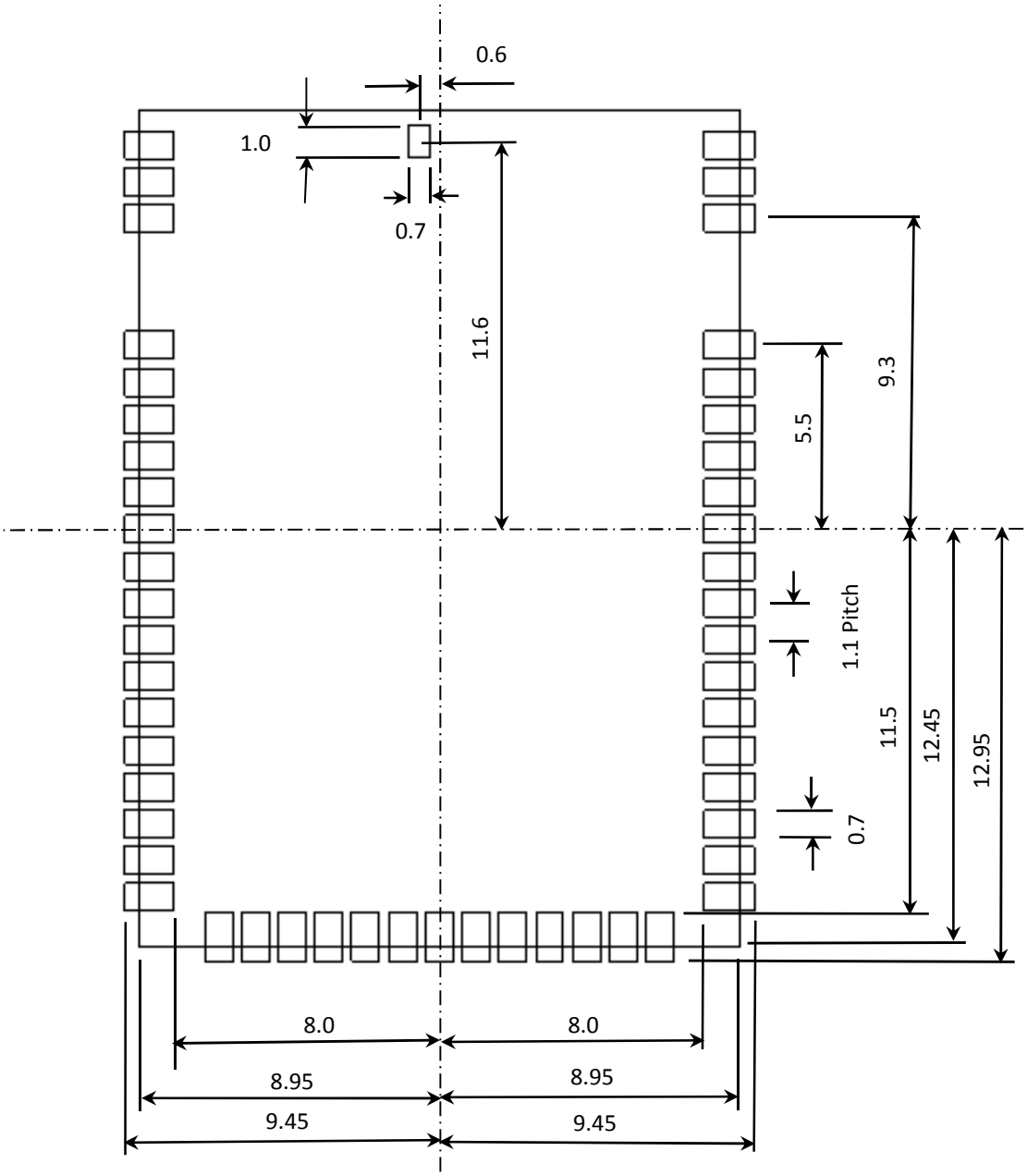


Figure 3: Module Footprint

2.3 Recommended Main PCB Copper Ground Design

(Only applicable to module with internal antenna)

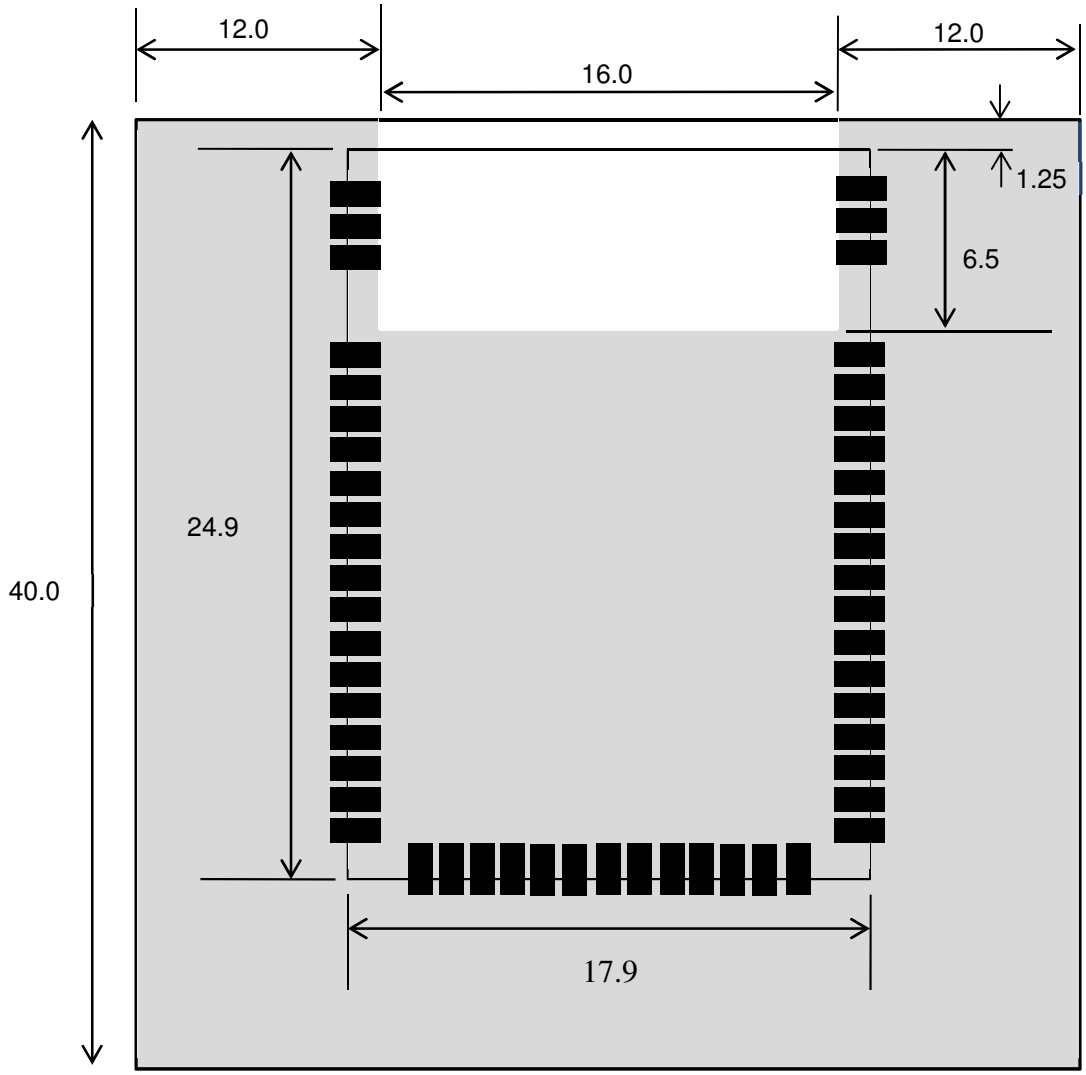


Figure 4: Recommended main PCB Copper design

2.4 Module Pin-Out

Module Pin Number	EM357 IC Pin Number	Name	Type	Description
1	49	GND	GND	Ground
2	49	GND	GND	Ground
3	49	GND	GND	Ground
4	49	GND	GND	Ground
5	49	GND	GND	Ground
6	49	GND	GND	Ground
7	49	GND	GND	Ground
8	49	GND	GND	Ground
9	11	PC5	I/O	Digital I/O
10	12	NRESET	I/O	Active low chip reset (internal pull-up on EM357)
11	13	PC6	I/O	Digital I/O
				OSC32B - 32.768KHz crystal oscillator
				nTX_ACTIVE - Inverted TX_ACTIVE signal
12	14	PC7	I/O	Digital I/O
				OSC32A - 32.768KHz crystal oscillator
				OSC32_EXT - Digital 32.768KHz clock input source
13	18	PA7	I/O	Digital I/O
				TIM1C4 - Timer 1 Channel 4 output
				TIM1C4 - Timer 1 Channel 4 input
				REG_EN - External regulator open drain output
14	19	PB3	I/O	Digital I/O
				TIM2C3 - Timer 2 channel 3 output
				TIM2C3 - Timer 2 channel 3 input
				SC1nCTS - UART CTS handshake of serial controller 1
				SC1nCTS - SPI master/slave clock of serial controller 1
15	20	PB4	I/O	Digital I/O
				TIM2C4 - Timer 2 channel 4 output
				TIM2C4 - Timer 2 channel 4 input
				SC1nRTS - UART RTS handshake of serial controller 1
				SC1nSSEL - SPI slave select of serial controller 1
16	21	PA0	I/O	Digital I/O
				TIM2C1 - Timer 2 channel 1 output
				TIM2C1 - Timer 2 channel 1 input
				SC2MOSI - SPI master data out of serial controller 2
				SC2MOSI - SPI slave data in of serial controller 2
17	22	PA1	I/O	Digital I/O

				TIM2C3 - Timer 2 channel 3 output
				TIM2C3 - Timer 2 channel 3 input
				SC2MISO - SPI slave data out of serial controller 2
				SC2MISO - SPI master data in of serial controller 2
18	24	PA2	I/O	Digital I/O
				TIM2C4 - Timer 2 channel 4 output
				TIM2C4 - Timer 2 channel 4 input
				SC2SCL - TWI clock of serial controller 2
				SC2SCL -SPI master/slave clock of serial controller 2
19	49	GND	GND	Ground
20	49	GND	GND	Ground
21	25	PA3	I/O	Digital I/O
				SC2nSSEL - SPI slave select of serial controller 2
				TRACECLK - Synchronous CPU trace clock
				TIM2C2 - Timer 2 channel 2 output
				TIM2C2 - Timer 2 channel 2 input
22	26	PA4	I/O	Digital I/O
				ADC4 - ADC Input 4
				PTI_EN - Frame signal of packet Trace Interface (PTI)
				TRACEDATA2 - Synchronous CPU trace data bit 2
23	27	PA5	I/O	Digital I/O
				ADC5 - ADC Input 5
				PTI_DATA - Data signal of Packet Trace Interface (PTI)
				nBOOTMODE - Embedded serial bootloader activation out of reset
				TRACEDATA3 - Synchronous CPU trace data bit 3
24	29	PA6	I/O	Digital I/O
				TIM1C3 - Timer 1 channel 3 output
				TIM1C3 - Timer 1 channel 3 input
25	30	PB1	I/O	Digital I/O
				SC1MISO - SPI master/slave data out of serial controller 1
				SC1SDA - TWI data of serial controller 1
				SC1TXD - UART transmit data of serial controller 1
				TIM2C1 - Timer 2 channel 1 output
				TIM2C1 - Timer 2 channel 1 input
26	31	PB2	I/O	Digital I/O
				SC1MISO - SPI master/slave data in of serial controller 1
				SC1SCL - TWI clock of serial controller 1
				SC1RXD - UART receive data of serial controller 1
				TIM2C2 - Timer 2 channel 2 output
				TIM2C2 - Timer 2 channel 2 input

27	32	JCLK	I	JTAG clock input from debugger
				SWCLK - Serial Wire clock input/output with debugger
28	33	PC2	I/O	Digital I/O
				JTDO - JTAG data out to debugger
				SWO - Serial Wire Output asynchronous trace output to debugger
29	34	PC3	I/O	Digital I/O
				JTDI - JTAG data in from debugger
30	35	PC4	I/O	Digital I/O
				JTMS - JTAG mode select from debugger
				SWDIO - Serial Wire bidirectional data to/from debugger
31	36	PB0	I/O	Digital I/O
				VREF - ADC reference output
				VREF - ADC reference input
				IRQA - External interrupt source A
				TRACECLK - Synchronous CPU trace clock
				TIM1CLK - Timer 1 external clock input
				TIM2MSK - Timer 2 external clock mask input
32	49	GND	GND	Ground
33	49	GND	GND	Ground
34	16,23,28,37	VDD	Power	2.1 to 3.6V Module power domain
35	49	GND	GND	Ground
36	38	PC1	I/O	Digital I/O
				ADC3 - ADC Input 3
				SWO - Serial Wire Output asynchronous trace output to debugger
				TRACEDATA0 - Synchronous CPU trace data bit 0
37	40	PC0	I/O	Digital I/O
				JRST - JTAG reset input from debugger
				IRQD - Default external interrupt source D
				TRACEDATA1 - Synchronous CPU trace data bit 1
38	41	PB7	I/O	Digital I/O
				ADC2 - ADC Input 2
				IRQC - Default external interrupt source C
				TIM1C2 - Timer 1 channel 2 output
				TIM1C2 - Timer 1 channel 2 input
39	42	PB6	I/O	Digital I/O
				ADC1 - ADC Input 1
				IRQB - External interrupt source B
				TIM1C1 - Timer 1 channel 1 output
				TIM1C1 - Timer 1 channel 1 input

40	43	PB5	I/O	Digital I/O ADC0 - ADC Input 0 TIM2CLK - Timer 2 external clock input TIM1MSK - Timer 1 external clock mask input
41	49	GND	GND	Ground
42	49	GND	GND	Ground
43	49	GND	GND	Ground
44	49	GND	GND	Ground
45	49	GND	GND	Ground
46	49	GND	GND	Ground
47	49	GND	GND	Ground
48	49	GND	GND	Ground
49	49	GND	GND	Ground
50	49	GND	GND	Ground
51	49	GND	GND	Ground
52	-	LGA pad	RF	TX/Rx Antenna connection. Not applicable to UFL and internal Chip antenna option

Table 1: Module Signal Description

Notes:

(1) The serial UART connections TXD, RXD, CTS and RTS are PB1, PB2, PB3 and PB4 respectively.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Power Supply Voltage (VDD)	-0.3	+3.6	V
Voltage on any IO	-0.3	VDD+0.3	V
Voltage on any Pad pin (PA4, PA5, PB5, PB6, PB7, PC1), when used as an input to the general purpose ADC	-0.3	2.0	V
RF Input Power		+15	dBm
Storage temperature	-40	85	℃

Table 2: Absolute Maximum Ratings

3.2 Environmental Characteristics

PARAMETER	MIN	MAX	UNIT
ESD on any pad (human body model)		±2	kV
ESD on non-RF pads (charged device model)		±400	V
ESD on RF terminal (charged device model)		±225	V
Moisture Sensitivity Level		3	

Table 3: Environment Characteristics

3.3 Operating Conditions

PARAMETER	MIN	TYP	MAX	Unit
Power supply	2.1	3.0	3.6	V
Operating Temperature	-40	25	85	℃

Table 4: Operating Conditions

3.4 DC characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive Mode	VDD = 3.0V, TA = 25 ℃, total Rx current		24.0		mA
Transmit Mode	VDD = 3.0V, TA = 25 ℃, power setting (+3 dBm)		32		mA
Receive Mode (Boost mode)	VDD = 3.0V, TA = 25 ℃, boost mode total Rx current		25.5		mA
Transmit Mode (Boost mode)	VDD = 3.0V, TA = 25 ℃, max power setting (+8 dBm)		43		mA
Sleep Mode	VDD = 3.0V, TA = 25 ℃, including Internal RC oscillator		0.7		uA

Table 5: DC characteristics

3.5 RF Characteristics

(VDD = 3V, TA = 25°C, Boost Mode measured at the U.FL connector with 50Ω termination)

PARAMETER (Receive Section)	MIN	TYP	MAX	UNIT
Frequency range	2400		2500	MHz
Sensitivity (boost mode)		-102	-96	dBm
Sensitivity		-100	-94	dBm
Maximum input signal level for correct operation	0			dBm
High-Side Adjacent Channel Rejection		37		dB
Low-Side Adjacent Channel Rejection		42		dB
2nd High-Side Adjacent Channel Rejection		53		dB
2nd Low-Side Adjacent Channel Rejection		50		dB
Co-channel rejection		-6		dBc
Spurious emission 30 ~ 1000MHz 1 ~ 12.75GHz		 -77 -76		 dBm dBm

Table 6: Rx Characteristics

PARAMETER (Transmit Section)	MIN	TYP	MAX	UNIT
Maximum output power (boost mode)		7.9		dBm
Maximum output power	0	4.0		dBm
Error vector magnitude (Offset-EVM)		5	15	%
Carrier frequency error	-40		+40	ppm
PSD mask relative	-20			dB
PSD mask absolute	-30			dBm
2nd Harmonic		-54		dBm
3rd Harmonic		-53		dBm
Spurious emission (Max power modulated signal) 30 ~ 1000 MHz 1 ~ 2.5 GHz 2.5 ~ 12.7 GHz (outside restricted bands)		 -80 -67 -74		 dBm dBm dBm

Table 7: Tx Characteristics

3.6 Transmit Power Characteristics

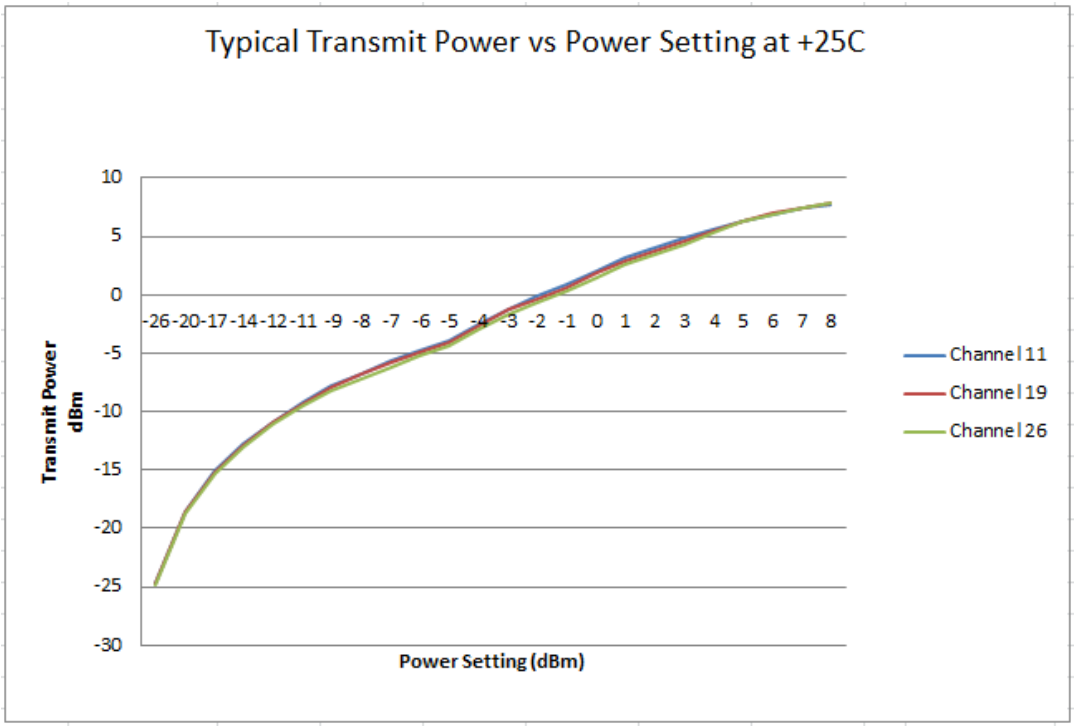


Figure 5: Transmit Power vs Power Setting

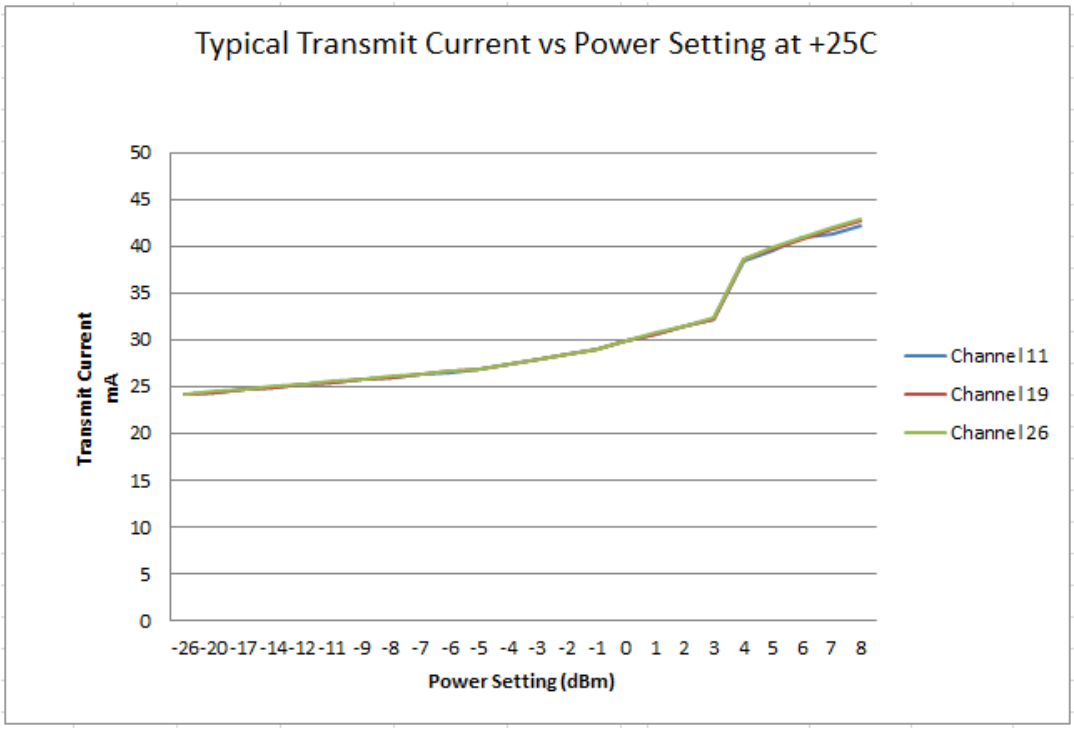


Figure 6: Transmit Current vs Power Setting

4.0 APPLICATION NOTES

4.1 Pin Assignments

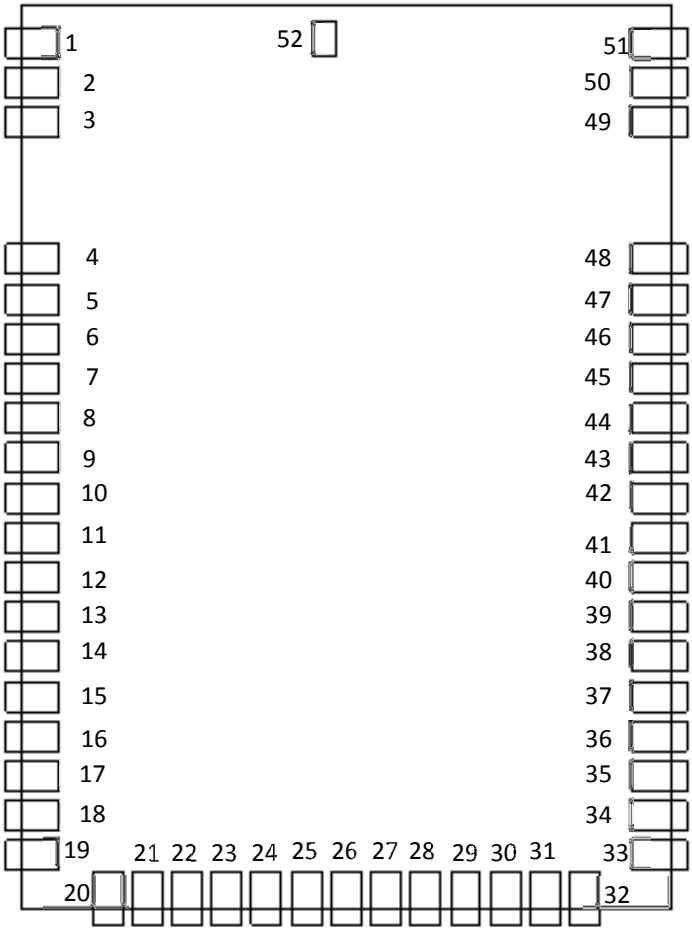


Figure 7. Pin Assignments

Refer to above chapter 2.4 for detailed pin functions.

4.2 Serial Communication

AT357 module provides several options for serial communications.

- *SPI (Serial Peripheral Interface)*

SPI(Slave) Pin	Module Pin Number	GPIO Port
SC2MOSI	16	PA0
SC2MISO	17	PA1
SC2SCKL	18	PA2
SC2nSSEL	21	PA3

Table 8: SPI Pins

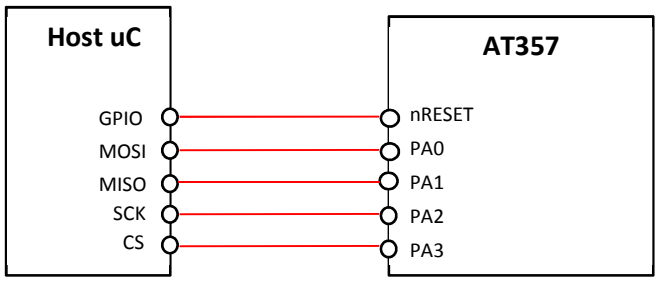


Figure 8a. Host uC to AT357 module via SPI Interface

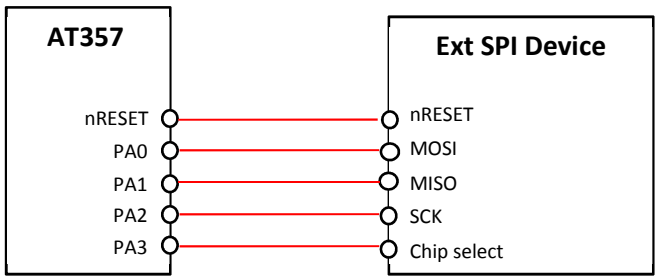


Figure 8b. AT357 module to external SPI device

- *UART (Universal Asynchronous Receiver/Transmitter)*

UART pin	Module Pin Number	GPIO Port
TXD	25	PB1
RXD	26	PB2
nCTS	14	PB3
nRTS	15	PB4

Table 9: UART Pins

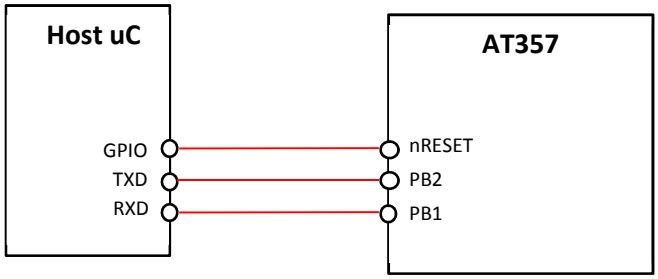


Figure 9a. Host uC to AT357 module via UART Interface

AT357 module can interface UART to external serial device (for example RS-232) through a level shifter (SP3232EBCN from Sipex).

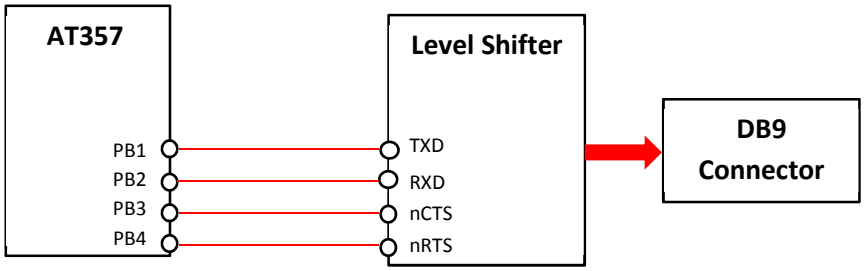


Figure 9b. AT357 module to external UART device

- *TWI (Two Wire Serial Interface)*

TWI pin	Module Pin Number	GPIO Port
SC2SDA (open drain)	17	PA1
SC2SCL (open drain)	18	PA2

Table 10: TWI Pins

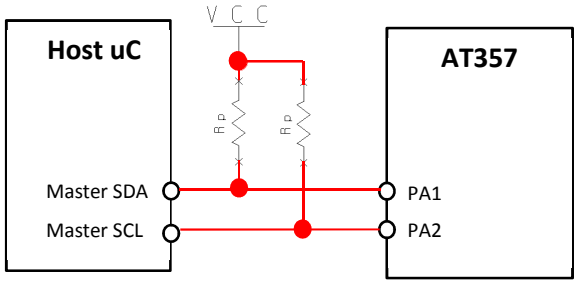


Figure 10a. Host uC to AT357 module via I2C Interface

AT357 can support external I2C devices such as sensor board to provide wireless sensing application.

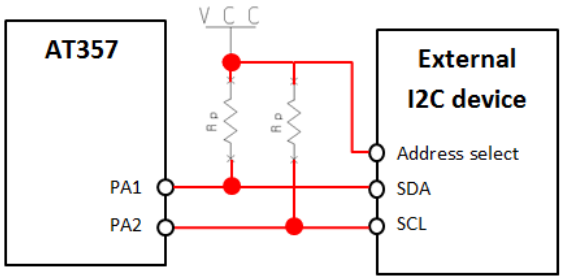


Figure 10b. AT357 module to external I2C device

4.3 Power Supply Design

Excessive noise or ripple (from switching DC-DC regulator) which is decoupled into power supply pin will lead to severe radio performance degradation. Therefore, it's a must to implement proper power supply decoupling circuits in order to sharply suppress any undesired noise.

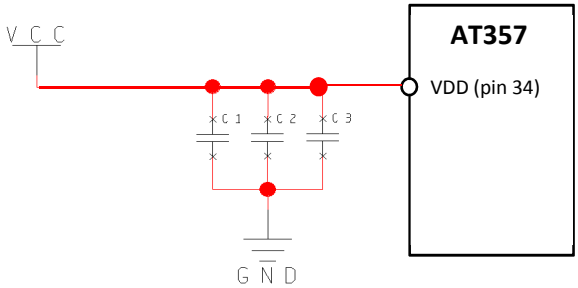


Figure 11. Power supply decoupling circuits

The decoupling capacitors can be in value of 10uF, 1uF and 10pF. The placement of three decoupling capacitor must be in the following order: 10uF (C1), 1uF (C2) and followed by 10pF (C3) which is closer to power supply pin.

4.4 External Flash Memory

The AT357 can support bootloader feature that allows a node to update its image on demand, either by serial communication or over the air (OTA). The boot loading program is stored in external flash memory (for example AT45DB021D from ATMEL) which is accessible using SPI communication (refer to Figure 8b for signal connection).

4.5 ADC

The AT357 has offered 24 multi-purpose GPIO ports. Six of them may be individually configured as ADC input.

Analog Signal Pin	Module Pin Number	GPIO port
ADC0	40	PB5
ADC1	39	PB6
ADC2	38	PB7
ADC3	36	PC1
ADC4	22	PA4
ADC5	23	PA5

Table 11: ADC Pins

Refer to EM35x datasheet (120-035x-000M) for detailed configuration.

4.6 GPIO ports (default setting)

Below listed the default setting of all 24 multi-purpose GPIO ports.

Ports	Assignment	Logic Level	Peripheral
PA0	SPI bus		MOSI
PA1	SPI bus		MISO
PA2	SPI bus		SCLK
PA3	Digital out	Active Low	nSSEL (slave SPI only)
PA4	Digital out	Active High	
PA5	Digital input	Active Low	Bootloader
PA6	Digital out	Active Low	
PA7	Digital out	Active Low	
PB0	Digital out	Active High	
PB1	TxD		UART
PB2	RxD		UART
PB3	nCTS		UART
PB4	nRTS		UART
PB5	ADC Input	Analog	
PB6	Digital input	Active Low	
PB7	Digital out	Analog	
PC0	JTAG		nJRST
PC1	ADC Input	Analog	
PC2	JTAG		JTDO
PC3	JTAG		JTDI
PC4	JTAG		JTMS
PC5	Digital out	Active Low	
PC6	Digital input	Active Low	
PC7	Digital out	Active Low	

Table 12: GPIO Ports

5.0 ASSEMBLY INFORMATION

5.1 Lead-Free soldering reflow profile

Condition	Exposure
Average ramp-up rate (200°C to 250°C)	< 3 °C / second
> 217°C	60-120 seconds
Peak temperature	250 +0/-5°C
Time within 5°C of peak	20-30 seconds
Ramp-down rate (Peak to 50°C)	Less than 6°C / second

Table 13: Reflow Profile Recommendation

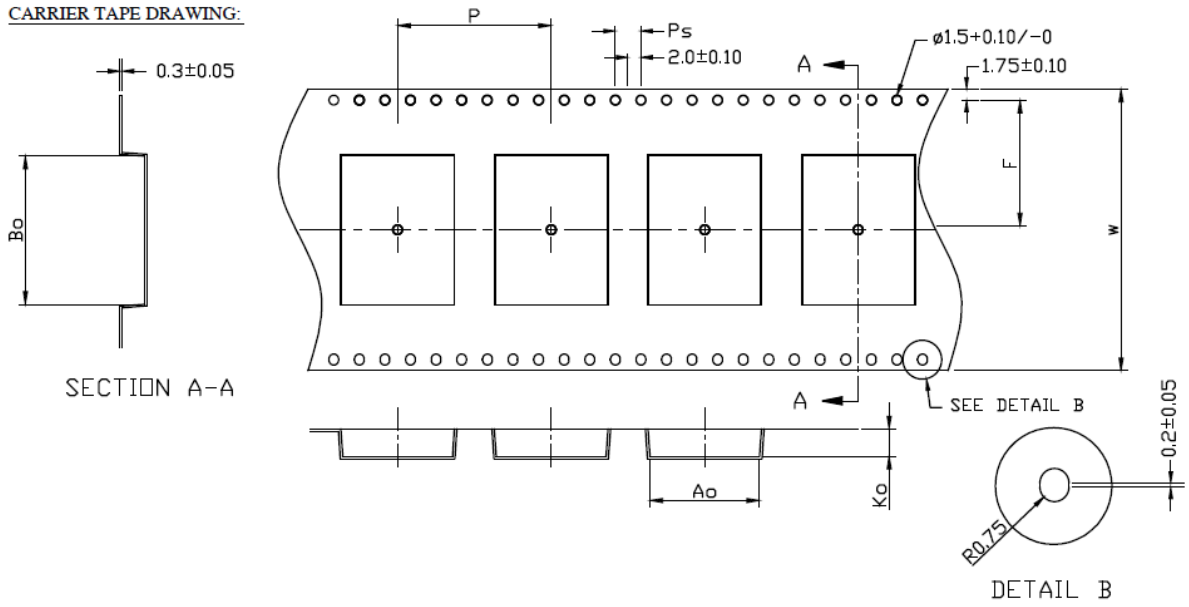
6.0 RELIABILITY TESTS

No.	Test item	Test condition
1	Reflow Thermal Cycle	Normal Pbfree reflow Condition 2 times
2	Thermal Shock Cycle	30min. at -40°C, 30min. at 85°C , 100Cycles Recovery Time 1hours
3	Vibration Test	JESD22-B103-B Service Condition 5, 5Hz -> 500Hz, Acceleration 0.3g, 4min/Cycle. Total 4 cycles per axis
4	High Temperature Storage Test	96 hours at 85°C, Recovery Time 1hours
5	Low Temperature Storage Test	96 hours at -40°C, Recovery Time 1hours
6	High Temperature & Humidity Storage Test	96 hours at 60°C & 90%RH±2%RH. Recovery Time 1hours
7	Drop Test	Height min 76 ㎝, All sides onto metal plate

Table 14: Reliability Tests

7.0 PACKAGING INFORMATION

7.1 Tape and Reel specification

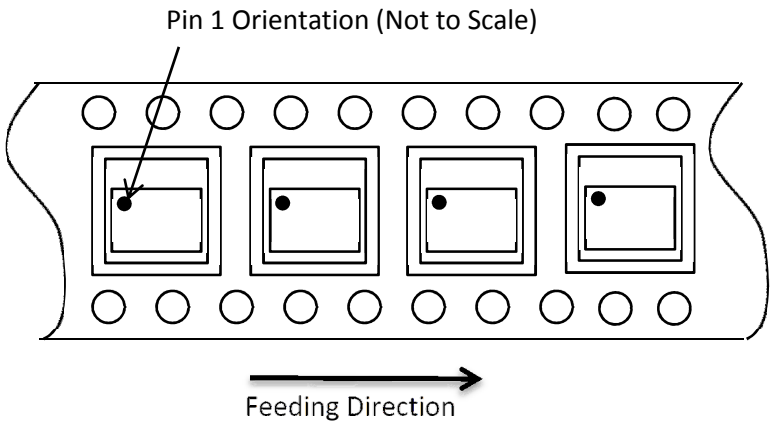


DIMENSIONS	W	P	Ao	A1	Bo	B1	Ko	K1	Ps	F
SPECS' Nominal	44.00	24.00	18.50	NA	25.50	NA	3.30	NA	4.00	20.20
Tolerance +/-	0.30	0.10	0.10	NA	0.10	NA	0.10	NA	0.10	0.10

All dimensions in mm

Figure 12: Tape Dimensions

7.2 Component Orientation



7.2.1 Tape Width: 44 mm
7.2.2 Tape Pitch (part to part): 24 mm
7.2.3 Reel Diameter: 330 mm

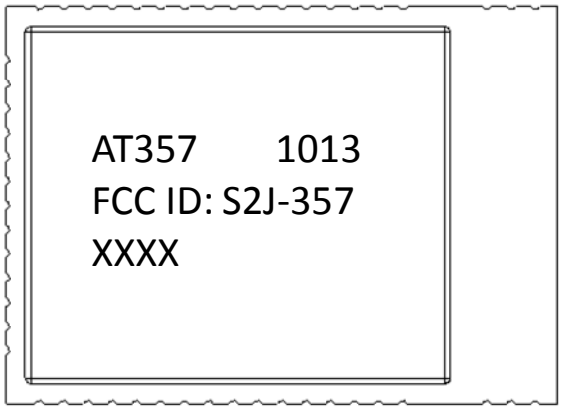
7.3 Module Marking

Legend:

AT357 - Module Model Number

1013 - Date Code (Example: 10-Workweek, 13-Year)

XXXX - Customer Program information



8.0 REGULATORY INFORMATION

8.1 FCC Notice

This module complies with Part 15 of the FCC rules and regulations. Compliance with the labeling requirements, FCC notice and antenna usage guideline is required. The OEM must comply with the following regulations:

1. The OEM integrator must ensure that the text on the external label provided with this device is placed on the outside of the final product.
2. AT357 module may only be used with antenna that have been tested and approved for use with this module.

FCC Caution: Any changes or modifications not expressly approval by the party responsible for compliance could void the user's authority to operate this device.

8.2 OEM Labeling Requirements

The Original Equipment Manufacturing (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the finished product specifying the AT357 FCC identifier (**FCC ID: S2J-357**).

Below FCC label statements are required for OEM products containing AT357 Module.

Contains FCC ID: S2J-357
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.

8.3 RF Exposure

This module has been certified for remote and base radio applications and is not intended to be operated within 20cm of the body. If the module will be used for portable applications, the OEM or OEM integrator is responsible for passing additional SAR (Specific Absorption Rate) testing in accordance with FCC Rules 2.1093.

The preceding statement must be included as a CAUTION statement in OEM product manuals in order to alert users of FCC RF exposure compliance.

To satisfy FCC RF exposure requirements, a separation distance of 20cm or more should be maintained between the antenna of this device and persons during device operation. To ensure compliance, operation at closer than this distance is not recommended. The antenna used for this transmitter must not be co-located or operating in conjunction with other antennas or transmitters.

8.4 FCC Approved Antenna

AT357 Module has been tested and approved for use with the following antenna:

- Dipole (2.5dBi, AAC part number A.01.120)

Table 15 shows approved channels of operations with the corresponding maximum output power steps settings.

	Channel 11-25	Channel 26
AT357	+8dBm	-5dBm

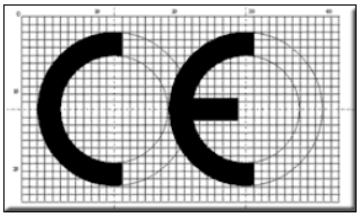
Table 15: Maximum Power Settings for FCC Compliance

8.5 CE Notice

The AT357 module has been tested and certified for use in the European Union.
If this module is to be incorporated into a product, the OEM must ensure compliance of the final product to the European Harmonized EMC and low voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. The final product must not exceed the specified power ratings, antenna specifications and installation requirements as specified in this user manual. If any of these specifications are exceeded in the final product then a submission must be made to a notified body for compliance testing to all of the required standards.

8.6 OEM Labeling Requirements

1. The CE conformity marking must consist of the initials CE taking the following form:



If the CE conformity marking is reduced or enlarged the proportions given in the above graduated drawing must be respected

2. Where the directive concerned does not impose specific dimensions, the CE marking must have a height of at least 5 mm.

3. The CE marking must be affixed to the product or to its data plate. However, where this is not possible or not warranted on account of the nature of the product, it must be affixed to the packaging, if any, and to the accompanying documents, where the directive concerned provides for such documents.

4. The CE marking must be affixed visibly, legibly and indelibly.

For more information please refer to http://ec.europa.eu/enterprise/faq/ce-mark.htm. Customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market.

8.7 CE Compliance Power Settings

The following antenna has been tested and approved for use with the AT357 Module:

- Dipole (2.5dBi, AAC part number A.01.120)

Table 16 shows approved channels of operations with the corresponding maximum output power steps settings.

	Channel 11-26
AT357	+8dBm

Table 16: Maximum Power Settings for Europe (ESTI)

9.0 RoHS Declaration

Based on our supplier declarations, this product does not contain substances that are banned by Directive 2002/95/EC or contains a maximum concentration of 0.1% or 1000 ppm by weight in homogeneous materials for:

- Lead and lead compounds
- Mercury and mercury compounds
- Chromium (VI)
- PBB (polybrominated biphenyl)
- PBDE (polybrominated biphenyl ether)

And a maximum concentration of 0.01% or 100 ppm by weight in homogeneous materials for:

- Cadmium and cadmium compounds

10.0 Ordering Information

Module	Description	QTY/Reel	Order Number
AT357	+8dBm Output Power ZigBee Module • Based on Silicon Labs EM357 • AAC AT Style Command Interpreter • EmberZNet meshing and self-healing ZigBee PRO stack • U.FL/i-Pex Antenna Connector	600	R001

Note:

All Modules are pre-programmed with AAC AT style command interpreter based on the EmberZNet stack. Customers who are using their own firmware will be able to erase and write to the flash memory of the EM357.