CONTENT

1.0 Objective

This document outlines the trouble shooting for the CT6558.

2.0 Scope

1. Used for radio trouble shooting in factory.
2. Used for radio trouble shooting in customer service.

3.0 Definition of terms

Nil

4.0 Responsibility

Nil

5.0 Detail procedure

6.0 Referrence

5.1 General description

5.11 Product overview:

CT6558 product is new model phone designed by CECW, it works at Tri-band, EGSM、DCS and PCS band its weight is only 85g, the size is **85x45x24** CT6558 is a more powerful product, with 300,000 pixels camera sensor inside, 65k colors CSTN main display which pixels is 128*160,sub-display is STN screen, and has 64 polyphonies, and has hand free function.

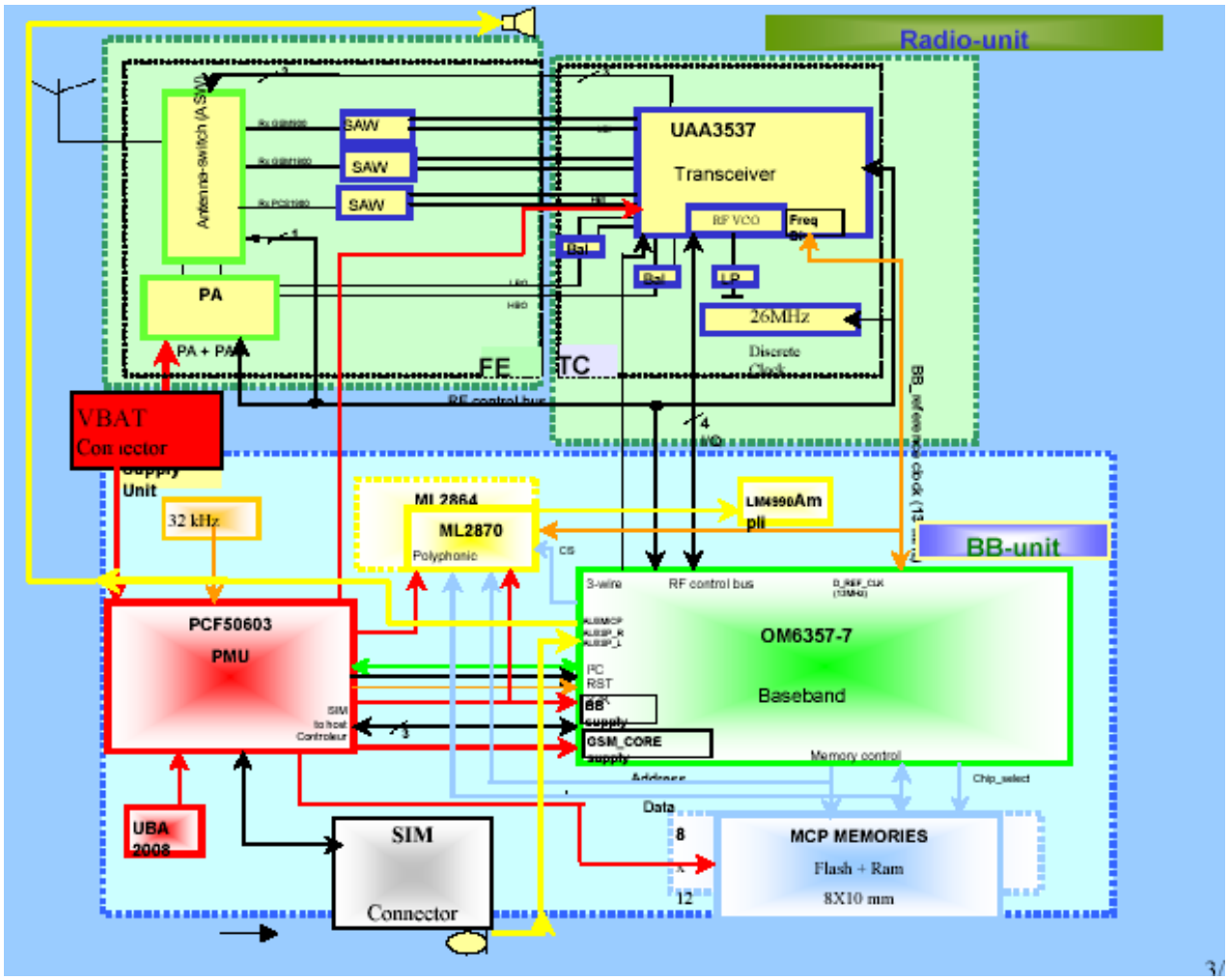
CT6558 CPU runs at 13MHz, with 128M Flash Memory and 32M SRAM. The main IC include CPU（OM6357EL/3C5/7）、FLASH(M36L0R7050T0ZAQT /STM)、PMU(PCF50603)、Transceiver(UAA3537HN)、PA(SKY77324), CT6558 can dial 4 hours continuously and can be in idle mode up to 400hours ,using 600Mah LI battery.

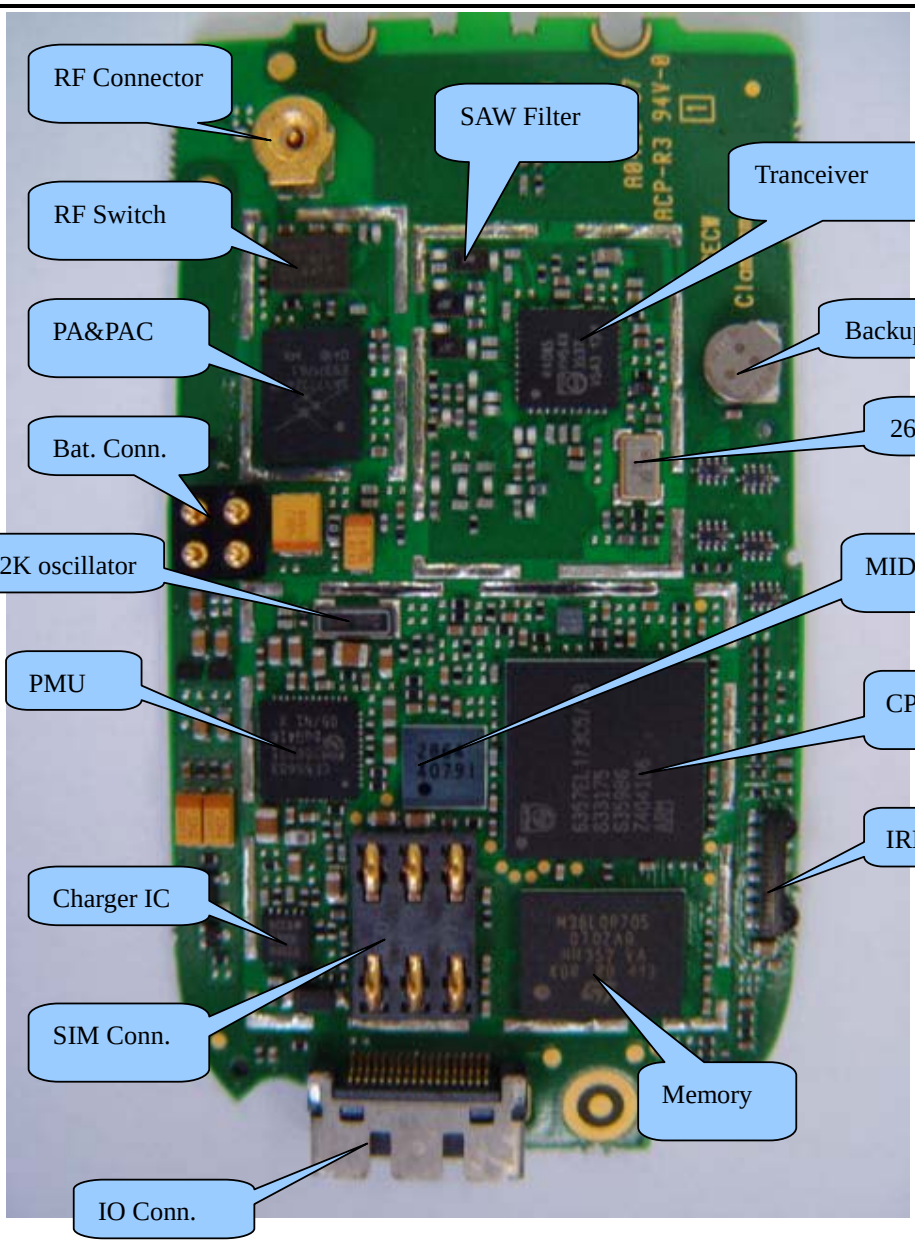
5.1.2 Product technical parameters:

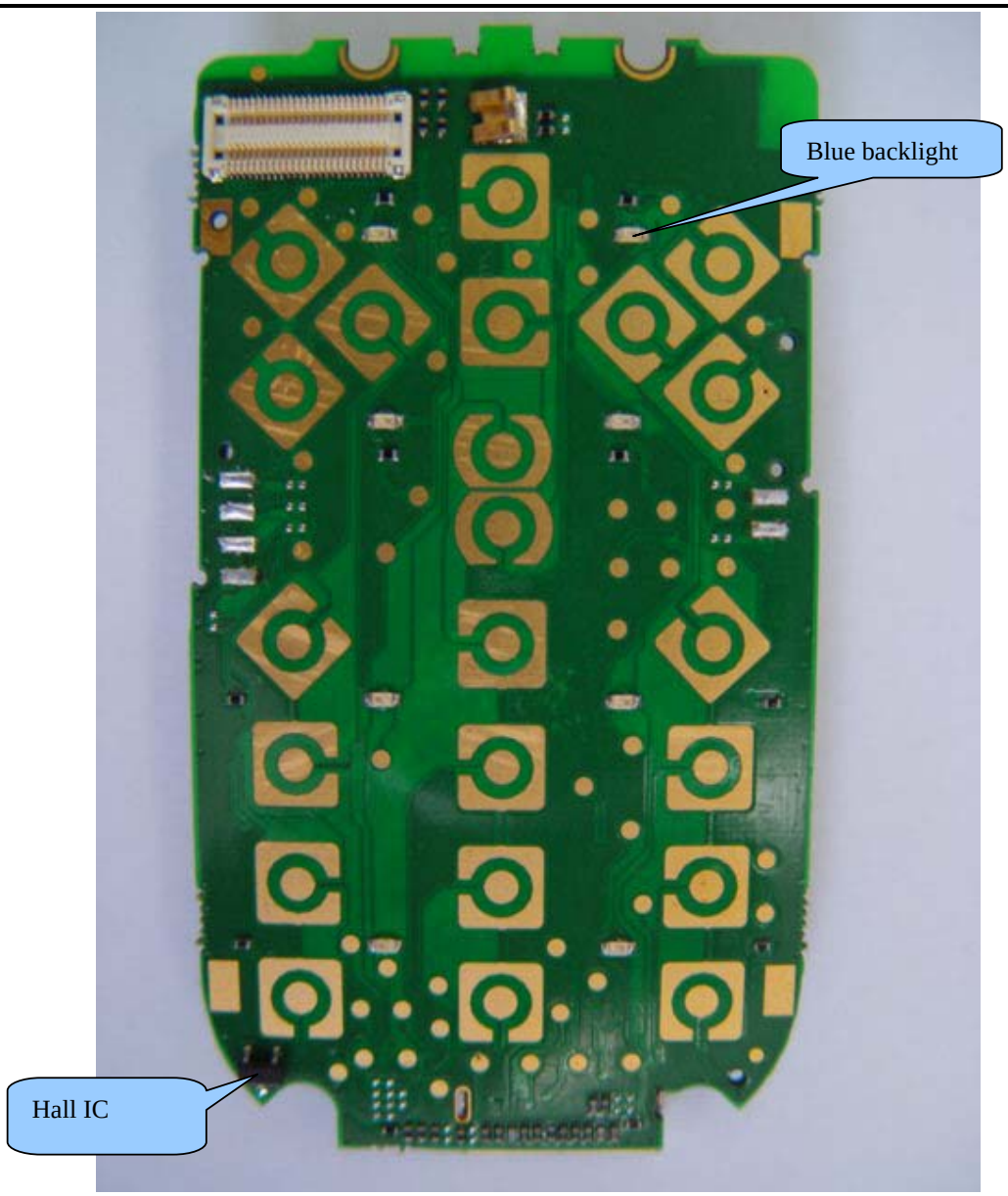
GENERAL:

item	EGSM(GSM)	DCS	PCS
Frequency allocation	TX（Uplink）:880MHZ-915MHZ RX（Downlink）:925MHZ-960MHZ	TX（Uplink）:1710MHZ-1785MHZ RX（Downlink）:1805MHZ-1880MHZ	TX（Uplink）：1850MHZ-1910MHZ RX（Downlink）:1930MHZ-1990MHZ
Channel band width	200KHz	200KHz	200KHz
Channel	975-1023,0-124	512-885	512-810
Modulation	GMSK,BT=0.3	GMSK,BT=0.3	GMSK,BT=0.3
TX/RX channel space	45MHz	95MHz	80MHz
(Fn)Freq. calculating formula	GSM Fn=890.2+(N-1)*0.2 EGSM Fn=880.2+(N-975)*0.2 N: Channel No. Unit: MHz	Fn=1710.2+(N-512)*0.2 Unit: MHz	Fn=1850.2+(N-512)*0.2 Unit: MHz

5.2 CT6558 Signal Flow Overview:

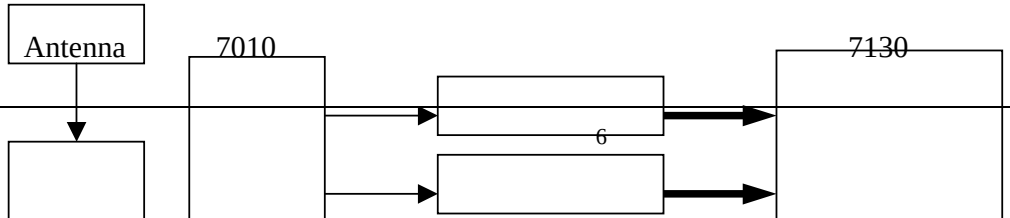

Radio-unit
Antenna-switch (ASW)
SAW
SAW
SAW
UAA3537
Transceiver
RF VCO
Freq
LP
26MHz
Discrete
PA
PA + PA
FE
TC
RF control bus
VBAT
Con ıector
Unit
32 kHz
ML2870
Polyphonic
LM4990Am
pli
BB-unit
3-wire
RF control bus
PCF50603
PMU
OM6357-7
Baseband
I²C
RST
BB
supply
GSM_CORE
supply
Memory control
Chip_select
Data
8
12
MCP MEMORIES
Flash + Ram
8X10 mm
UBA
2008
SIM
Connector


RF Connector
SAW Filter
Tranceiver
RF Switch
PA&PAC
Backup Battery
Bat. Conn.
26M oscillator
32K oscillator
MIDI IC
PMU
CPU
IRDA
Charger IC
SIM Conn.
Memory
IO Conn.
LCD conn.



5.2.1 Receiver principle and troubleshooting

CT6558 RX signal flow chart(Figure 1)：



EGSM SAW Filter

RF CONN → RF_SW PCS SAW Filter Tranceiver

DCS SAW Filter

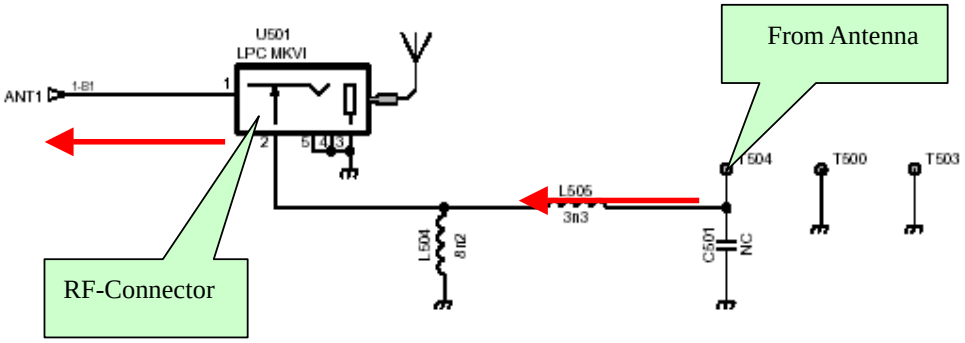
I&Q

Receiver CPU

7300

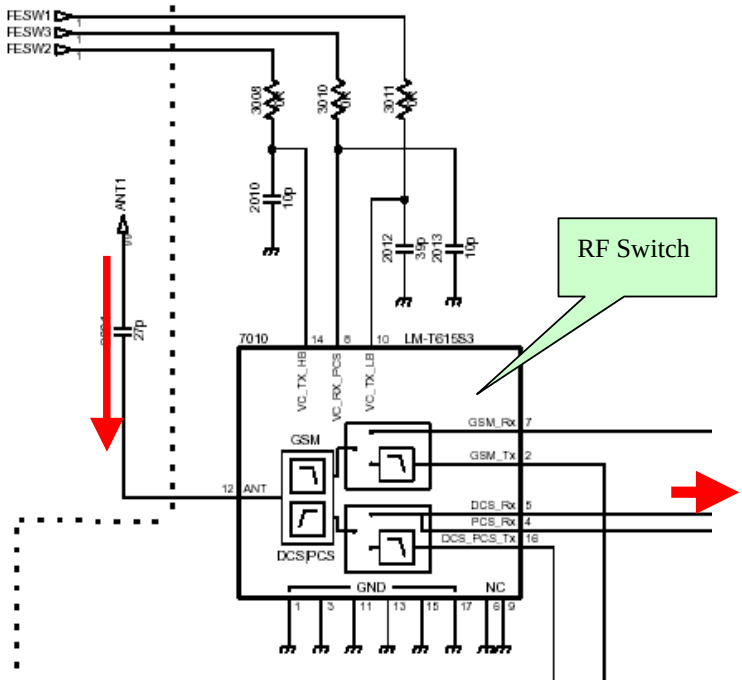
Figure 1

1.CT6558 downlink signal flow from Antenna to RF-Connector：



The aerial signal mobile phone received go from antenna to RF Connector。RF Connector, which is a special parts developed for RF test. By connecting U501 and RF cable to spectrum analyzer, you can measure the signal.

2. Signal output from RF Connector will be input to RF_SW。Tranceiver control FSW1、FSW2、FSW3 signals, which will be in charge of RF_SW in relative Band(EGSM、DCS、PCS)，and in TX/RX status.。



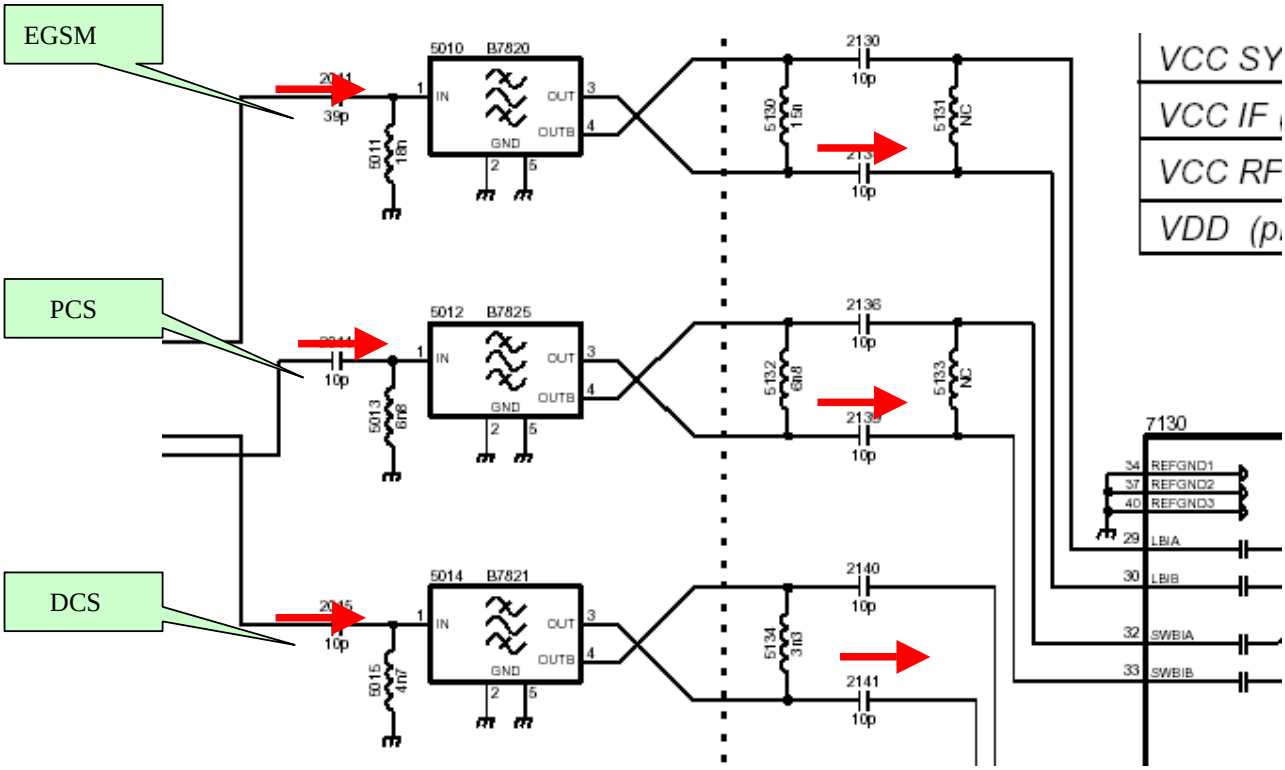
Following is the relative controlling signal status :

3. Control Logic

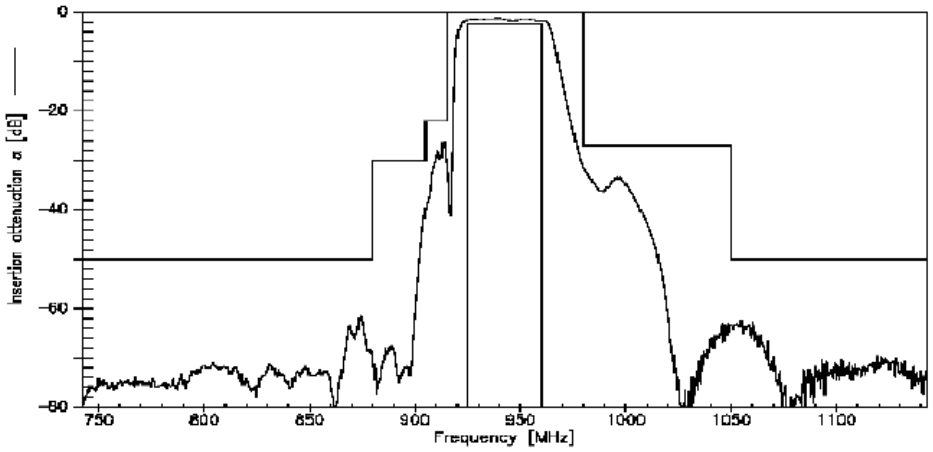
Operating Mode	VCONT1	VCONT2	VCONT3
Tx-GSM850/900	H	L	L
Tx-DCS/PCS	L	H	L
Rx-GSM850/900	L	L	L
Rx-DCS	L	L	L
Rx-PCS	L	L	H

3. The RX signal output from RF_SW, flowing to relative SAW Filter, then go through Balun circuit , input to tranceiver.

SAW Filter

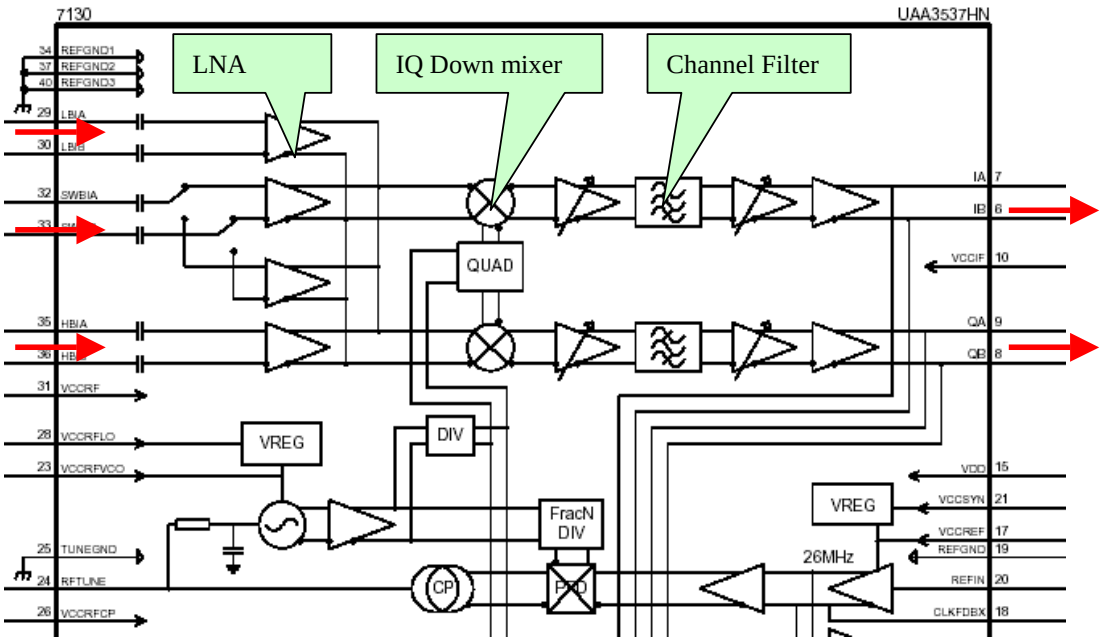


For example:(EGAM, 925-960Mhz)



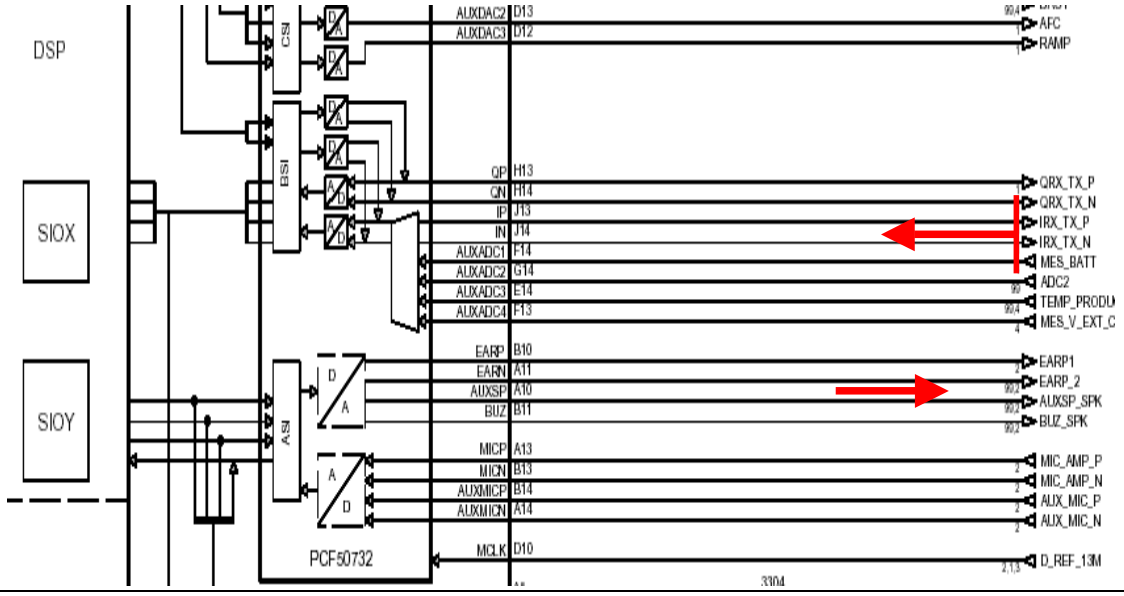
SAW Filter (EGSM)

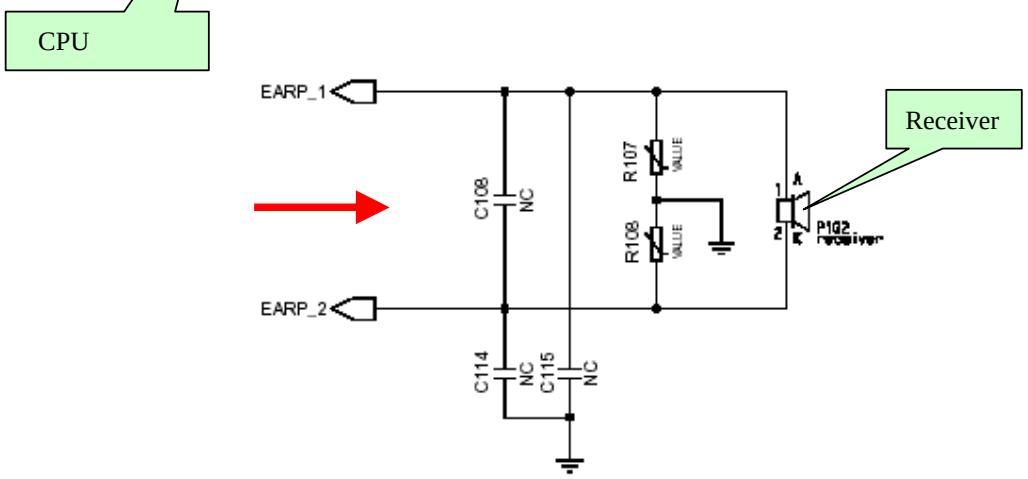
4. 7130 is the main IC in RF circuit, which response for signal modulation and demodulation. Signal input in 7130 after pass BPF, Signal pass LNA, then mix with local signal (RF-VCO) get the -100Khz signal. After pass the filter, output (IA IB QA QB) IQ signal. RF-VCO is fully integrated inside 7130.



The receiver consists of two distinct parts, the RF receiver front-end and IF section. The RF front-end amplifies the EGSM/DCS/PCS aerial signal, converts the chosen channel down to a low IF of –100kHz,and provides in addition more than 35dB image suppression. Fout LNAs are available on chip and can be configured to allow 3 bands(low, high and switched).The switched LNA will be used for roaming in different countries. some selectivity is provided at this stage by an on-chip low-pass filter,chan channel selectivity is provided by means of a high performance integrated band-pass filter. The IF section further amplifies the wanted channel, performs gain control to tune the output level to the desired value and rejects DC.

5.Four IQ signals input to CPU , go through A/D ,DSP, and D/A section in CPU , then output to receiver.





Trouble shooting to receiver circuit

1. We separate the failures in 3 parts: Logic failure, receiver failure and transmission failure. First we need define the failure according to the failed item then we begin the analysis in detail.

2. Receiver key parameters include: RX LEVEL、RX QUALITY、MOBILE CALL、FLATNESS、TIME MASK、PHASE ERROR、 FREQUENCY ERROR, etc.

2.1 Confirm the analyzer station has been set up：

a .Setup the right work condition of Agilent8960： Band: EGSM; Channel, Altitude of transmitter of the BS.

b. Power on radio, Connect the RF cable from 8960 to radio, setup right channel no. and RX altitude of debug tool, same as 8960.

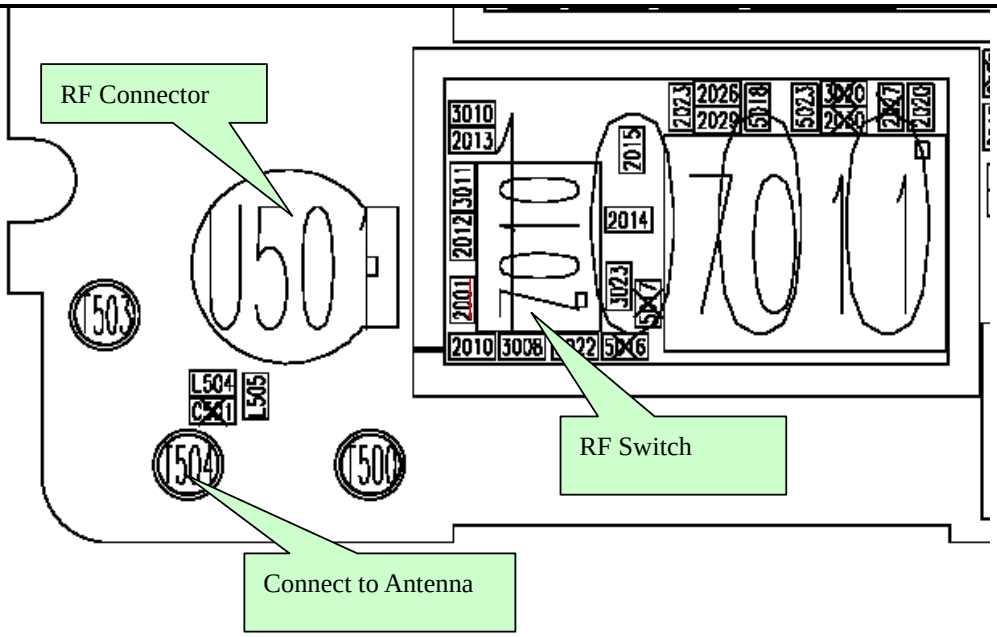
C. then using debug tool in RX mode, press ‘measure’ button to check whether the received signal is same as input signal.

Test signal on a good radio to get reference signal when you don’t know if the signal is right

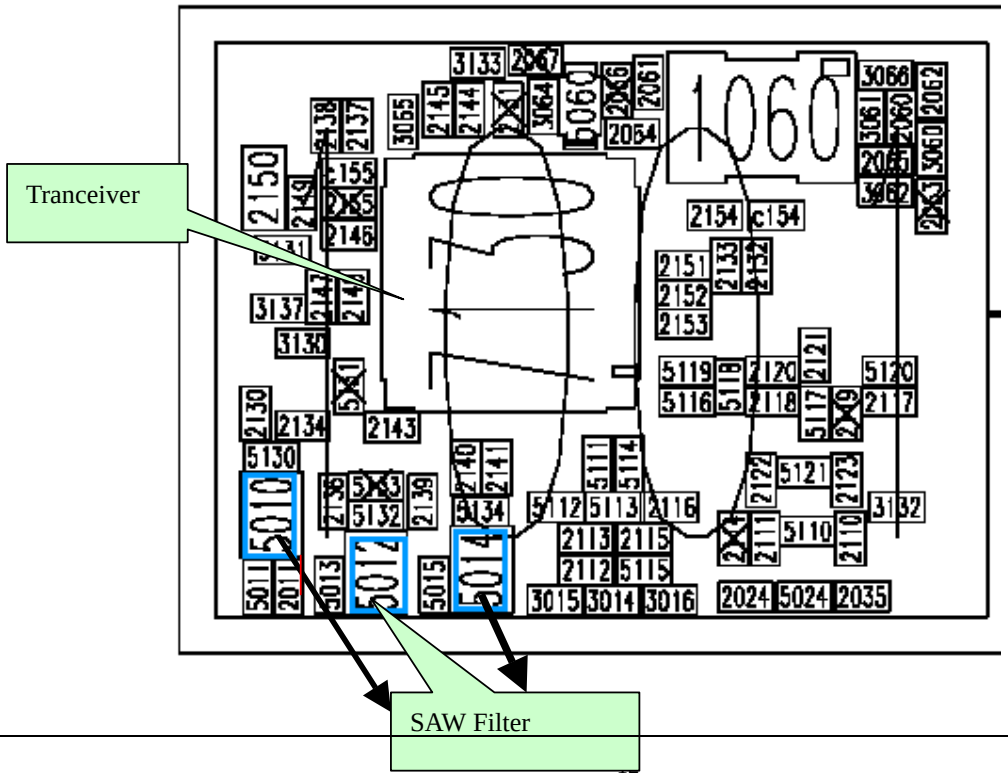
Step1:Measure the received signal according to signal flowing chart.

Measure the signal with spectrum analyzer on 2001 to check if the input signal is right. If wrong signal was detected it maybe U501 cold sold or part defect.

Measure the signal on pin12 of 7010 to check if the input signal is right. If wrong signal was detected it maybe 2001 cold soldering, tombstone part, part missing or screwed part.



Step2: Measure the output signal from 7010 to check if the signal is right, EGSM signal: measured from pin 7 (Measure at 2011); DCS signal: measured from pin5 (at 2015), and for PCS at 2014. If the signal is not right, should check if 7010 cold soldering, soldering short part, part defect or un-soldering. If no defect was found at 7010, then check if the control signal "FSW1, FSW2,FSW3" is right. If the signal is not right please check 7130 and parts around them. If no clear issue found, change 7010,7130, one by one



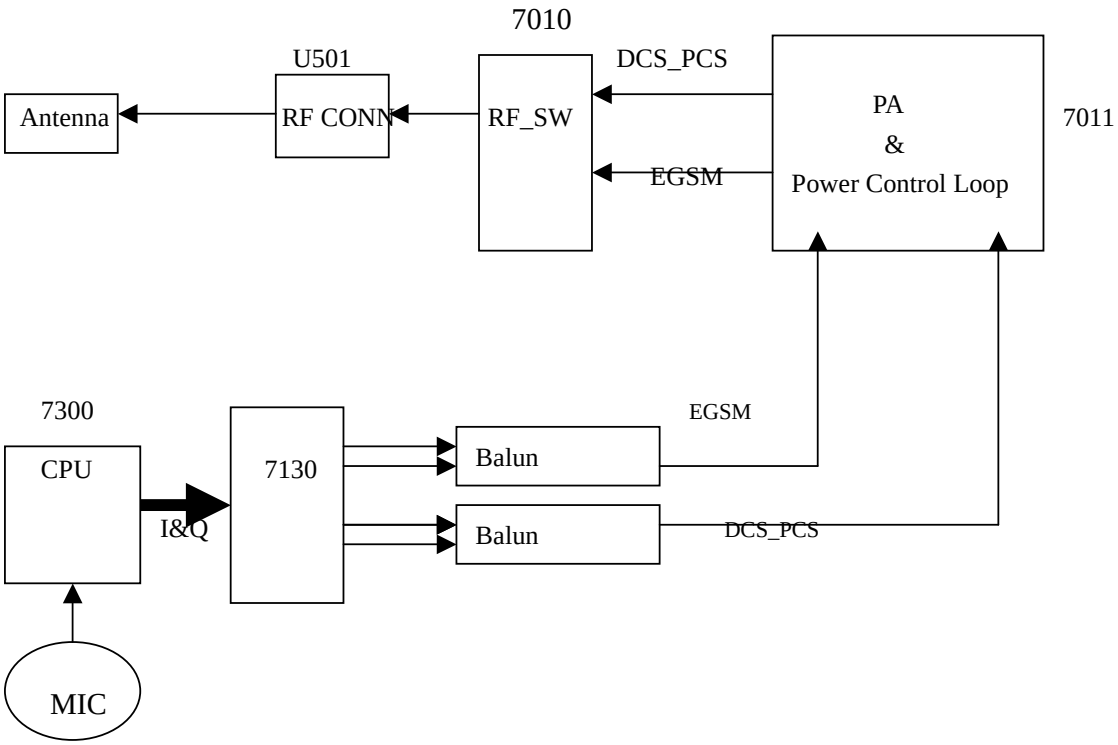
Step3: Measure the input signal and output signal of BPF. If the input signal is wrong, check on 2011: EGSM and 2015: DCS, 2014:PCS. If the output signal is wrong , check the filter 5010：EGSM，5014：DCS, 5012:PCS: 2014

Step4: Measure I/Q signal output from 7130. If the signal is not good, check if there are defects on 7130. Also need check the working voltage of 7130.

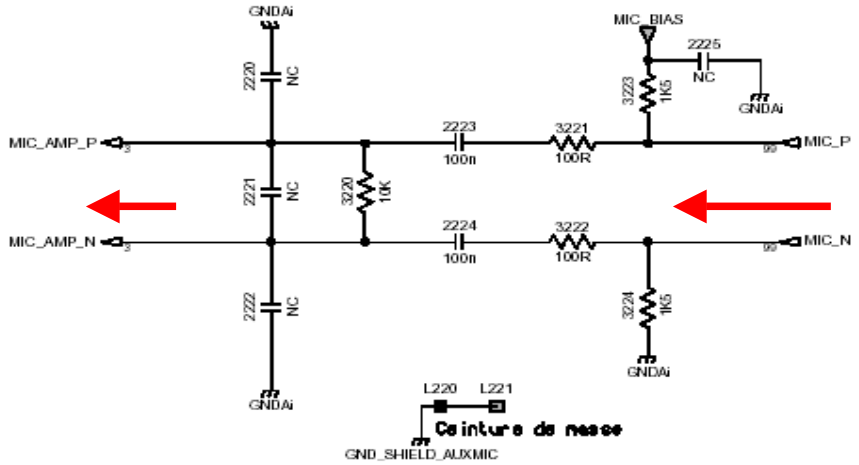
Step5: Measure I/Q Signal input to CPU, Otherwise change 7300.

5.2.2 Transmitter principle and troubleshooting:

Transmitter circuit signal flowing chart:

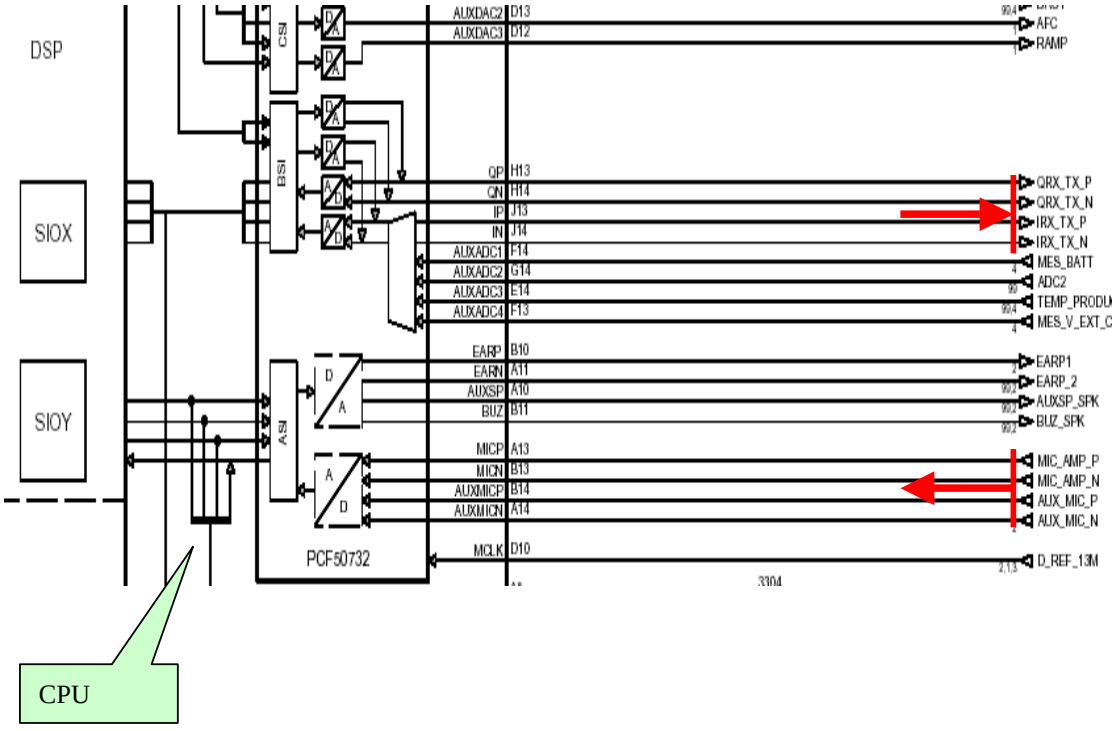


1. Micphone to CPU (7300):

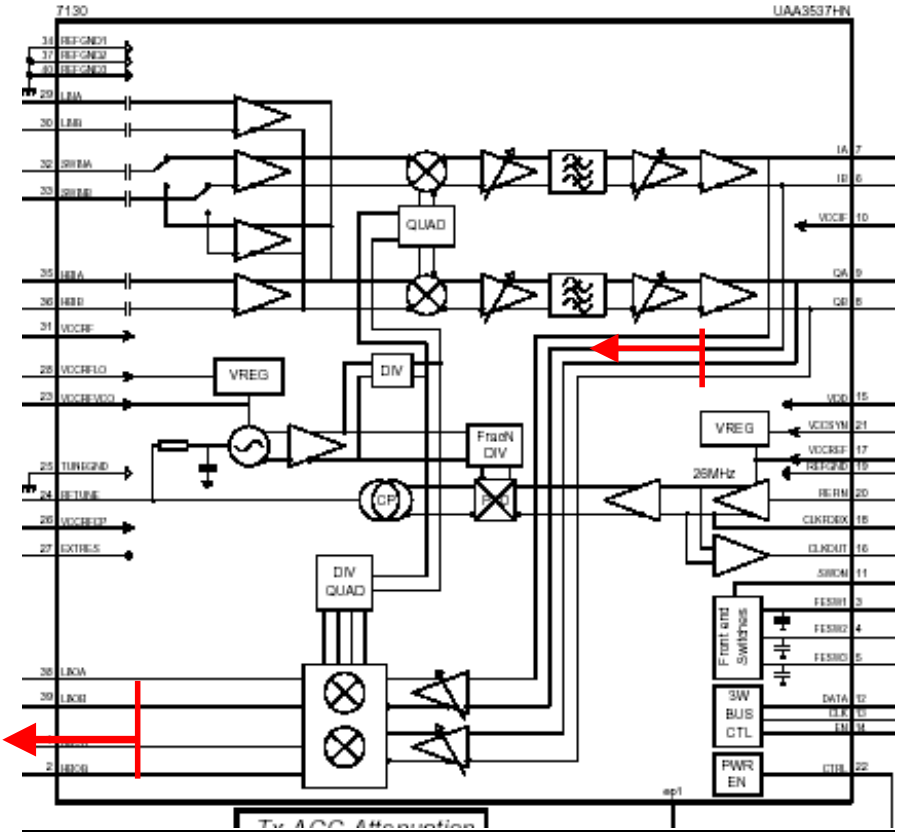


Audio signal input from Micphone , Micphone convert the voice signal to analog signal and input to CPU (7300).

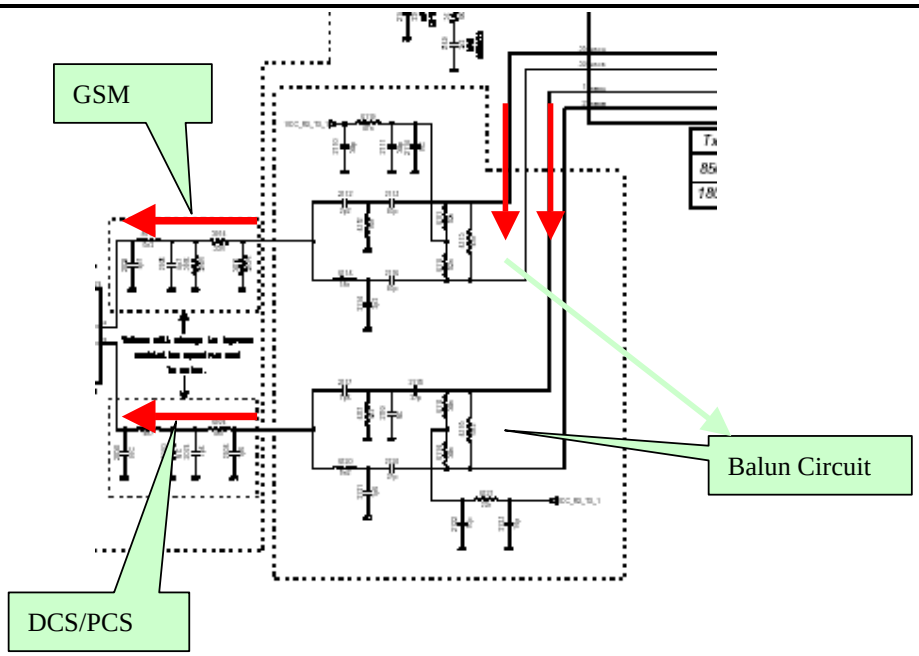
2.After A/D, convert analog signal to logic signal in CPU. Then send the logic signal to DSP pass ASI. Then processed logic signal pass D/A converter divided into four signals (IQ), output from CPU (7300) to 7130, QRX-TX-P, QRX-TX-N, IRX-TX-P, IRX-TX-N .



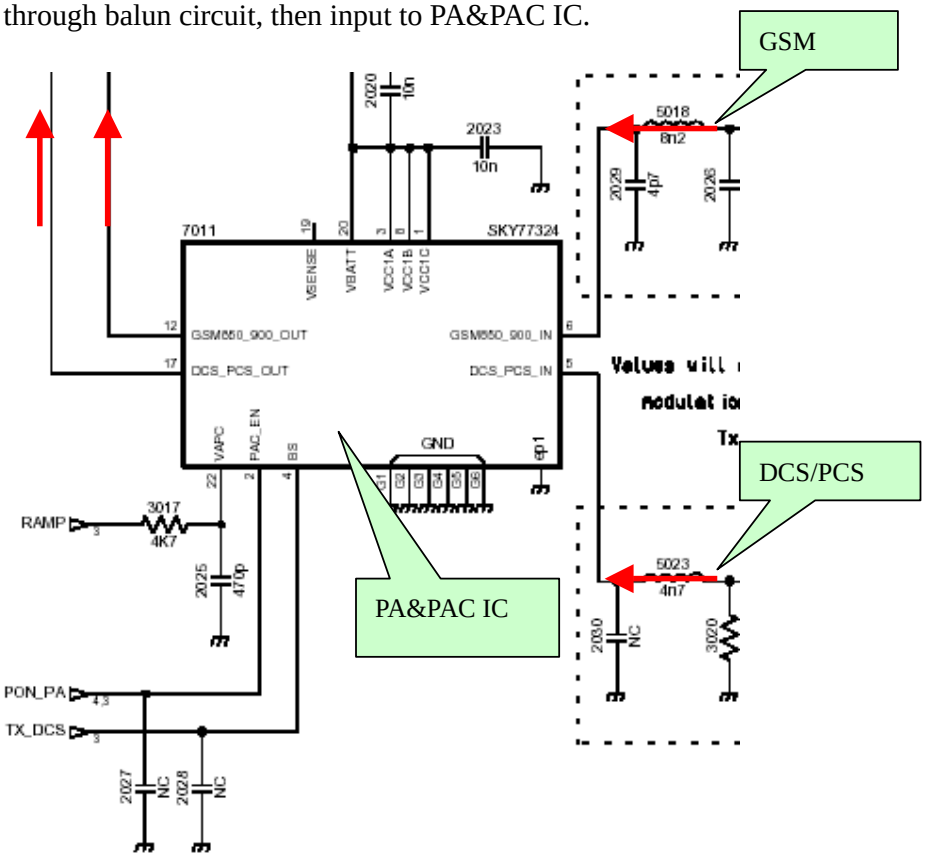
2. Then the I/Q signal modulate in 7130. The transmitter is fully differential using a direct-up conversion architecture. It consists of a single side band power up mixer. The fully-integrated VCO and the power mixer are designed to achieve LO suppression, quadrature phase error, quadrature amplitude balance and low noise floor specifications.



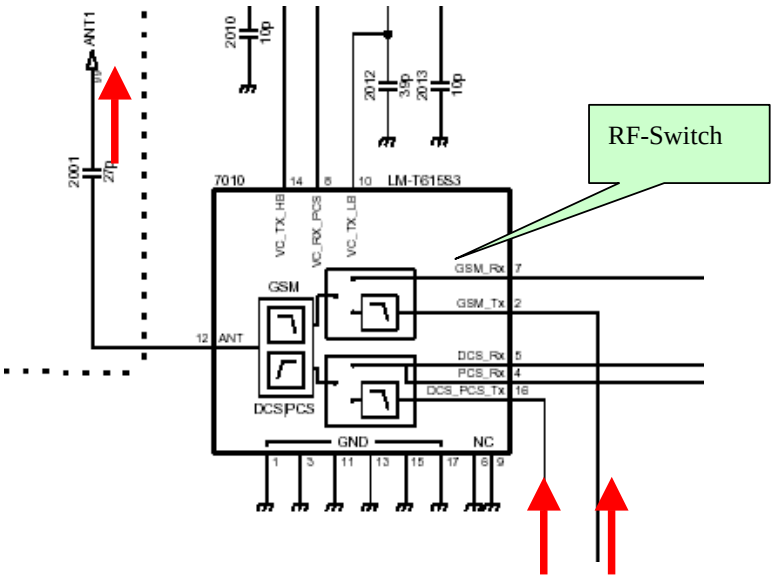
3.Output Signal from tranceiver will pass by Balun circuit, then flow to PA&PAC IC.



4.TX signal flow through balun circuit, then input to PA&PAC IC.



5. Tx signals output from PA, flow through RF-SW, RF-Connector to antenna.



TX circuit troubleshooting:

Key parameter of Tx circuit is “Freq. error”, “MAX POWER”, “TX-CURRENT”, “PA table”, etc.
Following is normal analysis of the circuit, according to failed item to do more analysis.
Confirm the instrument for analysis is good:

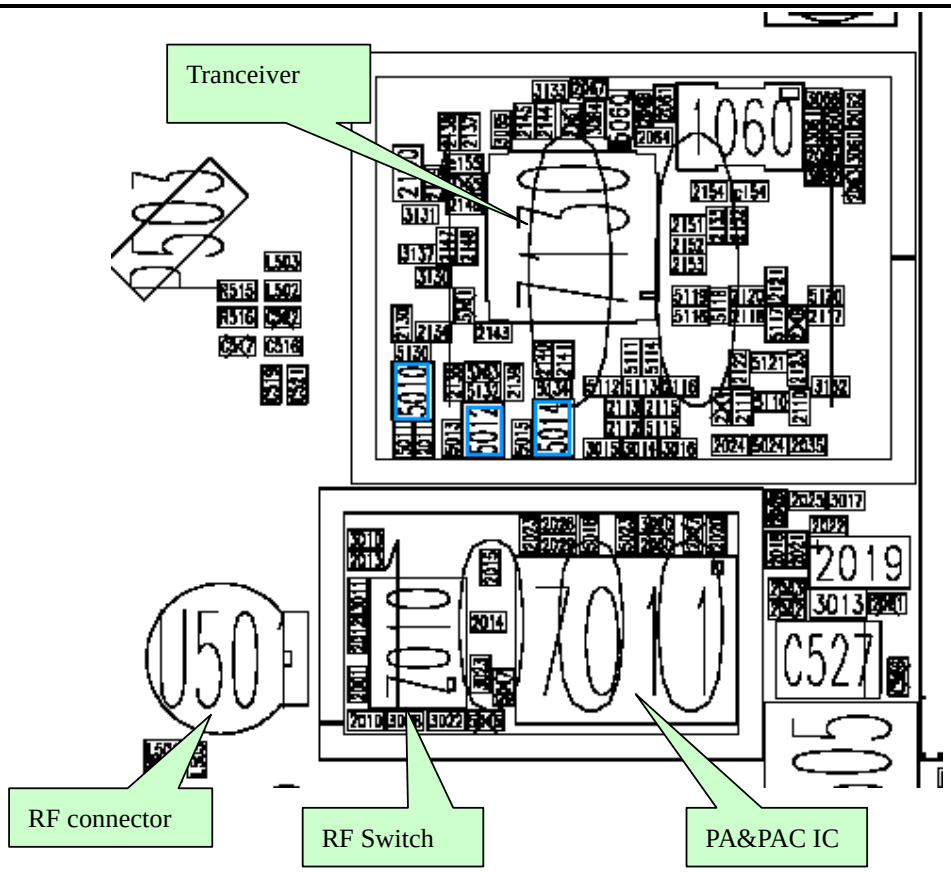
a. Power on radio, press ‘Tx command’ button, setting up the channel and power level.
b. Set the right frequency and sweeping time on spectrum analyzer.
c. Set up the voltmeter and oscilloscope.

Step1: Measure the I/Q signal from CPU (7300) to modulation and demodulation IC (7130). If the I/Q signal is not good, check CPU.

Step2: if I/Q signal is good, Measure the output signal of 7130, If the signal is not good, check 7130, and parts around 7130.

Step3: If the signal output from 7130 is right, continue to measure the TX signal at Balun circuit, and check balun Circuit parts around.

Step4:If the output signal from Balun circuit is good , continue to check output signal of PA. Measure the EGSM signal at pin12 of PA; Measure DCS signal at pin17 of PA. If the output signal is not good check PA or parts around PA. Check the operating voltage “VBAT” and control signal.



Step5: Measure the input signal and output signal of RF-SWITCH (7010). Also need check and control signal of 7010 . Measure antenna at last. CheckU501,Antenna, if the signal is not good.

5.2.3 Logic circuit principle and troubleshooting:

radio can't turn on

1. the turning on process introduction :

A. First power on radio, then after getting V_BAT, PMU will generate V_ISUP(2.7V), 7400 32.768K oscillator begin to run. ONKEY_N output 2.3V.

If radio is connected with I/O CABLE, when DownLoad software into radio, PC Sever will be ready.

B. Pressing ON_KEY, about 14ms later, PMU will generate VDD1,VDD2, VDD3,AVDD,VCC_SYN.and VDD1,VDD2 ,AVDD is supplied to CPU, V-MEM is supplied to Memory, VCC_SYN is supplied to 7130.

7130 will generate VCCREF which will be used for 1060(oscillator). After 9 CLK32 period(one CLK32 period is about 30uS),1060 will generate stable 26M clock signal, which will be divided by 2 inside 7130 ,and output REF_13M supplied to CPU.

C. After 32 CLK32 period when already generated stable 26M clock, the ON/OFF CONTROL module in PMU will generate RESTO_N signal, which will flow to CPU ,and reset CPU.

D. After resetting CPU, the basic turning on information read from ROM inside will be sent out by TXD0 pin, these codes will be sent to connector, if connector is connected with PC Sever by I/O CABLE, PC Sever will send back a reply code by RXD0 pin to CPU, Radio hand in PC successfully. Then begin to download '.fdl' file into Flash.

E. If connector is not connected with PC by I/O CABLE, no reply code feedback, CPU will run , open Bus, send out Chip-select signal, then run '.fdl' file in Flash, open backlight, display etc, enter normal mode.

2. **Trouble shooting :Radio cannot power on:**

A.

a. Power the radio measure "VBAT". If the voltage is not correct check battery or power supply.

b. Check the battery connector or interface connector.

c. Check the base band power supply and RF power supply provide by 7400. if not correct change 7400.

d. Check if 32Khz oscillator work. If not work change oscillator.

e. Check if 26M oscillator work. If it doesn't work, change 26M oscillator. Also need check the parts around it;

f. Check PMU, Memory, CPU, tranceiver, otherwise change them.

Vibration issue:

Check if the vibrator is good.

Check if there are assembly issues.

Check if the motor connector, has problem.

Check relative parts.

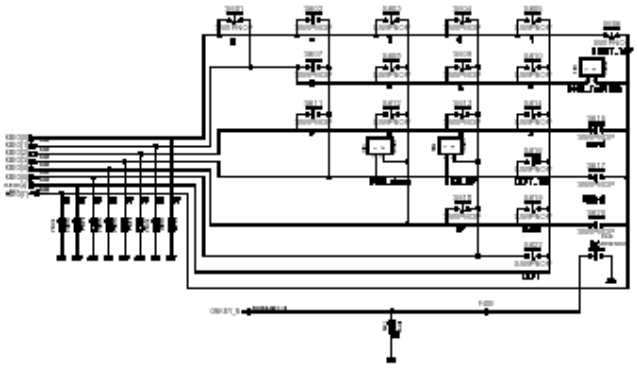
No key function:

Check metal dome, otherwise change it.

Check side key, whether there is soldering issue.

Check whether it's PCB issue.

Check CPU IC whether CS,US, otherwise change it.

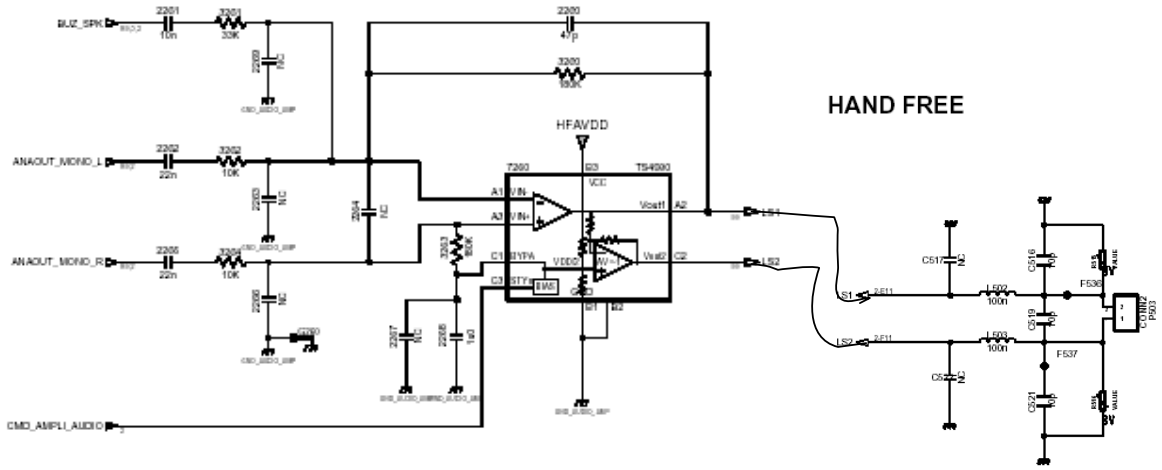


No hand free function:

Check the soldering issue of component.

Check Audio PA 7200,whether CS,US CD.

Check Speaker, LCD FPC, otherwise change them.



Mic has no function:

Check the assembly of Mic. Avoid assembly issue.

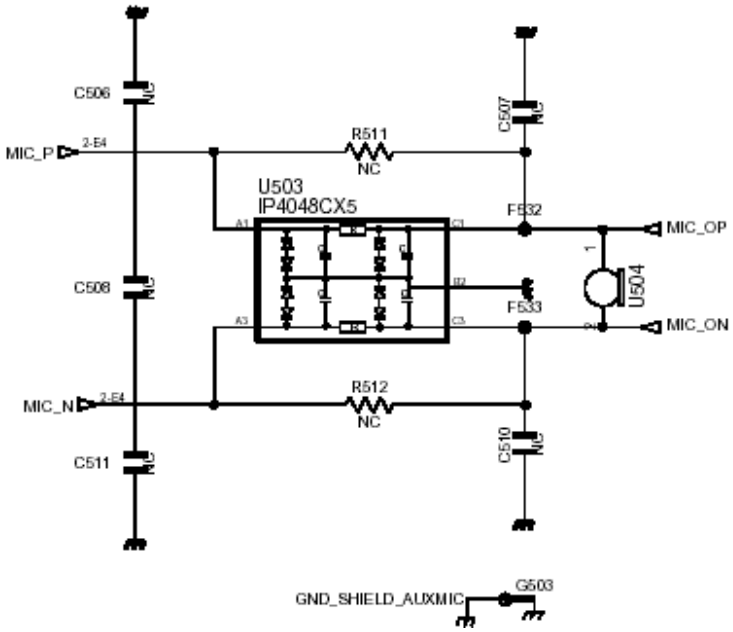
Check the signal at contact point to the Mic.

If the signal is not correct check the part in the circuit.

Check the signal “MIC-BIAS”. If it’s not correct, change 7400.

Otherwise change MIC, U503 in turns.

MICROPHONE



Check SIM card issue:

Check whether the SIM card can work

Check no soldering issue to SIM connector.

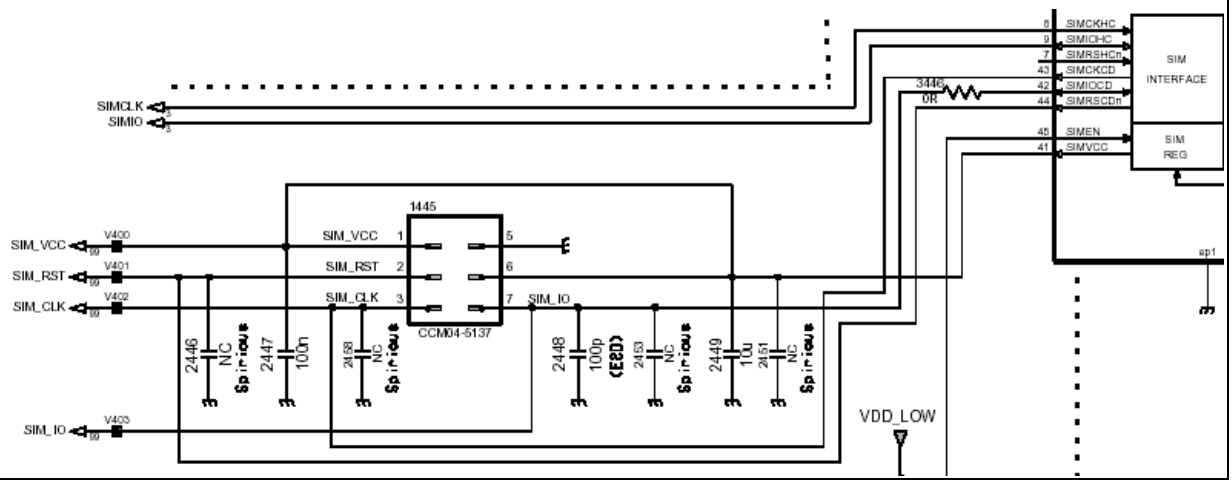
Check the good contact between SIM card and the connector

Check if the power signal is correct.

Check if the clock signal is correct.

Check if I/O signal is correct.

Otherwise change SIM connector, PMU, CPU in turns.



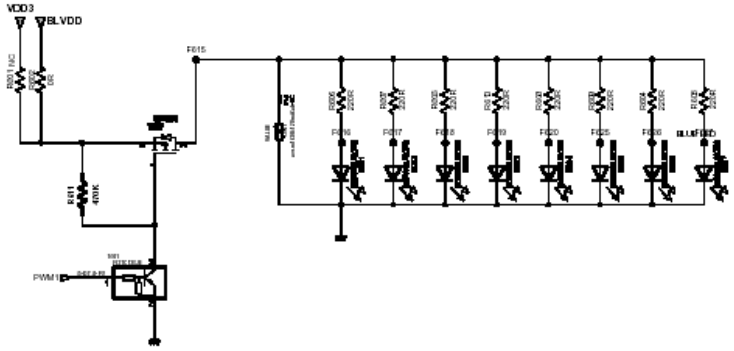
No back light：

1．Check back light and Resistance。

2．Check voltage of BLVDD，if it is abnormal, change 7400。

3．Check T602,T601 and relative parts, otherwise change it。

BACKLIGHT FOR KEYPAD



No display：

1．Check LCD FPC ,re-assemble the phone。

2．Check Connector on PCBA,， Pin on LCD PCB, whether CS,US,SS,CD。

3．Check LCD MODULE whether it’s defective.

4．Otherwise change CPU,MEMORY, PMU in turn。

No camera function：

1．Check LCD FPC ,if it’s defective, change it .

2．Check LCD MODULE(Sensor inside), if it’s defect, change it .

3．Check LCD Connector on PCBA, whether it’s CS,US SS.

4．Otherwise change CPU, MEMORY IC in turn.

No charging function:

Check if the battery connector is good.

Check whether the charging IC is good.

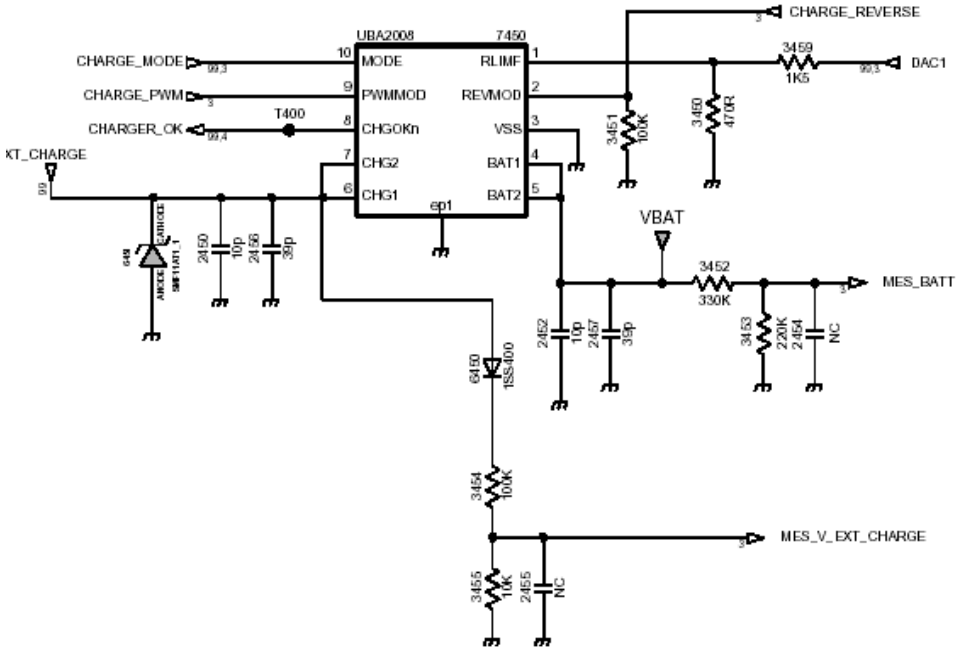
Check other relative parts around charging circuit

Check all the relative signals.

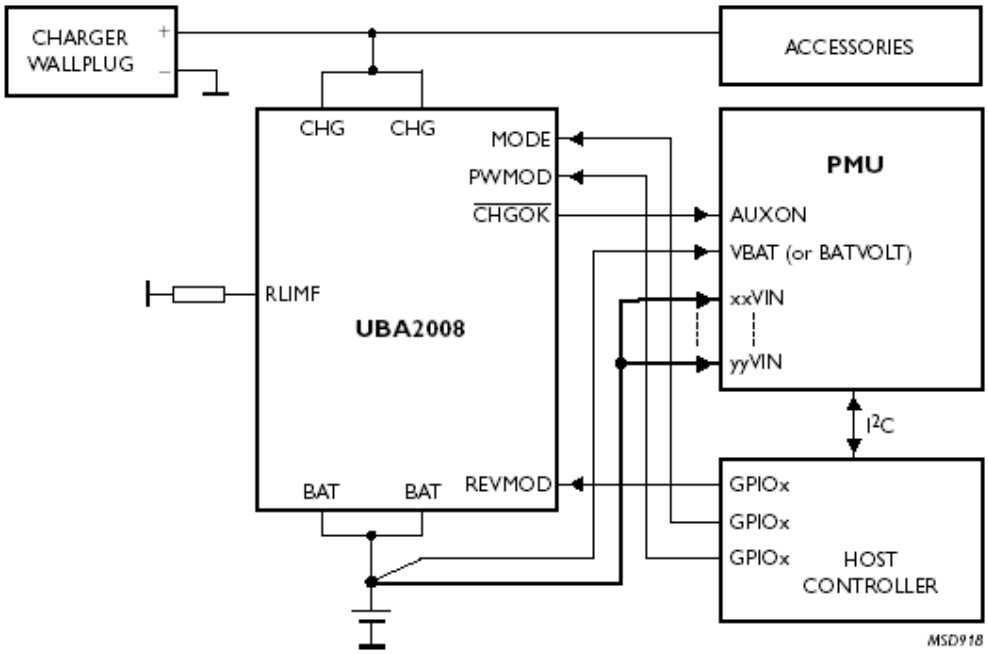
Change 7450,7400, 7300 one by one at last.

Charge of Battery

REF = 450-499 Function code = 2B7

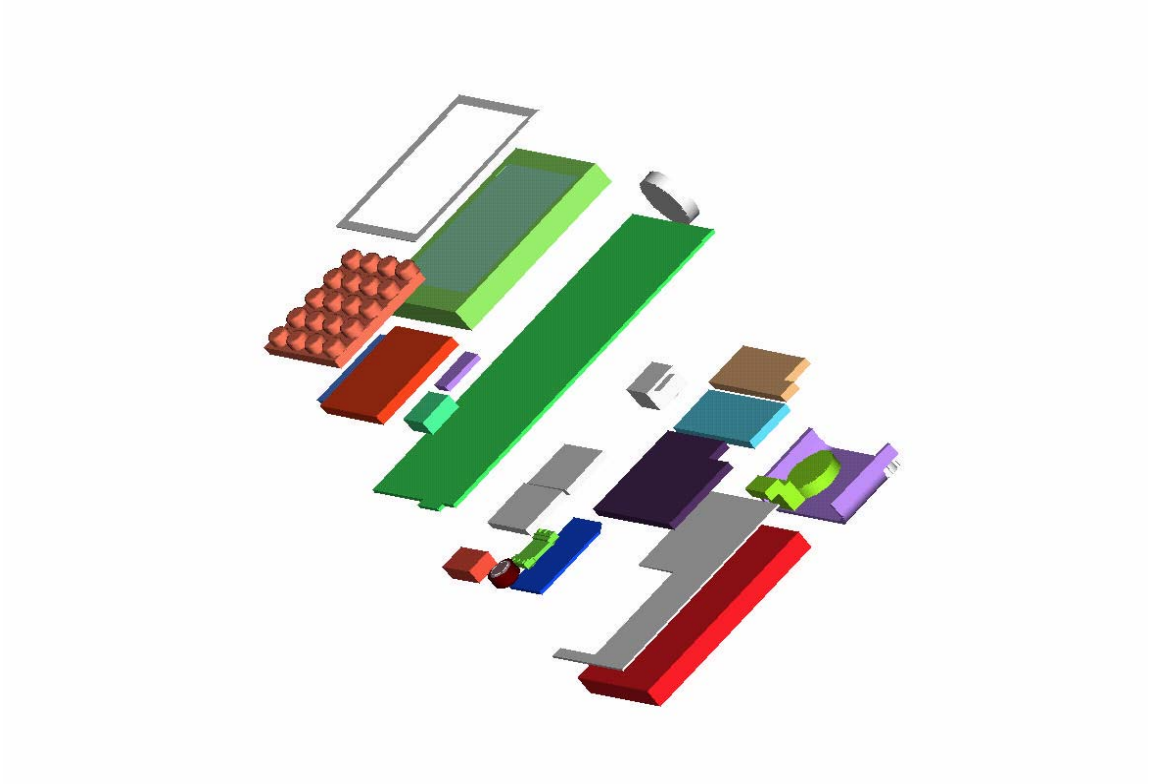


charging function figure：



5.3 Figure:

5.3.1 Product exploded view:



5.3.2Defect description abbreviation:

冷焊	CS（Cold Solder）	多余焊锡	ES（Excess Solder）	元件歪斜	SP（Skewed Part）
连焊	SS（Solder Short）	元件翘起	TP(Tombstone Part）	元件移动	MP（Misaligned Part）
开路	OT（Open Trace）	元件放反	RP（Reversed Part）	元件丢失	PM（Part Missing）
短路	DS（Direct Short）	多余元件	EP（Extra Part）	元件损坏	DP（Damaged Part）
错件	WP（Wrong Part）	管脚弯曲	BP（Bent Pin）	元件缺陷	CD(Component Defect)
虚焊	PS（Pretense Solder）	焊锡不足	IS（Insufficient Solder）		

6 Reference

CT6558 main IC introduction:

6.1 CPU (OM6357-7)

7300:

1 GENERAL REMARKS

The OM6357-7 is a multichip package (MCP) containing two integrated circuits. It is designed to provide the baseband processing for GSM handsets. The components are:

- PCF50874-6, an integrated baseband processor with an ARM micro controller, R.E.A.L. DSP, timer and interface hardware.
- PCF50732, an analogue baseband and audio interface with voiceband processor (VSP), baseband and auxiliary CODECs.

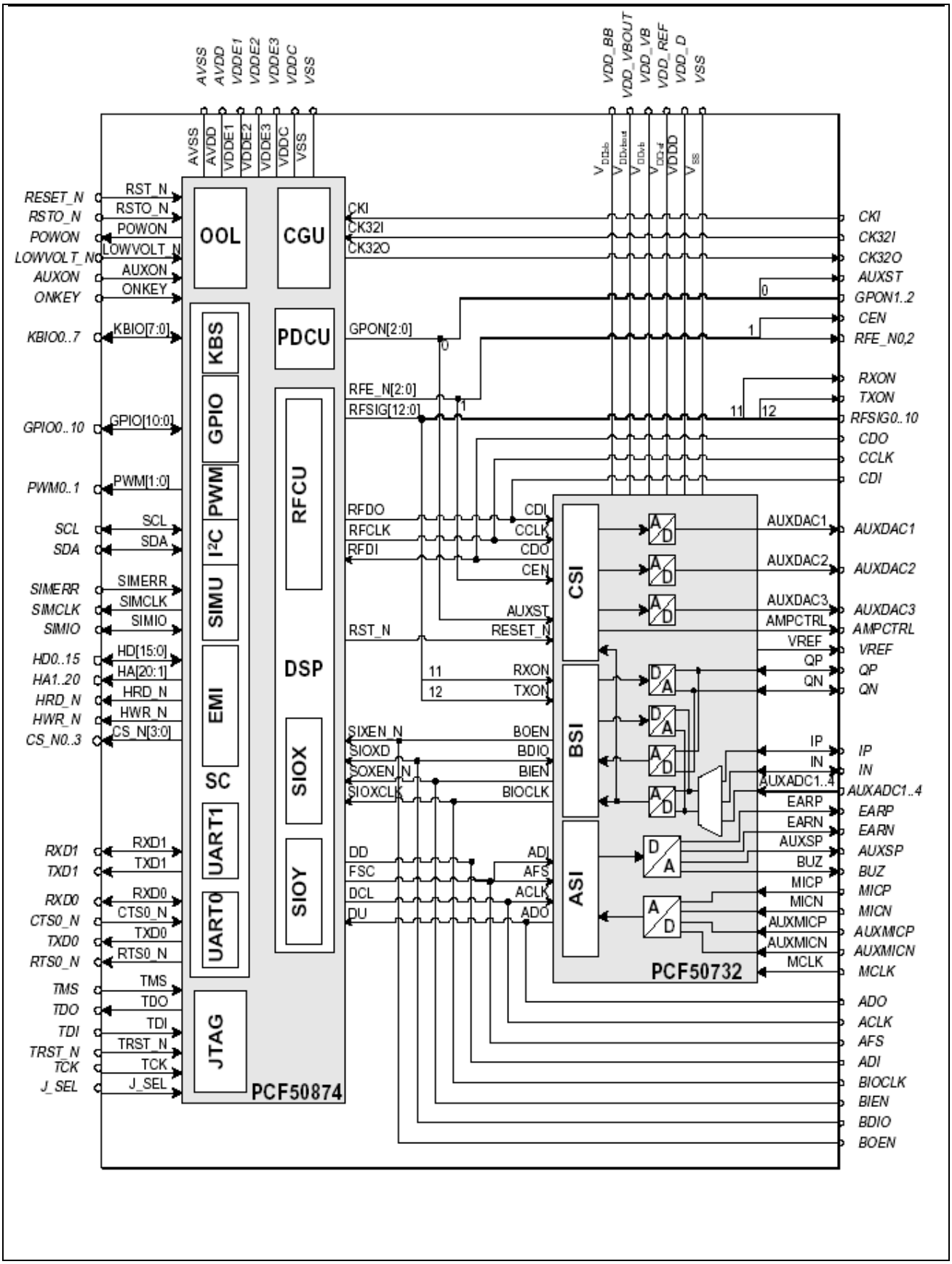

PCF50874
PCF50732
OOL
CGU
KBS
PDCU
GPIO
RFCU
PWM
I²C
SIMU
DSP
EMI
SC
SIOX
UART1
SIOY
UART0
JTAG
CSI
BSI
ASI
A/D
D/A
AVSS
AVDD
VDDE1
VDDE2
VDDE3
VDDC
VSS
VDD_BB
VDD_VBOUT
VDD_VB
VDD_REF
VDD_D
RESET_N
RSTO_N
POWON
LOWVOLT_N
AUXON
ONKEY
KBIO0..7
GPIO0..10
PWM0..1
SCL
SDA
SIMERR
SIMCLK
SIMIO
HD0..15
HA1..20
HRD_N
HWR_N
CS_N0..3
RXD1
TXD1
RXD0
CTS0_N
TXD0
RTS0_N
TMS
TDO
TDI
TRST_N
TCK
J_SEL
RST_N
POWON
LOWVOLT_N
AUXON
ONKEY
KBIO[7:0]
GPIO[10:0]
PWM[1:0]
SCL
SDA
SIMERR
SIMCLK
SIMIO
HD[15:0]
HA[20:1]
HRD_N
HWR_N
CS_N[3:0]
RXD1
TXD1
RXD0
CTS0_N
TXD0
RTS0_N
TMS
TDO
TDI
TRST_N
TCK
J_SEL
CKI
CK32I
CK32O
GPON[2:0]
RFE_N[2:0]
RFSIG[12:0]
RFDO
RFCLK
RFDI
RST_N
SIXEN_N
SIOXD
SOXEN_N
SIOXCLK
DD
FSC
DCL
DU
CDI
CCLK
CDO
CEN
AUXST
RESET_N
RXON
TXON
BOEN
BDIO
BIEN
BIOCLK
ADI
AFS
ACLK
ADO
AUXDAC1
AUXDAC2
AUXDAC3
AMPCTRL
VREF
QP
QN
IP
IN
AUXADC1..4
EARP
EARN
AUXSP
BUZ
MICP
MICN
AUXMICP
AUXMICN
MCLK
CKI
CK32I
CK32O
AUXST
GPON1..2
CEN
RFE_N0,2
RXON
TXON
RFSIG0..10
CDO
CCLK
CDI
AUXDAC1
AUXDAC2
AUXDAC3
AMPCTRL
VREF
QP
QN
IP
IN
AUXADC1..4
EARP
EARN
AUXSP
BUZ
MICP
MICN
AUXMICP
AUXMICN
MCLK
ADO
ACLK
AFS
ADI
BIOCLK
BIEN
BDIO
BOEN

Table 4 Pin Description

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
Power and Ground[5][6][7]								
VSS	Ground connections PCF50874-6	C3, E8, G1, G13, J1, K1, K7, M7, N5, N10, N11, N14, P1	G		VSS			
AVSS	Analog ground PCF50874-6	P10	G		AVSS			
VSS_BB	PCF50732 Baseband analog ground	E13				G		V_{SS}
VSS_REF	PCF50732 Bandgap Reference ground	C13				G		V_{SS}
VSS_VB	PCF50732 Voiceband ground	A12				G		V_{SS}
VSS_VBOUT	PCF50732 Voiceband output drivers ground	C11				G		V_{SS}
VSSD	PCF50732 Digital ground	D11				G		V_{SS}
VDD_BB	Analog supplies PCF50732	F12				P		V_{DDbb}
VDD_REF		D14				P		V_{DDref}
VDD_VB		B12				P		V_{DDvb}
VDD_VBOUT		C12				P		$V_{DDvbout}$
VDD_D	Digital supply PCF50732	C9	P			P		VDDD
AVDD	Analog supply PCF50874-6	P12	P		AVDD			
VDDE1	Digital supplies for PCF50874-6	C8, H11, N12, P9	P		VDDE1			
VDDE2		P8, C1	P		VDDE2			
VDDE3		P4, M6, G2, L3	P		VDDE3			
VDDC	Digital supply for core of PCF50874-6	F5, N13, M8, K6	P		VDDC			
Reference Voltage								

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
VREF	bandgap reference for external noise decoupling	C14				I/O	VDD_REF	VREF
On/Off Logic								
RST_N[5]	PCF50874-6 reset output	H10	I/O	VDDE1	RST_N			
RESET_N[5]	PCF50732 reset input	C10				I	VDDD	RESET_N
RSTO_N	PCF50874-6 reset input	M10	I	VDDE1	RSTO_N			
AUXON_N	auxiliary power-on signal	K14	I	VDDE1	AUXON_N			
Clocks								
CKI	13MHz clock input	P11	I	AVDD	CKI			
CKI32I	32kHz clock input	P13	I	VDDE1	CLK32I			
CK32O_TEST/TRCCLK[2]	CLK32k test output/Trace Clock	P14	O	VDDE1	CLK32O_TEST/TRCCLK			
MCLK	13MHz clock input	D10				I	VDD_BB	MCLK
RF Control Interface								
CCLK	RF interface clock	E10	O	VDDE1	RFCLK	I	VDDD	CCLK
CDO	control serial data	E9	I	VDDE1	RFDI	O	VDDD	CDO
CDI	control serial data	D8	O	VDDE1	RFDO	I	VDDD	CDI
CEN	enable ctrl. serial	D9	O	VDDE1	RFE_N1	I	VDDD	CEN
RFE_N2	additional RF interface enables	K12	O	VDDE1	RFE_N2			
RFE_N0/ TRCPKT[0][2]	RF interface group enable 0/Trace Packet Port	J12	O	VDDE1	RFE_N0/ TRCPKT[0]			
RFSIG12/ PIPESTAT[2] [2]	baseband transmit active/Pipeline Status	G12	I/O	VDDE1	RFSIG12/ PIPESTAT[2]	RFIG12/RFSIG11 is indirectly showing the package internal connection to the PCF50732		
RFSIG11/ PIPESTAT[1] [2]	baseband receive active/Pipeline Status	H12	I/O	VDDE1	RFSIG11/ PIPESTAT[1]			
RFSIG10	signal generator output	D7	O	VDDE1	RFSIG10			
RFSIG9/PIPESTAT[0][2]	signal generator output/Pipeline Status	K10	O	VDDE1	RFSIG9/ PIPESTAT[0]			

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
RFSIG8	signal generator output	E7	O	VDDE1	RFSIG8			
RFSIG7	signal generator output	C6	O	VDDE2	RFSIG7			
RFSIG6	signal generator output	B7	O	VDDE2	RFSIG6			
RFSIG5/ TRCSYNC[2]	signal generator output/Trace Synchronisation	C7	O	VDDE2	RFSIG5/ TRCSYNC			
RFSIG4	signal generator output	A7	O	VDDE2	RFSIG4			
RFSIG3	signal generator output	B6	O	VDDE2	RFSIG3			
RFSIG2	signal generator output	D6	O	VDDE2	RFSIG2			
RFSIG1	signal generator output	A6	O	VDDE2	RFSIG1			
RFSIG0	signal generator output	D5	O	VDDE2	RFSIG0			
Baseband Interface								
SIOXCLK/ TRCPKT[7][2]	interface clock/Trace Packet Port	F11	I/O	VDDE1	SIOXCLK/ TRCPKT[7]	SIOXCLK/SIXEN_N/ SOXEN_N is indirectly showing the package internal connection to the PCF50732		
SIXEN_N/ TRCPKT[5][2]	baseband serial data enable RX/ Trace Packet Port	G11	I/O	VDDE1	SIXEN_N/ TRCPKT[5]			
SOXEN_N/ TRCPKT[6][2]	baseband serial data enable TX/ Trace Packet Port	F10	I/O	VDDE1	SOXEN_N/ TRCPKT[6]			
BDIO	baseband serial data	E11	I/O	VDDE1	SIOXD	I/O	VDDD	BDIO
Audio Interface								
DCL/ TRCPKT[2][2]	audio serial interface clock/ Trace Packet Port	B8	I/O	VDDE1	DCL/ TRCPKT[2]	DCL/FSC/ DU/DD is indirectly showing the package internal connection to the PCF50732		
FSC/ TRCPKT[1][2]	audio serial frame/ Trace Packet Port	B9	I/O	VDDE1	FSC/ TRCPKT[1]			
DU/ TRCPKT[3][2]	TX audio serial / Trace Packet Port	A9	I/O	VDDE1	DU/ TRCPKT[3]			
DD/ TRCPKT[4][2]	RX audio serial/ Trace Packet Port	A8	I/O	VDDE1	DD/ TRCPKT[4]			

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
I²C Bus								
SCL	interface clock	C2	I/O	VDDE2	SCL			
SDA	data transfer	B3	I/O	VDDE2	SDA			
Memory Interface								
HWR_N	memory control signals	L5	O	VDDE3	HWR_N			
HRD_N		H5	O	VDDE3	HRD_N			
CS_N0		N4	O	VDDE3	CS0_N			
CS_N1		G5	O	VDDE3	CS1_N			
CS_N2		M5	O	VDDE3	CS2_N			
CS_N3		G3	O	VDDE3	CS3_N			
HA1	memory address bus	M4	O	VDDE3	HA1			
HA2		P3	O	VDDE3	HA2			
HA3		L4	O	VDDE3	HA3			
HA4		N3	O	VDDE3	HA4			
HA5		K5	O	VDDE3	HA5			
HA6		M3	O	VDDE3	HA6			
HA7		P2	O	VDDE3	HA7			
HA8		N2	O	VDDE3	HA8			
HA9		M1	O	VDDE3	HA9			
HA10		N1	O	VDDE3	HA10			
HA11		L2	O	VDDE3	HA11			
HA12		L1	O	VDDE3	HA12			
HA13		M2	O	VDDE3	HA13			
HA14		J2	O	VDDE3	HA14			
HA15		J5	O	VDDE3	HA15			
HA16		K3	O	VDDE3	HA16			
HA17		J4	O	VDDE3	HA17			
HA18		K4	O	VDDE3	HA18			
HA19(1)		K2	O	VDDE3	HA19			
HA20(1)		G4	O	VDDE3	HA20			
HA21		P5	O	VDDE3	HA21			
HA22(1)		N6	O	VDDE3	HA22			
HA23(1)		L6	O	VDDE3	HA23			
HA24		J7	O	VDDE3	HA24			
HA25(1) multiplexed	SC address HA25 / LDS_N / LDS	J6	O	VDDE3	HA25			

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
HA26[1] multiplexed	SC address HA0 / HA26 / UDS_N / UDS	H6	O	VDDE3	HA26			
HD0	memory data bus	H4	I/O	VDDE3	HD0			
HD1		H3	I/O	VDDE3	HD1			
HD2		H2	I/O	VDDE3	HD2			
HD3		J3	I/O	VDDE3	HD3			
HD4		E5	I/O	VDDE3	HD4			
HD5		H1	I/O	VDDE3	HD5			
HD6		B1	I/O	VDDE3	HD6			
HD7		E4	I/O	VDDE3	HD7			
HD8		F3	I/O	VDDE3	HD8			
HD9		F2	I/O	VDDE3	HD9			
HD10		F1	I/O	VDDE3	HD10			
HD11		E1	I/O	VDDE3	HD11			
HD12		D1	I/O	VDDE3	HD12			
HD13		E3	I/O	VDDE3	HD13			
HD14		E2	I/O	VDDE3	HD14			
HD15		B2	I/O	VDDE3	HD15			
Keyboard scanner								
KBIO7	keyboard matrix	L14	I/O	VDDE1	KBIO7			
KBIO6		L12	I/O	VDDE1	KBIO6			
KBIO5		L13	I/O	VDDE1	KBIO5			
KBIO4		L11	I/O	VDDE1	KBIO4			
KBIO3		J11	I/O	VDDE1	KBIO3			
KBIO2		K13	I/O	VDDE1	KBIO2			
KBIO1		J10	I/O	VDDE1	KBIO1			
KBIO0		K11	O	VDDE1	KBIO0			
UART0								
CTS0_N	clear to send	B5	I	VDDE2	CTS0_N			
RTS0_N	request to send	A5	O	VDDE2	RTS0_N			
TXD0	transmit data	C5	O	VDDE2	TXD0			
RXD0	receive data	C4	I/O	VDDE2	RXD0			
UART1								
TXD1	transmit data	A4	O	VDDE2	TXD1			
RXD1	receive data	D4	I/O	VDDE2	RXD1			
SIM Interface								

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
SIMCLK	interface clock	M14	O	VDDE1	SIMCLK			
SIMIO	data transfer	M13	I/O	VDDE1	SIMIO			
SIMERR	error removal	M11	I	VDDE1	SIMERR			
General Purpose I/O Port								
GPIO10/EXT2	general purpose signal	K8	I/O	VDDE2	GPIO10/EXT2			
GPIO9/EXT1		N8	I/O	VDDE2	GPIO9/EXT1			
GPIO8/PWM01		P6	I/O	VDDE2	GPIO8/PWM01			
GPIO7/EXT3		N7	I/O	VDDE2	GPIO7/EXT3			
GPIO6/DSP_REQ		L9	I/O	VDDE2	GPIO6/DSP_REQ			
GPIO5		L7	I/O	VDDE2	GPIO5			
GPIO4		P7	I/O	VDDE2	GPIO4			
GPIO3/FRAME		M9	I/O	VDDE2	GPIO3/FRAME			
GPIO2		L8	I/O	VDDE2	GPIO2			
GPIO1		K9	I/O	VDDE2	GPIO1			
GPIO0		M12	I/O	VDDE2	GPIO0			
Pulse Width Modulator								
PWM1	pulse width modulator signal	E6	O	VDDE2	PWM1			
PWM0		F4	O	VDDE2	PWM0			
JTAG and Test Access Port								
TCK	interface clock	A3	I	VDDE2	TCK			
TMS	test mode select	A2	I	VDDE2	TMS			
TDI	test data input	D2	I	VDDE2	TDI			
TDO	test data output	D3	O	VDDE2	TDO			
TRST_N	reset	A1	I	VDDE2	TRST_N			
J_SEL	controller select BBP DSP or BBP SC	B4	I	VDDE2	J_SEL			
Power-Down Control								
GPON2	general purpose power down signal	N9	O	VDDE2	GPON2			
GPON1		L10	O	VDDE2	GPON1			
AUXST		G10	O	VDDE1	GPON0	I	VDDD	AUXST
IF Signals								

OM6357-7			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874-6			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
IP	baseband differential I signal	J13				I/O	VDD_BB	IP
IN		J14				I/O	VDD_BB	IN
QP	baseband differential Q signal	H13				I/O	VDD_BB	QP
QN		H14				I/O	VDD_BB	QN
Auxiliary Functions								
AUXADC1	auxiliary ADC input	F14				I	VDD_BB	AUXADC1
AUXADC2		G14				I	VDD_BB	AUXADC2
AUXADC3		E14				I	VDD_BB	AUXADC3
AUXADC4		F13				I	VDD_BB	AUXADC4
AUXDAC1	auxiliary DAC outputs	E12				O	VDD_BB	AUXDAC1
AUXDAC2		D13				O	VDD_BB	AUXDAC2
AUXDAC3		D12				O	VDD_BB	AUXDAC3
Voiceband Codec								
MICP	microphone differential input	A13				I	VDD_VB	MICP
MICN		B13				I	VDD_VB	MICN
AUXMICP	auxiliary microphone differential input	B14				I	VDD_VB	AUXMICP
AUXMICN		A14				I	VDD_VB	AUXMICN
EARN	earphone differential output	A11				O	VDD_VB OUT	EARN
EARP		B10				O	VDD_VB OUT	EARP
AUXSP	auxiliaryspeaker output	A10				O	VDD_VB OUT	AUXSP
BUZ	buzzer output	B11				O	VDD_VB OUT	BUZ

Table 3 LBGA183 Top view of MCP

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	TRST_N	TMS	TCK	TXD1	RTS0_N	RFSIG1	RFSIG4	DD/TRC PKT[4]	DU/TRC PKT[3]	AUXSP	EARN	VSS_VB	MICP	AUX MICN
B	HD6	HD15	SDA	J_SEL	CTS0_N	RFSIG3	RFSIG6	DCL/TRC PKT[2]	FSC/TRC PKT[1]	EARP	BUZ	VDD_VB	MICN	AUX MICP
C	VDDE2	SCL	VSS	RXD0	TXD0	RFSIG7	RFSIG5/ TRCSYN C	VDDE1	VDD_D	RESETN	VSS_ VBOUT	VDD_ VBOUT	VSS_ REF	VREF
D	HD12	TDI	TDO	RXD1	RFSIG0	RFSIG2	RFSIG10	CDI	CEN	MCLK	VSSD	AUX DAC3	AUX DAC2	VDD_ REF
E	HD11	HD14	HD13	HD7	HD4	PWM1	RFSIG8	VSS	CDO	CCLK	BDIO	AUX DAC1	VSS_ BB	AUX ADC3
F	HD10	HD9	HD8	PWM0	VDDC					SCKEN_ N/TRCPK T[6]	SIOXCLK /TRCPKT [7]	VDD_BB	AUX ADC4	AUX ADC1
G	VSS	VDDE3	CS3_N	HA20	CS1_N					AUXST	SIXEN_N /TRCPKT [5]	RFSIG12 /PIPESTA T[2]	VSS	AUX ADC2
H	HD5	HD2	HD1	HD0	HRD_N	HA26				RST_N	VDDE1	RFSIG11 /PIPESTA T[1]	QP	QN
J	VSS	HA14	HD3	HA17	HA15	HA25	HA24			KBIO1	KBIO3	RFE_N0 /TRCPKT [0]	IP	IN
K	VSS	HA19	HA16	HA18	HA5	VDDC	VSS	GPIO10	GPIO1	RFSIG9/ PIPESTA T[0]	KBIO0	RFE_N2	KBIO2	AUXON_ N
L	HA12	HA11	VDDE3	HA3	HWR_N	HA23	GPIO5	GPIO2	GPIO6	GPON1	KBIO4	KBIO6	KBIO5	KBIO7
M	HA9	HA13	HA6	HA1	CS2_N	VDDE3	VSS	VDDC	GPIO3	RSTO_N	SIMERR	GPIO0	SIMIO	SIMCLK
N	HA10	HA8	HA4	CS0_N	VSS	HA22	GPIO7	GPIO9	GPON2	VSS	VSS	VDDE1	VDDC	VSS
P	VSS	HA7	HA2	VDDE3	HA21	GPIO8	GPIO4	VDDE2	VDDE1	AVSS	CKI	AVDD	CKI32I	CK32O_ TEST/TR CCLK

6.2 PMU (PCF50603)

7400：POWE-SIM-MANAGEMENT

The PCF50603 is a highly integrated solution for power supply generation, battery management including charging and a Subscriber Identity Module (SIM) card interface including supply generation. The device is controlled by a host controller via a 400 kHz I^2C serial interface.

2.1 System control

- Serial 400 kHz I^2C interface to transfer the control data between the PCF50603 and the host controller.
- On/Off Control module (hereafter OOC) to control the power ramp-up and ramp-down sequences for the handset. Furthermore it determines the supported system operating states: NOPOWER, SAVE, STANDBY, ACTIVE to realize minimum power consumption in all states.
- Internal current controlled oscillator (hereafter CCO) generates the internal high clock frequency. The generated frequency is typically 3.6 MHz.
- An accurate 32.768 kHz oscillator (hereafter OSC32). This oscillator can be used to supply the 32 kHz clock domains in the system, to improve the accuracy of the internal clock, and to reduce the power consumption of the PCF50603.
- Interrupt controller (hereafter INT) that generates the interrupt request for the host controller. All interrupt sources can be masked.
- The Real Time Clock module (hereafter RTC) uses the 32 kHz clock to provide time reference and alarm functions with wake up control for the handset.
- One accessory recognition pin with debounce filters and capability to start up the system (hereafter $\overline{\text{REC1}}$).
- One accessory detection comparator input with programmable threshold levels that issues an interrupt when an accessory is connected (hereafter $\overline{\text{REC2}}$).
- Two pulse-width modulators (hereafter PWM1 and PWM2): generating an output voltage with programmable duty cycle and frequency.
- Two LED modulators (hereafter LED1 and LED2) capable of generating 8 different blinking patterns with 8 different repetition periods.
- Three General Purpose Outputs (hereafter GPO), programmable through the serial interface. The GPO are open drain NMOST outputs, capable of handling the full battery voltage range and high sink currents.

The GPO's can be programmed to be continuously active low or tristate. In addition the GPO outputs can be controlled by the LED or PWM modulators.

- Watchdog timer that can be activated by software.

2.2 Supply voltage generation

- The power supplies have programmable activity modes (OFF, ECO, ON). In the ACTIVE state, the operation modes can be selected by the two external pins PWREN1 and PWREN2.
- One charge pump with programmable output voltage for the supply of white or blue LED's (hereafter CP).
- Two 100 mA LDO voltage regulators with fixed output voltage (mask programmable) for RF supplies. Regulators are optimized for low noise, high power supply rejection, and excellent load regulation (hereafter RF1REG, RF2REG).
- Two 150 mA LDO voltage regulators that are optimized for small external capacitors (hereafter D1REG, D2REG). D1REG provides a programmable output voltage, D2REG provides a fixed output voltage (mask programmable).
- One 150 mA LDO voltage regulator dedicated for the supply of the IO pads. This regulator has a fixed output voltage (mask programmable) and is optimized for a small external capacitor (hereafter IOREG).
- One 100 mA LDO voltage regulator with fixed output voltage (mask programmable). In its ECO mode (low power operation mode), it can be used to permanently supply parts in the system in all activity states (hereafter LPREG).
- One 100 mA LDO voltage regulator with programmable output voltage. This regulator is optimized for a small external capacitor (hereafter D3REG).
- One 250 mA LDO voltage regulator with programmable output voltage. This high current regulator is optimized for applications like hands-free audio (hereafter HCREG).
- D1REG, D2REG, D3REG, IOREG, and LPREG support a low power operation mode (hereafter ECO mode). In this mode, the output power is limited to 1 mA and the internal power consumption is reduced significantly.
- Microphone bias voltage generator with low noise, and high power supply rejection (MBGEN).
- The temperature high sensor (hereafter TS) provides thermal protection for the whole chip.
- Enhanced ESD protection on all pins that connect to the main battery pack.

2.3 Battery management

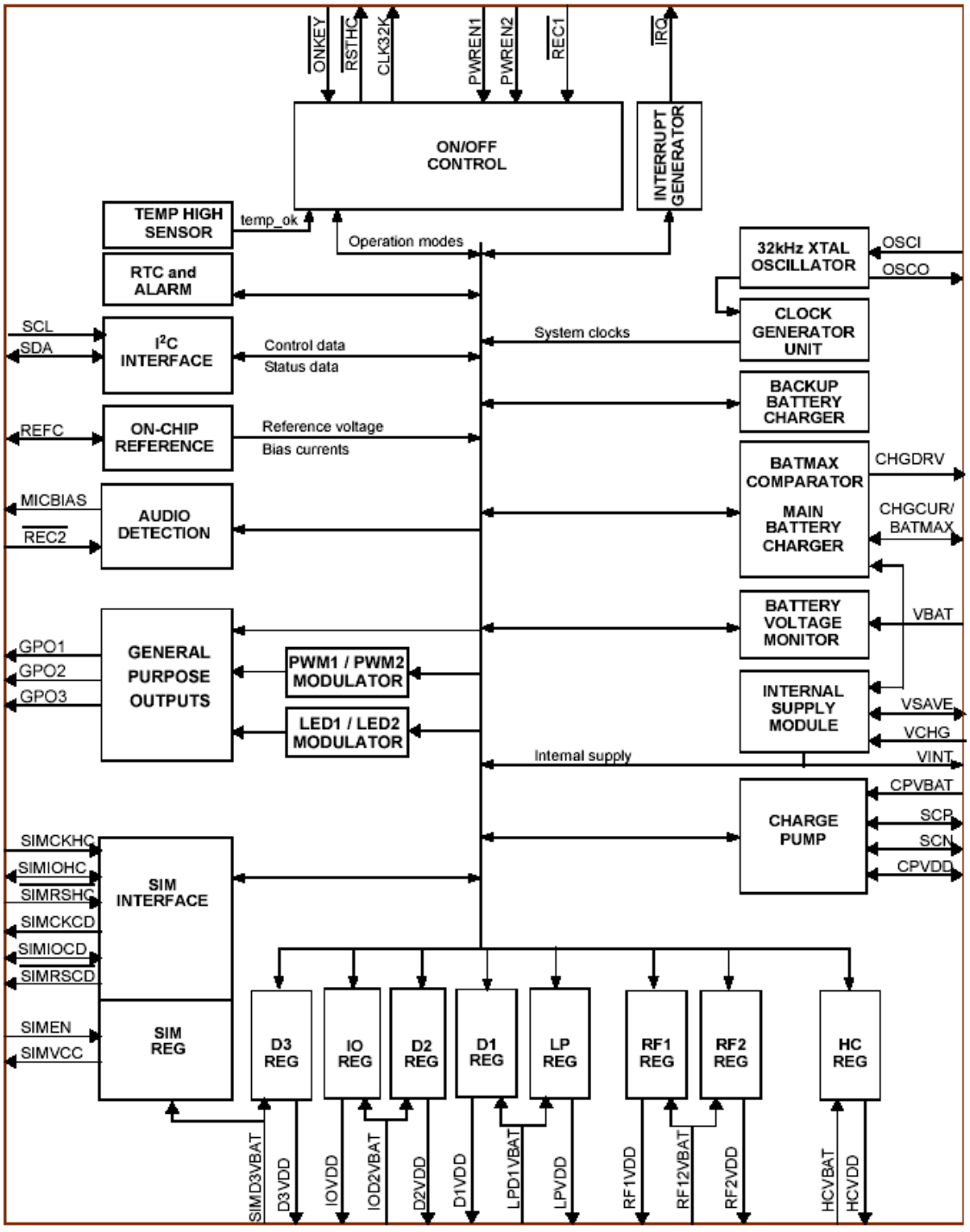
- The PCF50603 operates from a 3 cell NiCd/NiMH or a 1 cell LiIon battery pack.
- Battery voltage monitor (hereafter BVM) to detect a too low main battery voltage with programmable threshold levels. A low battery condition is reported via the interrupt mechanism.
- Charger control: option between two different charger control functions, depending on the configuration:
  - Configuration CCCV: Constant Current Constant Voltage (hereafter CCCV) linear charger control supporting LiIon as well as NiCd/NiMH battery types for a wide range of battery capacities.

- Configuration BATMAX: comparator that compares the battery voltage against a programmable threshold voltage. This function can be activated by software and is used to detect the end-of-charge.

- The PCF50603 supports the use of a backup battery that powers the PCF50603 at empty main battery situations. The backup battery is used to supply the real-time clock, the internal state, and the LPVDD supply in its ECO mode. Goldcaps, Li and LiIon cells are supported.
- Includes a backup battery charger (hereafter BBC). A rechargeable backup battery or backup capacitor can be charged from the main battery. For charging, a programmable constant voltage mode is supported.

2.4 Subscriber Identity Module card interface

- The Subscriber Identity Module card interface (hereafter SIMI) supports two different modes that can be selected:
  - Transparent interface including an arbiter and signal level translators.
  - SIM card interface with integrated sequencer, arbiter and signal level translators. The sequencer supports and controls card activation and de-activation, warm reset, and controlled clock stop for power down modes.
- Dedicated SIM supply (hereafter SIMREG) that supports 3.0 V and 1.8 V cards. Including a power saving ECO mode for the power down mode of the SIM card.
- Enhanced ESD protection on all pins that connect to the SIM card contact pins.



g 1. Functional Diagram PCF50603

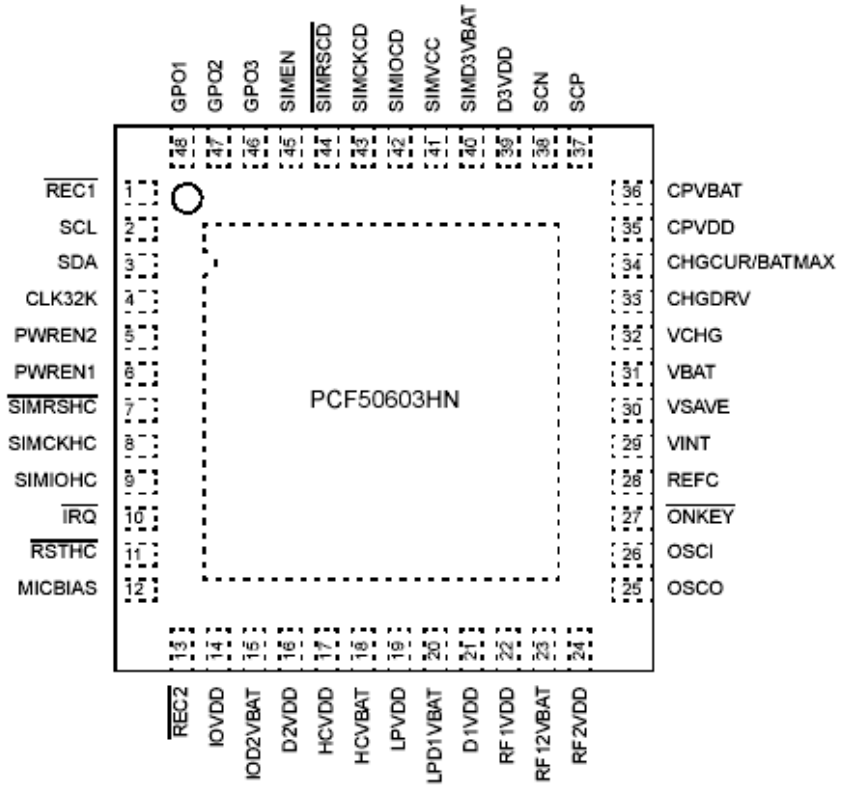
Table 6: Pin description...*continued*

Symbol	HVQFN48 Pin no	Supply	Description/Remarks
CLK32K	4	IOVDD	32.768 kHz digital clock output; note that this output is only available when the system is in ACTIVE state and IOVDD is on.[1]
PWREN1	6	IOVDD	Control signal selects in combination with PWREN2 the ON, OFF or ECO mode of the linear regulators.[1]
PWREN2	5	IOVDD	Control signal selects in combination with PWREN1 the ON, OFF or ECO mode of the linear regulators.[1]
$\overline{IRQ}$	10	IOVDD	Interrupt request to host controller; this low active signal is realized as an open drain output with an internal pull-up resistor to IOVDD.[1]
$\overline{REC1}$	1	VINT	Accessory recognition input with debounce filter. Input with internal pull-up resistor to VINT.[1]
$\overline{REC2}$	13	MICBIAS	Accessory recognition input with debounce filter and programmable threshold.[1]
Charge Pump			
CPVBAT	36	n.a.	Input for charge pump[1]
SCP	37	n.a.	Switching capacitor positive side[1]
SCN	38	n.a.	Switching capacitor negative side[1]
CPVDD	35	n.a.	Charge pump output voltage[1]
Linear regulators			
RF12VBAT	23	n.a.	Shared input for RF1 and RF2 linear regulators[1]
RF1VDD	22	n.a.	RF1 linear regulator output voltage[1]
RF2VDD	24	n.a.	RF2 linear regulator output voltage[1]
IOD2VBAT	15	n.a.	Shared input for IO and D2 linear regulator [1]
IOVDD	14	n.a.	IO linear regulator output voltage[1]
D2VDD	16	n.a.	Digital 2 linear regulator output voltage[1]
SIMD3VBAT	40	n.a.	Shared input for D3 and SIM linear regulators[1]
D3VDD	39	n.a.	Digital 3 linear regulator output voltage[1]
LPD1VBAT	20	n.a.	Shared input for D1 and LP linear regulators[1]
LPVDD	19	n.a.	Low-power linear regulator output voltage[1]
D1VDD	21	n.a.	Digital 1 linear regulator output voltage[1]
HCVBAT	18	n.a.	Input for high current linear regulator[1]
HCVDD	17	n.a.	High current linear regulator output voltage[1]
32.768 kHz oscillator			
OSCI	26	VINT	32.768 kHz oscillator input[1]
OSCO	25	VINT	32.768 kHz oscillator output[1]
Internal supply			
VBAT	31	n.a.	Main battery connection[1]
VSAVE	30	n.a.	Backup battery connection[1]
VCHG	32	n.a.	Charger connection[2]
VINT	29	n.a.	Internal supply voltage output[1]
On-chip reference and microphone bias generator			

Table 6: Pin description...continued

Symbol	HVQFN48 Pin no	Supply	Description/Remarks
REFC	28	n.a.	Reference voltage bypass capacitor connection [1]
MICBIAS	12	n.a.	Microphone bias voltage output [1]
I²C interface			
SCL	2	IOVDD	I²C clock [1]
SDA	3	IOVDD	I²C data [1]
SIM interface & supply			
SIMEN	45	IOVDD	Enable of the SIM interface & SIM supply [1]
SIMVCC	41	n.a.	SIM supply [1]
SIMCKHC	8	IOVDD	SIM clock from host controller [1]
$\overline{\text{SIMRSHC}}$	7	IOVDD	Active low SIM reset from host controller [1]
SIMIOHC	9	IOVDD	SIM IO data to/from the host controller Internal pull-up resistor to IOVDD [1]
SIMCKCD	43	SIMVCC	SIM clock to the SIM card [1]
$\overline{\text{SIMRSCD}}$	44	SIMVCC	Active low SIM reset to the SIM card [1]
SIMIOCD	42	SIMVCC	SIM IO data to/from the SIM card. Internal pull-up resistor to SIMVCC [1]
Battery charging control			
CHGDRV	33	n.a.	Drive of external charger circuitry (configuration CCCV). [1]
CHGCUR	34	n.a.	Charger current feedback (configuration CCCV). [1]
BATMAX	34	n.a.	Open drain output of BATMAX comparator (configuration BATMAX). [1]
Pulse-width modulator & LED driver			
GPO1	48	n.a.	General purpose open drain output [1]
GPO2	47	n.a.	General purpose open drain output [1]
GPO3	46	n.a.	General purpose open drain output [1]
Ground			
VSS & REFGND		n.a.	The ground and VSS pins of all modules are connected to the ground plane of the package.

$\overline{\text{SLPMOD}}$	D5	DVDD1	Signal switches the system to SLEEP state. At start up this signal is ignored until enabled by the system controller (see OOCC2 register).
TM	F5	ISUPD	Test mode selection; shall be connected to ground for normal operation.
$\overline{\text{RSTO}}$	D6	DVDD1	Active-low reset for logic supplied by DVDD1
$\overline{\text{ONKEY}}$	F4	ISUPD	Active Low On-key input with debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Edge sensitive input.
$\overline{\text{AUXON}}$	G4	ISUPD	Active Low Auxiliary On-Key input with 62 msec debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Level sensitive input.
CLK32	B8	DVDD1	32.768 kHz digital clock output; note that this output is only available when system is in ACTIVE or SLEEP state and DVDD1 is on.
$\overline{\text{INT}}$	D7	DVDD1	Interrupt to system controller; this active low signal is realized as an open drain output. Requires external pull-up resistor.
REC1	J2	DVDD2	Accessory recognition with interrupt; these inputs have selectable debounce filters (0, 14 or 62 ms) to prevent multiple interrupt generation
REC2	H3	DVDD2	
REC3	G3	DVDD2	



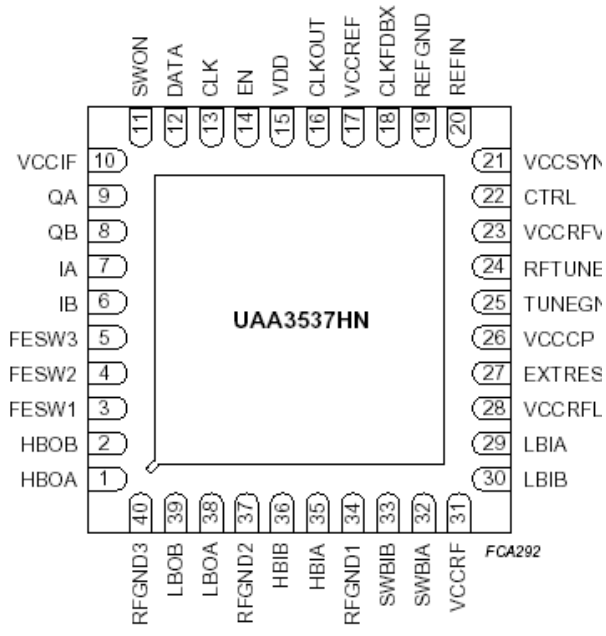
(1) This diagram is a TOP side (or die side) view.

6.3 Transceiver (UAA3537HN)

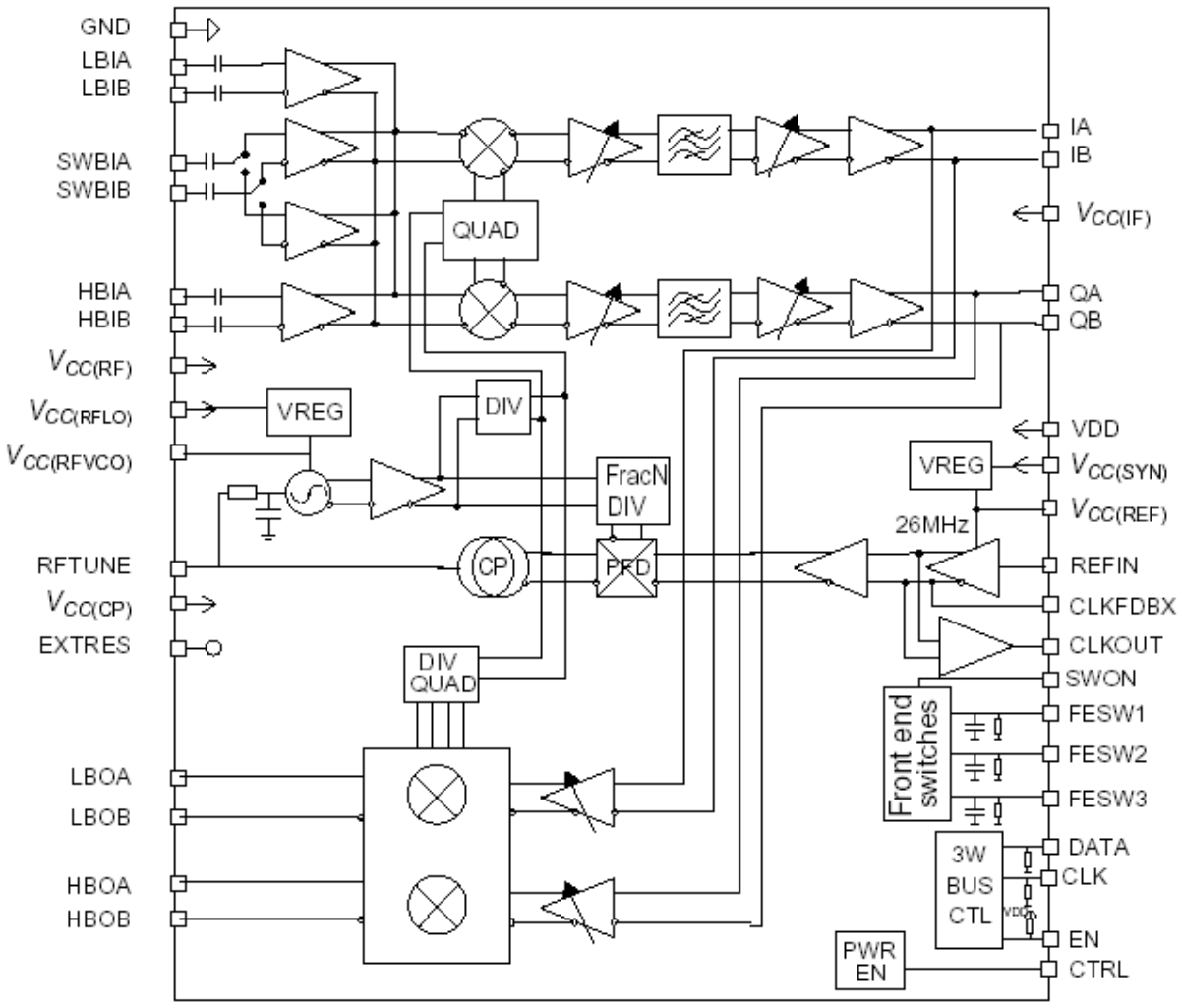
The UAA3537 is a fully-integrated GSM hand-held transceiver

Features

- Multiple band application within the 850, 900, 1800 and 1900 MHz frequency bands.
- Low noise and wide dynamic range low IF receiver
- GPRS multi slot class 12 capable
- More than 35 dB on chip image rejection in receive
- More than 68 dB gain control range in receive
- Direct-up conversion in transmit
- Fully-integrated fractional-N RF-synthesizer with AFC control possibility
- Fully-integrated RF VCO with integrated supply regulator
- semi-integrated reference oscillator with integrated supply regulator
- Fully differential design to minimize cross-talk and spurs
- Functional down to 2.4 V and up to 3.0 V
- Three output to control RF frontend switches (pin diodes)
- 3-wire serial bus interface
- HVQFN40 package



configuration (bottom view).



7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
HBOA	1	DCS1800 and PCS1900 bands RF output
HBOB	2	DCS1800 and PCS1900 bands RF output
FESW1	3	front end switch control output
FESW2	4	front end switch control output
FESW3	5	front end switch control output
IB	6	baseband input-output; I path

Table 3: Pin description...*continued*

Symbol	Pin	Description
IA	7	baseband input-output; I path
QB	8	baseband input-output; Q path
QA	9	baseband input-output; Q path
$V_{CC(IF)}$	10	IF supply
SWON	11	front end switch control input
DATA	12	3-wire bus; DATA input
CLK	13	3-wire bus; CLK input
EN	14	3-wire bus; ENABLE control pin
VDD	15	digital supply
CLKOUT	16	reference oscillator output
$V_{CC(REF)}$	17	reference regulator output and reference supply
CLKFDBX	18	reference oscillator feedback
REFGND	19	GND for reference oscillator
REFIN	20	reference oscillator input
$V_{CC(SYN)}$	21	synthesizer and reference regulator supply
CTRL	22	global enable control pin
$V_{CC(RFVCO)}$	23	RFVCO regulator output and RF VCO supply
RFTUNE	24	tuning input of RF VCO
TUNEGND	25	ground for RF VCO tuning
$V_{CC(CP)}$	26	RF charge pump supply
EXTRES	27	reference resistor for RF PLL charge pump gains
$V_{CC(RFLO)}$	28	RF LO and RFVCO regulator supply
LBIA	29	receiver GSM850/900 RF input
LBIB	30	receiver GSM850/900 RF input
$V_{CC(RF)}$	31	RF front end and transmit part supply
SWBIA	32	receiver DCS1800/PCS1900 or GSM850/900 switched RF input
SWBIB	33	receiver DCS1800/PCS1900 or GSM850/900 switched RF input
RFGND1	34	ground for front end
HBIA	35	receiver DCS1800 or PCS1900 bands RF input
HBIB	36	receiver DCS1800 or PCS1900 bands RF input
RFGND2	37	ground for front end
LBOA	38	GSM850 and GSM900 RF output
LBOB	39	GSM850 and GSM900 RF output
RFGND3	40	ground for front end

6.4 PA&PAC (SKY77324)

The SKY77324 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 Ω input and output impedances, and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom CMOS integrated circuit provides the internal PAC function and interface circuitry. Fabricated onto a single Gallium Arsenide (GaAs) die, one Heterojunction Bipolar Transistor (HBT) PA block supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

FEATURES

- Low input power range
  - 0 to 6 dBm
- High efficiency
  - GSM850 49%
  - GSM900 53%
  - DCS 53%
  - PCS 53%
- Internal I_{CC} sense resistor for PAC
- Closed loop iPAC or open loop operation with external PAC circuit
- Input/Output matching 50 Ω internal (with DC blocking)
- 22-pin package
- Small outline:
  - 6 mm x 8 mm
- Low profile
  - 1.2 mm maximum
- Low APC current
  - 20 µA
- Gold plated, lead-free contacts

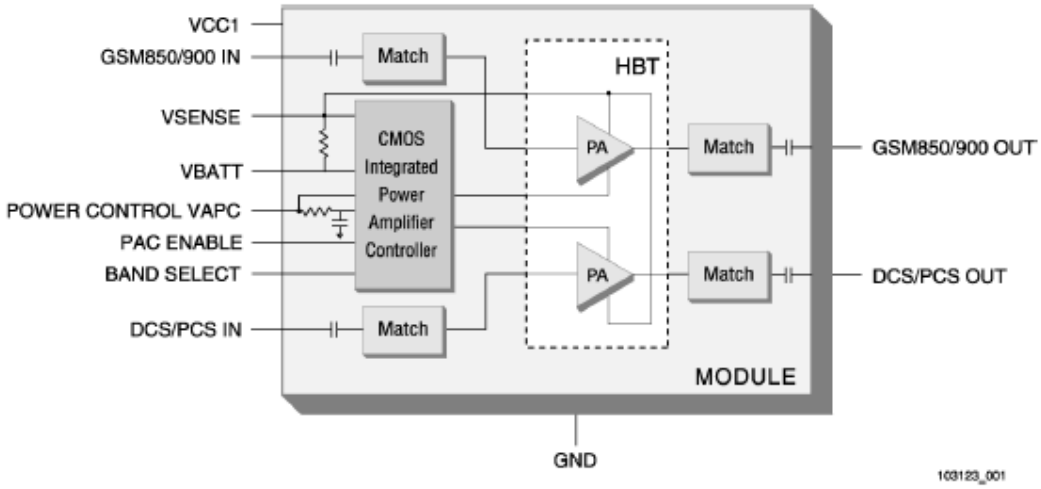


Figure 1. Functional Block Diagram

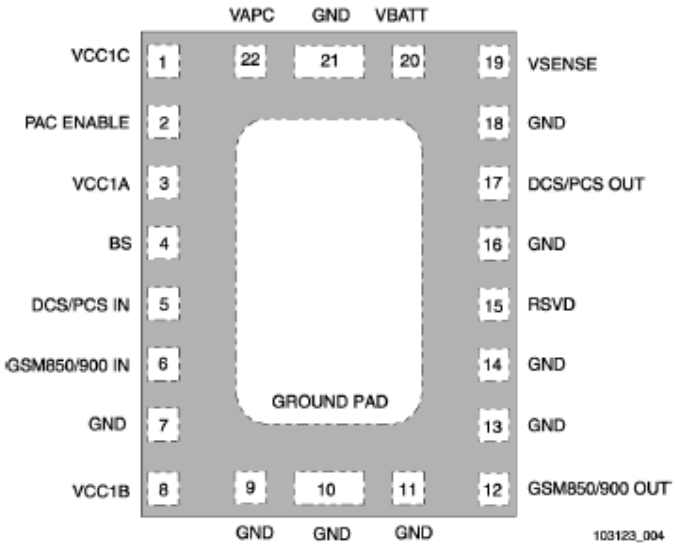


Figure 5. SKY77324 PAM Pin Configuration—22-Pin Leadless (Top View)

Table 4. SKY77324 Pin Names and Signal Descriptions

Pin	Name	Description
1	VCC1C	VCC (to PAC)
2	PAC ENABLE	Closed loop PAC mode CMOS enable
3	VCC1A	VCC (to GSM 1st stage, DCS 1st stages)
4	BS	Band Select
5	DCS/PCS IN	RF input 1710–1910 MHz
6	GSM850/900 IN	RF input 824–915 MHz
7	GND	RF and DC Ground
8	VCC1B	VCC (to GSM 2nd stage, DCS 2nd stage)
9	GND	RF and DC Ground
10	GND	RF and DC Ground
11	GND	RF and DC Ground
12	GSM850/900 OUT	RF Output 824–915 MHz
13	GND	RF and DC Ground
14	GND	RF and DC Ground
15	RSVD	Reserved
16	GND	RF and DC Ground
17	DCS/PCS OUT	RF Output 1710–1910 MHz
18	GND	RF and DC Ground
19	VSENSE	Voltage output of low side of internal sense resistor (DO NOT CONNECT IN CLOSED LOOP MODE.)
20	VBATT	Battery input to high side of internal sense resistor
21	GND	RF and DC Ground
22	VAPC	Power Control Bias Voltage
GND PAD (23)	GND	Ground Pad, bottom

6.5 CAMERA &LCD CONTROL IC(BU1594GS)

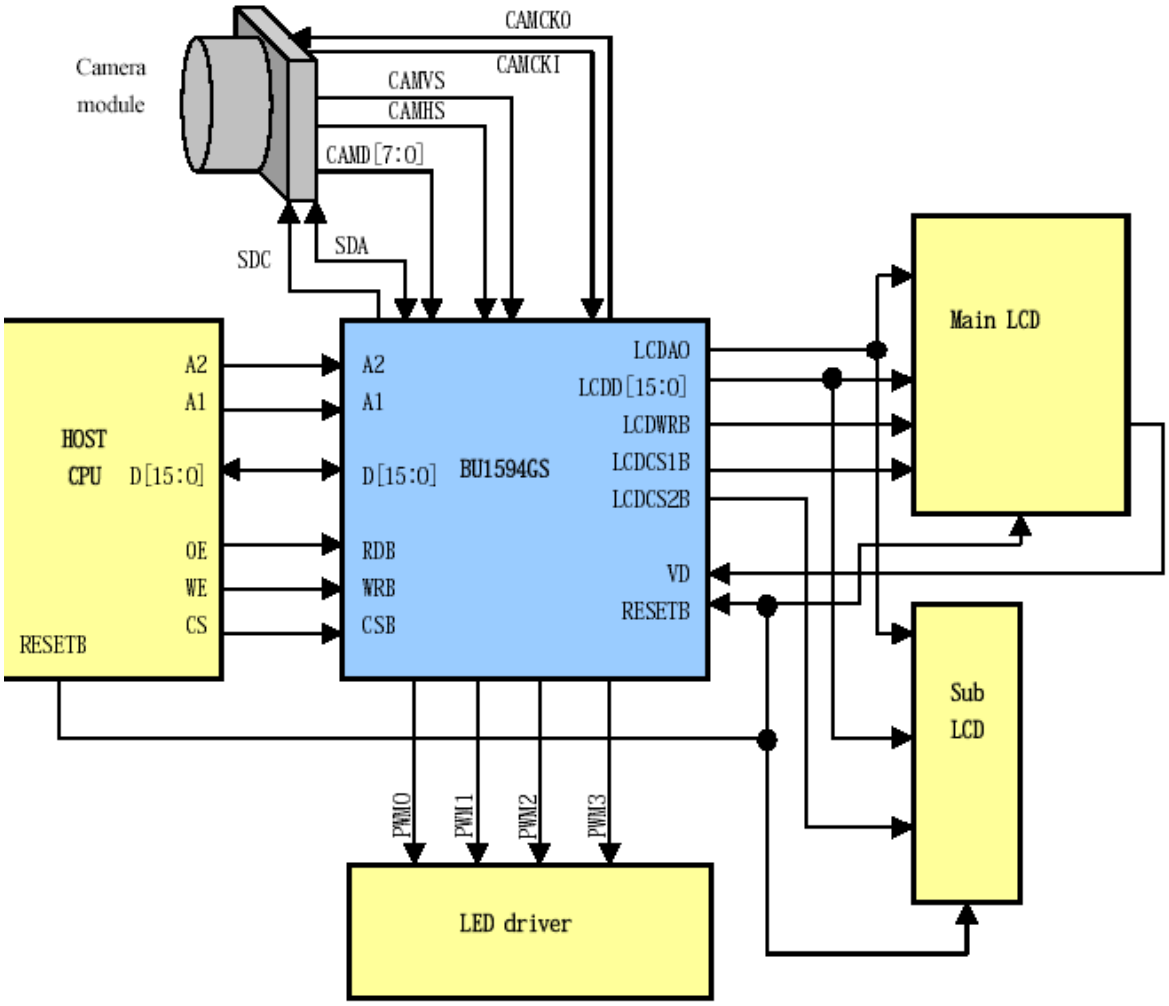


Fig.4-1 BU1594GS system connection diagram

1.5. BU1594GS Block Diagram

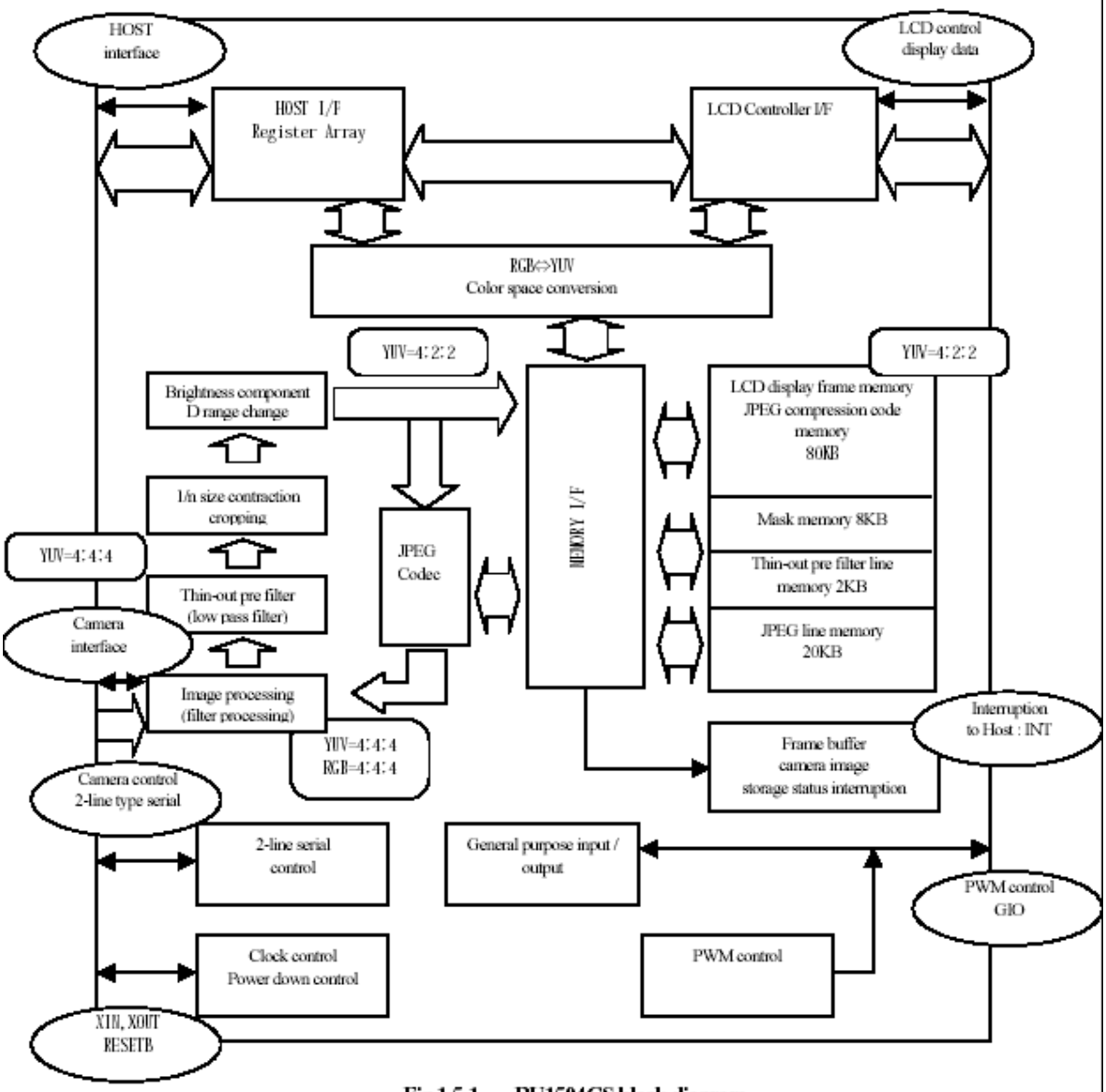


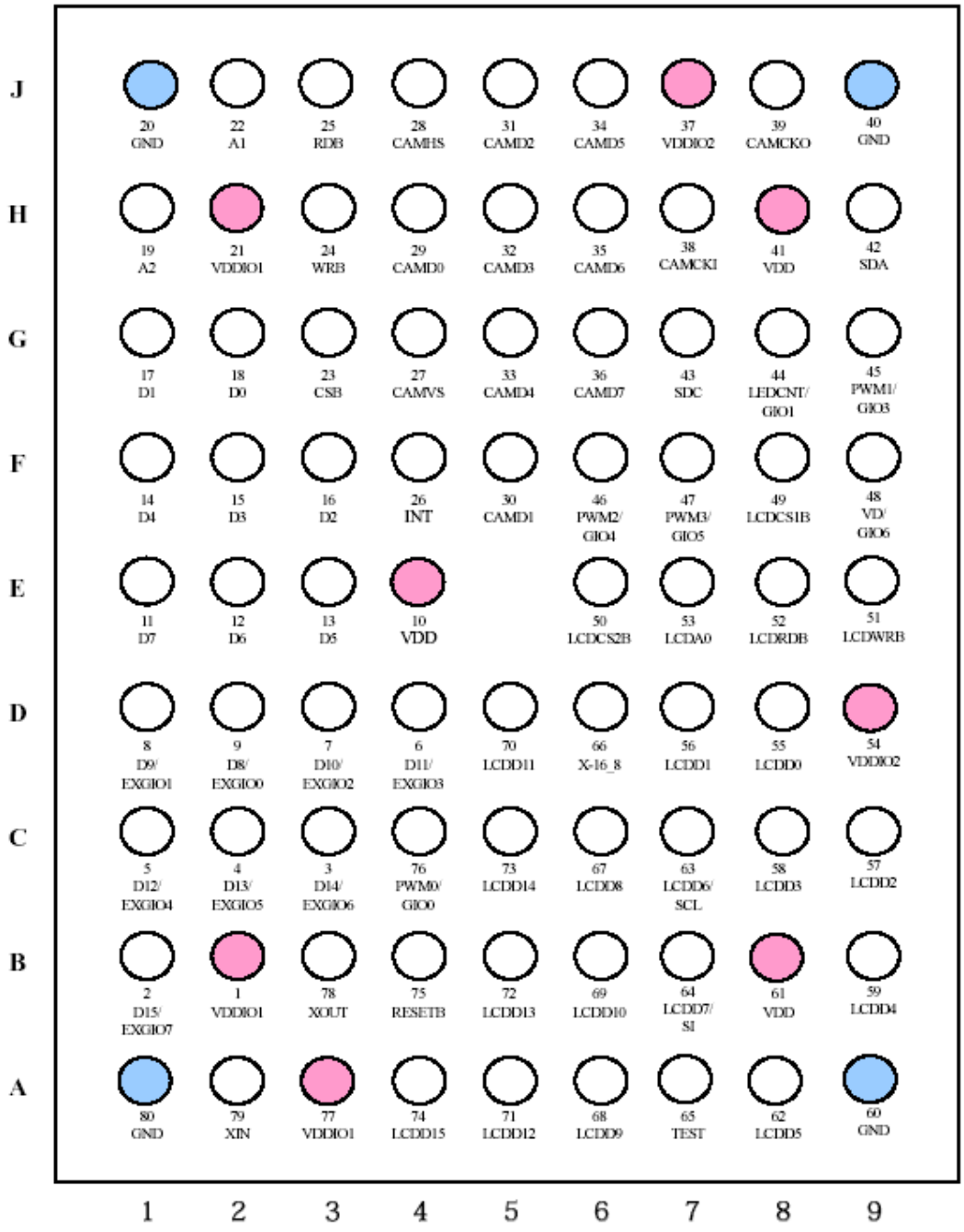
Fig.1.5-1. BU1594GS block diagram

Table 1.6-1 Table of BU1594GS terminal functions (1)

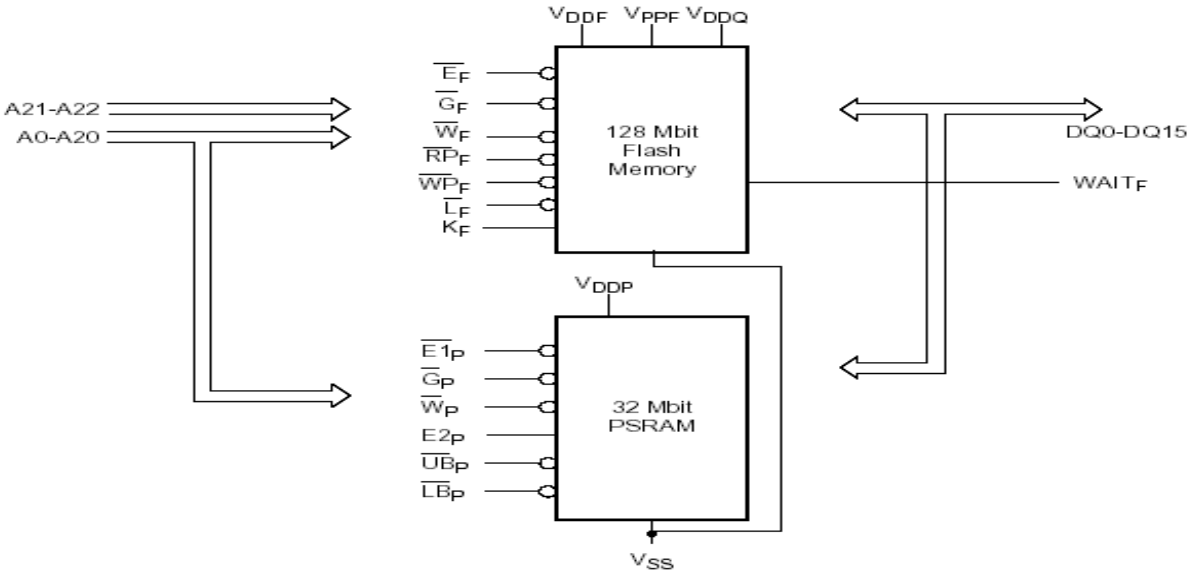
No.	Ball	PIN Name	In/Out	Active	Init	Function explanation	Function division	I/O
1	B2	VDDIO1	--	PWR	--	Digital I/O power source (system 1)	--	--
2	B1	D15/EXGIO7	In/Out	DATA	In *1	Host data bus bit 15	HOST IF	H
3	C3	D14/EXGIO6	In/Out	DATA	In *1	Host data bus bit 14	HOST IF	H
4	C2	D13/EXGIO5	In/Out	DATA	In *1	Host data bus bit 13	HOST IF	H
5	C1	D12/EXGIO4	In/Out	DATA	In *1	Host data bus bit 12	HOST IF	H
6	D4	D11/EXGIO3	In/Out	DATA	In *1	Host data bus bit 11	HOST IF	H
7	D3	D10/EXGIO2	In/Out	DATA	In *1	Host data bus bit 10	HOST IF	H
8	D1	D9/EXGIO1	In/Out	DATA	In *1	Host data bus bit 9	HOST IF	H
9	D2	D8/EXGIO0	In/Out	DATA	In *1	Host data bus bit 8	HOST IF	H
10	E4	VDD	--	PWR	--	Digital core power source	--	--
11	E1	D7	In/Out	DATA	In *1	Host data bus bit 7	HOST IF	G
12	E2	D6	In/Out	DATA	In *1	Host data bus bit 6	HOST IF	G
13	E3	D5	In/Out	DATA	In *1	Host data bus bit 5	HOST IF	G
14	F1	D4	In/Out	DATA	In *1	Host data bus bit 4	HOST IF	G
15	F2	D3	In/Out	DATA	In *1	Host data bus bit 3	HOST IF	G
16	F3	D2	In/Out	DATA	In *1	Host data bus bit 2	HOST IF	G
17	G1	D1	In/Out	DATA	In *1	Host data bus bit 1	HOST IF	G
18	G2	D0	In/Out	DATA	In *1	Host data bus bit 0	HOST IF	G
19	H1	A2	In	DATA	--	Host address bus bit 2	HOST IF	A
20	J1	GND	--	GND	--	Common ground	--	--
21	H2	VDDIO1	--	PWR	--	Digital I/O power source (system 1)	--	--
22	J2	A1	In	DATA	--	Host address bus bit 1	HOST IF	A
23	G3	CSB	In	Low	--	Chip select signal	HOST IF	C
24	H3	WRB	In	Low	--	Write enable signal	HOST IF	C
25	J3	RDB	In	Low	--	Output enable signal	HOST IF	C
26	F4	INT	Out	High	Low	Interruption signal	HOST IF	E
27	G4	CAMVS	In	*	--	Camera vertical timing signal (pull down at CAMOFF)	CAMERA	B
28	J4	CAMHS	In	*	--	Camera horizontal timing signal (pull down at CAMOFF)	CAMERA	B
29	H4	CAMD0	In	DATA	--	Camera data input / bit 0 (pull down at CAMOFF)	CAMERA	B
30	F5	CAMD1	In	DATA	--	Camera data input / bit 1 (pull down at CAMOFF)	CAMERA	B
31	J5	CAMD2	In	DATA	--	Camera data input / bit 2 (pull down at CAMOFF)	CAMERA	B
32	H5	CAMD3	In	DATA	--	Camera data input / bit 3 (pull down at CAMOFF)	CAMERA	B
33	G5	CAMD4	In	DATA	--	Camera data input / bit 4 (pull down at CAMOFF)	CAMERA	B
34	J6	CAMD5	In	DATA	--	Camera data input / bit 5 (pull down at CAMOFF)	CAMERA	B
35	H6	CAMD6	In	DATA	--	Camera data input / bit 6 (pull down at CAMOFF)	CAMERA	B
36	G6	CAMD7	In	DATA	--	Camera data input / bit 7 (pull down at CAMOFF)	CAMERA	B
37	J7	VDDIO2	--	PWR	--	Digital IO power source (system 2)	--	--
38	H7	CAMCKI	In	CLK	--	Camera clock input (pull down at CAMOFF)	CAMERA	B
39	J8	CAMCKO	Out	CLK	Low	Camera clock output	CAMERA	E
40	J9	GND	--	GND	--	Common ground	--	--

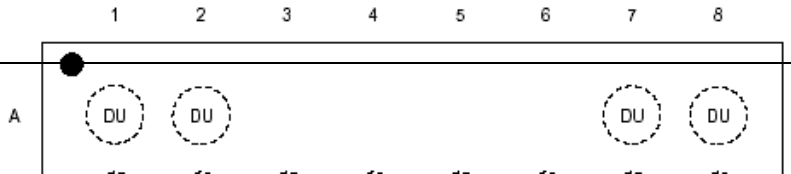
Table 1.6-2 BU1594GS terminal functions (2)

No.	Ball	PIN Name	In/Out	Active	Init	Function explanation	Function division	I/O
41	H8	VDD	--	PWR	–	Digital core power source	--	--
42	H9	SDA	In/Out	DATA	Out/Low	Serial control input / output (pull up at input)	CAMERA	J
43	G7	SDC	In/Out	CLK	Out/Low	Serial clock output (always pull up OFF)	CAMERA	J
44	G8	LEDCNT/GIO	In/Out	*	In	LED PWM control signal / general purpose input / output from sound source	SYSTEM	H
45	G9	PWM1/GIO3	In/Out	--	Low	LED PWM control signal	SYSTEM	H
46	F6	PWM2/GIO4	In/Out	--	Low	LED PWM control signal	SYSTEM	H
47	F7	PWM3/GIO5	In/Out	High	Low	LED PWM control signal	SYSTEM	H
48	F9	VD/GIO6	In	*	–	LCD controller vertical synchronization signal	LCD IF	H
49	F8	LCDCS1B	Out	Low	High	LCD controller chip select 1	LCD IF	E
50	E6	LCDCS2B	Out	Low	High	LCD controller chip select 2	LCD IF	E
51	E9	LCDWRB	Out	Low	Low	LCD controller write enable signal	LCD IF	G *2
52	E8	LCDRDB	Out	Low	Low	LCD controller read enable signal	LCD IF	G *2
53	E7	LCDA0	Out	*	Low	LCD controller command parameter identification	LCD IF	G *2
54	D9	VDDIO2	--	PWR	–	Digital IO power source (system 2)	--	--
55	D8	LCDD0	In/Out	DATA	Low	LCD controller data bus / bit 0	LCD IF	H
56	D7	LCDD1	In/Out	DATA	Low	LCD controller data bus / bit 1	LCD IF	H
57	C9	LCDD2	In/Out	DATA	Low	LCD controller data bus / bit 2	LCD IF	H
58	C8	LCDD3	In/Out	DATA	Low	LCD controller data bus / bit 3	LCD IF	H
59	B9	LCDD4	In/Out	DATA	Low	LCD controller data bus / bit 4	LCD IF	H
60	A9	GND	--	GND	–	Common ground	--	--
61	B8	VDD	--	PWR	–	Digital core power source	--	--
62	A8	LCDD5	In/Out	DATA	Low	LCD controller data bus / bit 5	LCD IF	H
63	C7	LCDD6/SCL	In/Out	DATA	Low	LCD controller data bus / bit 6	LCD IF	H
64	B7	LCDD7/SI	In/Out	DATA	Low	LCD controller data bus / bit 7	LCD IF	H
65	A7	TEST	In	Low	–	Test mode terminal (connected to GND)	SYSTEM	B
66	D6	X16_8	In	--	–	Host data bus 16-bit / 8-bit selection	SYSTEM	A
67	C6	LCDD8	In/Out	DATA	Low	LCD controller data bus / bit 8	LCD IF	H
68	A6	LCDD9	In/Out	DATA	Low	LCD controller data bus / bit 9	LCD IF	H
69	B6	LCDD10	In/Out	DATA	Low	LCD controller data bus / bit 10	LCD IF	H
70	D5	LCDD11	In/Out	DATA	Low	LCD controller data bus / bit 11	LCD IF	H
71	A5	LCDD12	In/Out	DATA	Low	LCD controller data bus / bit 12	LCD IF	H
72	B5	LCDD13	In/Out	DATA	Low	LCD controller data bus / bit 13	LCD IF	H
73	C5	LCDD14	In/Out	DATA	Low	LCD controller data bus / bit 14	LCD IF	H
74	A4	LCDD15	In/Out	DATA	Low	LCD controller data bus / bit 15	LCD IF	H
75	B4	RESETB	In	Low	–	System reset signal	SYSTEM	C
76	C4	PWM0/GIO0	In/Out	DATA	In	LED PWM control signal / general purpose input / output	SYSTEM	H
77	A3	VDDIO1	--	PWR	–	Digital IO power source (system 1)	--	--
78	B3	XOUT	Out	CLK	High	Clock output (always HIGH output at setting of external input)	SYSTEM	I
79	A2	XIN	In	CLK	–	Clock input *3	SYSTEM	C,I
80	A1	GND	--	GND	–	Common ground	--	--


J
20 GND
22 A1
25 RDB
28 CAMHS
31 CAMD2
34 CAMD5
37 VDDIO2
39 CAMCKO
40 GND
H
19 A2
21 VDDIO1
24 WRB
29 CAMD0
32 CAMD3
35 CAMD6
38 CAMCKI
41 VDD
42 SDA
G
17 D1
18 D0
23 CSB
27 CAMVS
33 CAMD4
36 CAMD7
43 SDC
44 LEDCNT/ GIO1
45 PWM1/ GIO3
F
14 D4
15 D3
16 D2
26 INT
30 CAMD1
46 PWM2/ GIO4
47 PWM3/ GIO5
49 LCDCS1B
48 VD/ GIO6
E
11 D7
12 D6
13 D5
10 VDD
50 LCDCS2B
53 LCDA0
52 LCDRDB
51 LCDWRB
D
8 D9/ EXGIO1
9 D8/ EXGIO0
7 D10/ EXGIO2
6 D11/ EXGIO3
70 LCDD11
66 X-16_8
56 LCDD1
55 LCDD0
54 VDDIO2
C
5 D12/ EXGIO4
4 D13/ EXGIO5
3 D14/ EXGIO6
76 PWM0/ GIO0
73 LCDD14
67 LCDD8
63 LCDD6/ SCL
58 LCDD3
57 LCDD2
B
2 D15/ EXGIO7
1 VDDIO1
78 XOUT
75 RESETB
72 LCDD13
69 LCDD10
64 LCDD7/ SI
61 VDD
59 LCDD4
A
80 GND
79 XIN
77 VDDIO1
74 LCDD15
71 LCDD12
68 LCDD9
65 TEST
62 LCDD5
60 GND
1 2 3 4 5 6 7 8 9

6.6 MEMORY (M36L0R7050T0ZAQT/STM)





6.1.7 MELODY IC(ML2864)

ML2864 DATA SHEET

16-Tone, 64-Poly Hi-Grade PCM Sound Generator LSI

Version : 1.0.0 Rivised on Saturday, August 30, 2003

GENERAL DESCRIPTION

ML2864 is a PCM-based hi-grade sound generator LSI, developed specifically for music ringers used in cellular/PHS phones, and plays 16 tones and 64 polyphonies simultaneously. It also has hi-grade 175 polyphonies based on General MIDI system level 1, the standard spec for PCM sound generator.

ML2864 plays standard MIDI file which is standard spec of MIDI file. It is optimum sound generator to connect to the Internet and for BGM on browser.

The on-chip FIFOs and sequencer reduce the CPU power. ML2864 is also embedded 2bit/4bit ADPCM, 8bit/16bit PCM for sound effect and LED driver with brightness-control function. It is easy to build the high quality music ringer subsystem.

FEATURES

1) On-chip high-quality GM sound set

2) 16 timbre and 64 polyphonies simultaneously

3) Ports

Vibrator direct driver – one port

LED direct driver with PWM – four ports

LED direct driver for Front LCD panel – one port

External I/O port (depending on package type)

W-CSP: 5 ports (P4-0)

4) 3 or 4-pin serial interface or 8bit bus interface selectable

5) On-chip FIFO buffer memory

1024bit(128Byte) FIFO for musical score data

128bit(16Byte) FIFO for MIDI messages

4096bit(512Byte) FIFO for ADPCM audio synthesis

6) Low power consumption at power-down: Idds = 1μA (typ.)

Operating current: 60mA (max.)

7) Power Supply: +2.7 V ~ 3.6 V

8) Package options

49-pin W-CSP (P-VFLGA49-4.91X4.91 –0.65-W)

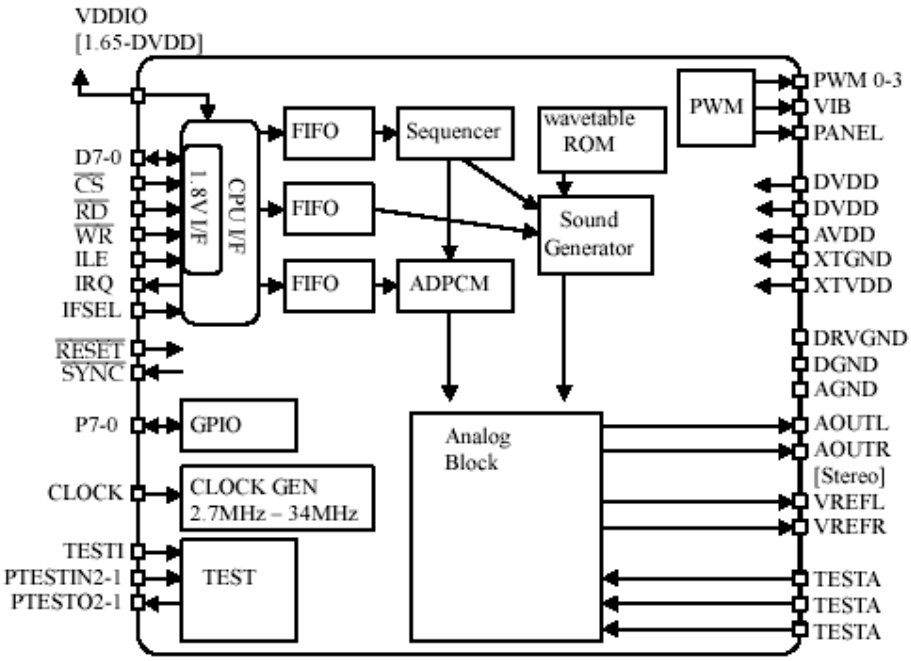
9) Operating Temperature: -20 ~ +85°C

10) Ordering part number :

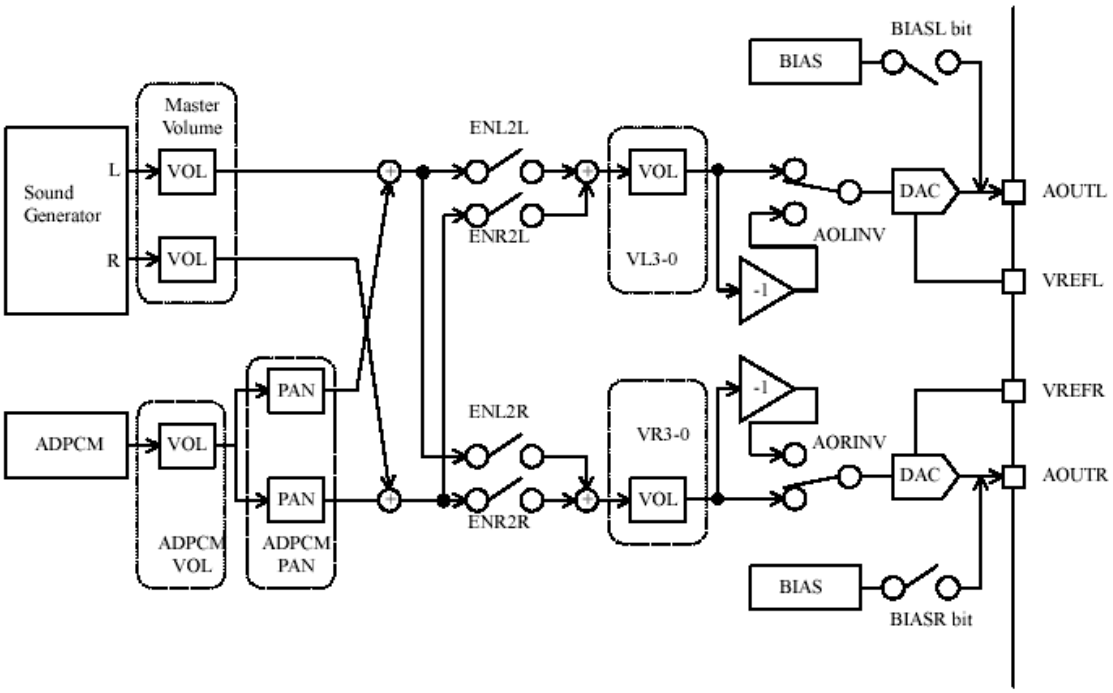
49-pin WCSP : ML2864HB Z060 (PbSn, Tape & Reel)

ML2864HB Z03B (Lead Free, Tape & Reel)

BLOCK DIAGRAM [LOGIC PART]

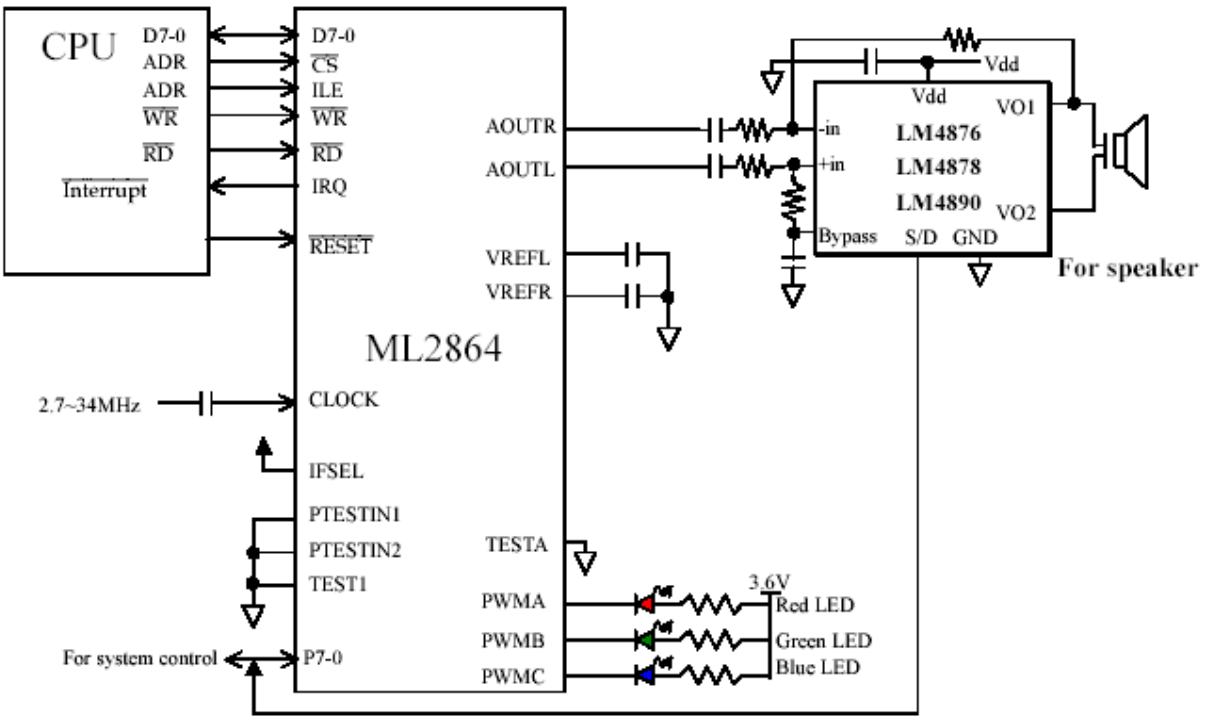


BLOCK DIAGRAM [ANALOG PART]



	G	F	E	D	C	B	A
7	PTESTIN1	VDDIO	DGND	D3/ARQ	D6/DIPH	$\overline{RD}$	PTESTO2
6	CLOCK	XTGND	D0/SDIN	D1/SDOUT	D4/SRQ	$\overline{CS}$	AGND
5	XTVDD	P0	TESTI	D2/SCLK	$\overline{WR}$	AOUTR	AOUTL
4	P2	P1	PWMA	D5/ERQ	ILE	VREFR	VREFL
3	P4	P3	PWMB	D7	TESTA	TESTA	AVDD
2	VIB	PANEL	PWMD	IRQ	TESTA	SYNC	IFSEL
1	PTESTO1	DrvGND	PWMC	DVDD	TESTI	$\overline{RESET}$	PTESTIN2

Bottom View



6.1.8 Charge Management IC(UBA2008)

The UBA2008 is an intelligent charge switch IC for pulse mode charging applications. With its integrated low-ohmic power switch it is designed for charging of 1-cell LiIon or 3-cell NiMH batteries in either a pre-charge or fast charge mode. The reverse mode of the UBA2008 allows the supply of accessories connected to the charger pin. Several integrated safety mechanisms such as current limitation, over-voltage protection, thermal protection, and ESD guarantee fail-safe operation.

Features：

- Very low ohmic charge switch (0.25 Ω) with soft switching and adjustable current limitation
- Very low ohmic reverse switch (0.25 Ω) with built-in current limitation
- 130 mA pre-charge current
- Battery over-voltage and under-voltage protection.
- Charger over-voltage (up to 20 V) and reverse polarity (down to -20 V) protection.
- On-chip thermal protection
- Charger detection
- Built-in current sensing
- Small 3 x 3 mm HVSON10 package with excellent thermal properties
- The UBA2008 is qualified according to the IEC 61000-4-2 standard for ESD performance.

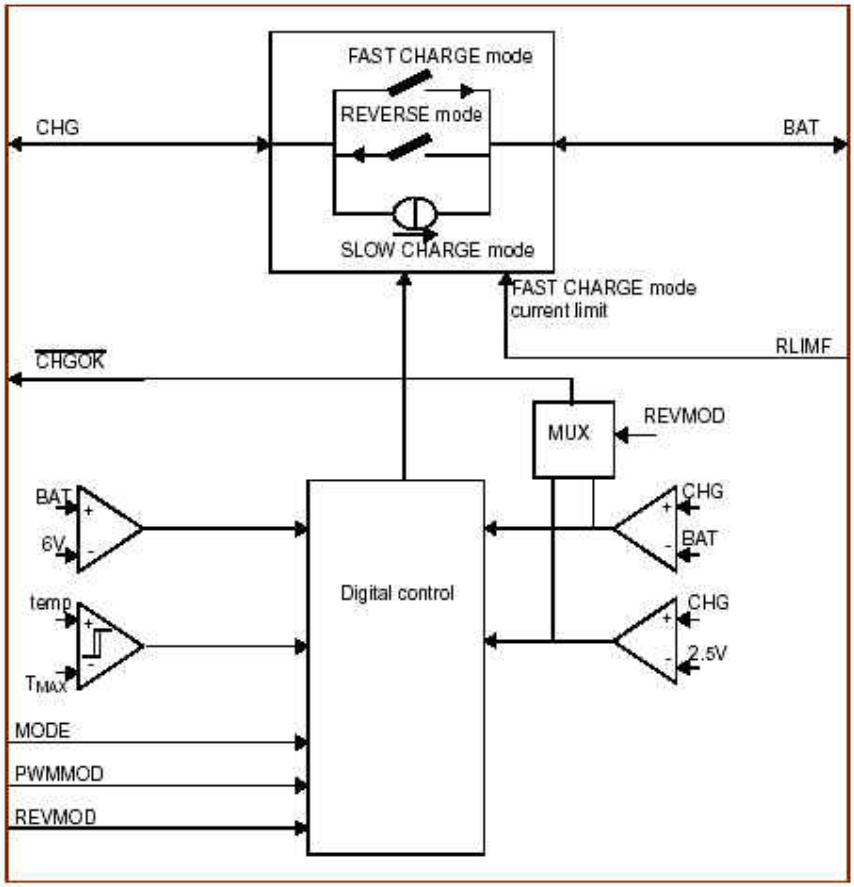


Fig 1. Functional Diagram UBA2008

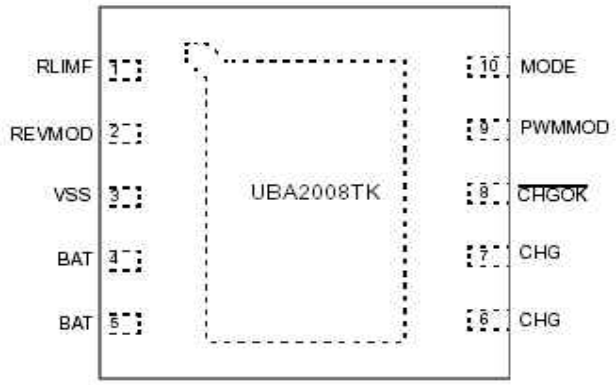


Table 2: UBA2008 pin list

Symbol	HVSON10 Pin no	Supply	Description/Remarks
BAT	4,5	n.a.	Battery pin. Power Input/Output.
CHG	6,7	n.a.	Charger input / REVERSE mode output. Power Input/Output.
VSS	3	n.a.	Ground
MODE	10	n.a.	Charge mode input. See Table 3 for operating modes. Digital input, 160 kΩ pull-down.
PWMMOD	9	n.a.	PWM mode input. See Table 3 for operating modes. Digital input, 160 kΩ pull-down.
REVMOD	2	n.a.	REVERSE mode control. See Table 3 for operating modes. Digital input.
RLIMF	1	n.a.	FAST CHARGE mode current limiting resistor. Output current source.
$\overline{\text{CHGOK}}$	8	n.a.	Charger detection output. Output is in high impedance when charger voltage < 2.5 V and REVMOD is low. If REVMOD is high the output is in high impedance if $V_{CHG} < V_{BAT}$. Open drain output.