CONTENT

1.0 Objective

This document is intended for FCC testing; it mainly includes Tuning Up Procedure and Operational Manual.
It describes the key principles of K570; its tuning up, its operation among the interfaces and its antenna features.

2.0 Abbreviation and glossary

3WBUS Three-Wired BUS (Signalname)
AUXADC AUXilary Analog Digital Converter (Signalname)
AUXDAC AUXilary Digital Analog Converter (Signalname)
BB Baseband
BAI Baseband Audio Interface
COMBO Multi chip package consisting FLASH and SRAM
CPU Central Processing Unit
CSx Chip Select (Signalname)
DAI Digital Audio Interface
DCS Digital Cellular System
EEPROM Electrically Erasable Programmable Read-Only Memory
EVITA Evaluation, Verification, Integration, Test and Application platform
FLASH special kind of programmable memory devices
GPIO General Purpose Input/Output (Signalname)
GPON General Power ON (Signalname)
GPRS General Packet Radio Service
GSM Global System for Mobil Communication
IrDA Infra-red Data Adapter
IIC Inter-IC (Signalname)
JTAG IEEE standardized test interface for ICs (Signalname),
abb. from Join Test Action Groupe
KBIO KeyBoard Input/Output (Signalname)
LCD Liquid Crystal Display
LED Light Emitting Diode
MMI Man Machine Interface
PA Power Amplifier
PCB Printed Circuit Board
PCS Personal Communications System
PROM Programmable Read Only Memory
PMU Power Management Unit

RFSIG Signal lines to control the function of the RF parts (Signalname)
SIM Subscriber Identity Module
SIOX Serial Input/Output interface for baseband (Signalname)
SIOY Serial Input/Output interface for audio (Signalname)
SRAM Static Random Access Memory
TC Transceiver
UART Universal Asynchronous Receiver / Transmitte

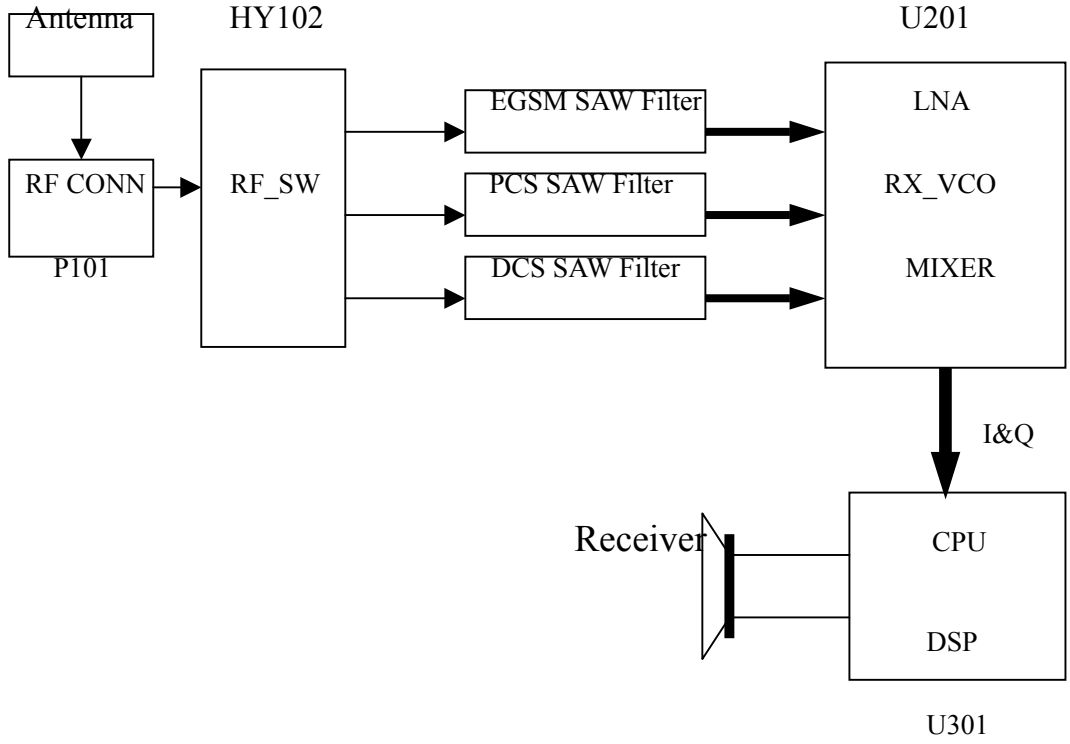
3.1 Principle of Rx Circuit

3.1.1 K570 supports three bands: EGSM 900/DCS 1800/PCS 1900.

PCS：

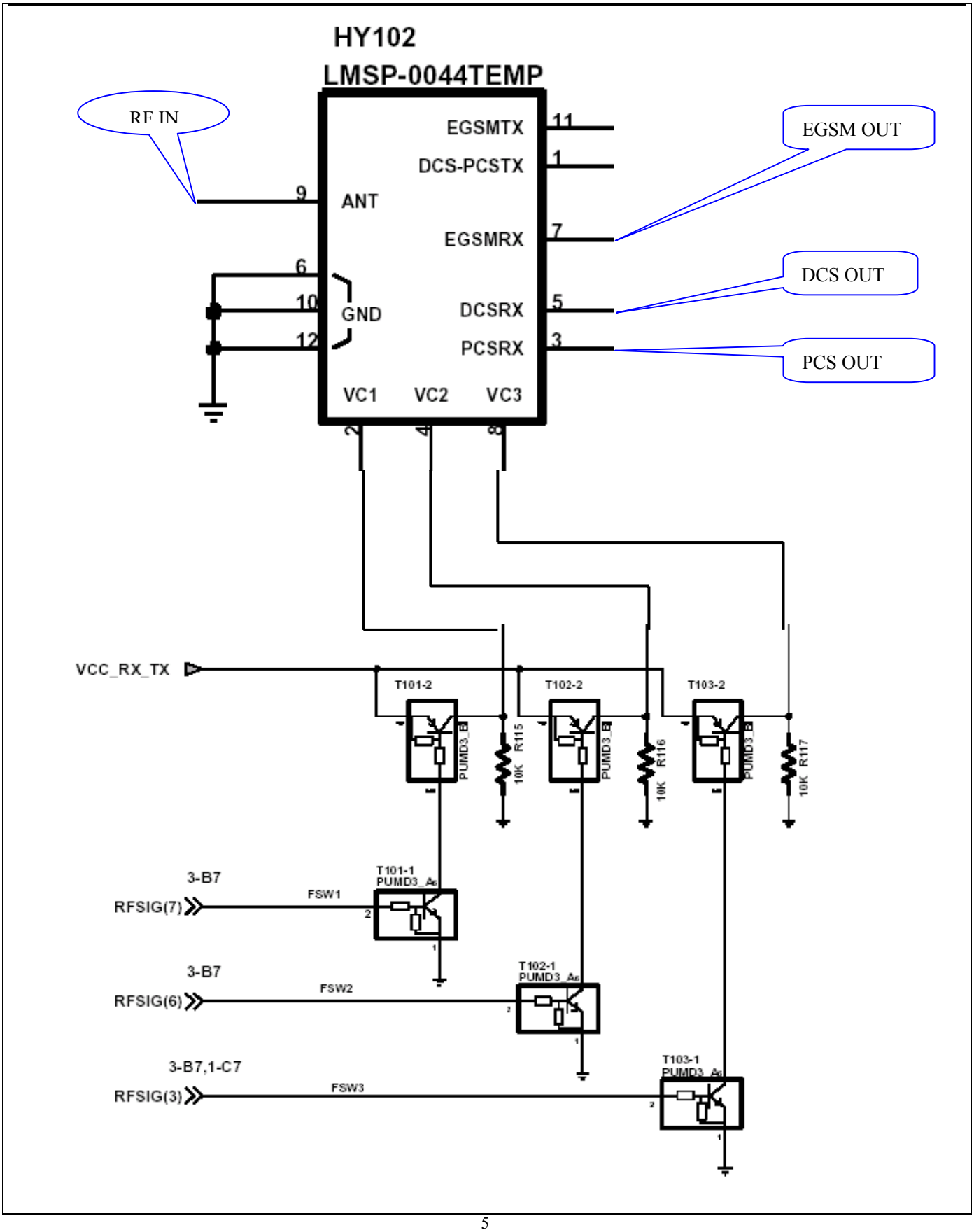
Channel Range ：512-810
Downlink：1930MHZ-1990MHZ
Uplink：1850MHZ-1910MHZ
Duplexer：80 MHZ
Bandwidth：200 KHZ
Power Level Range：0-15

3.1.2 K570 Block Diagram for Receive Path：

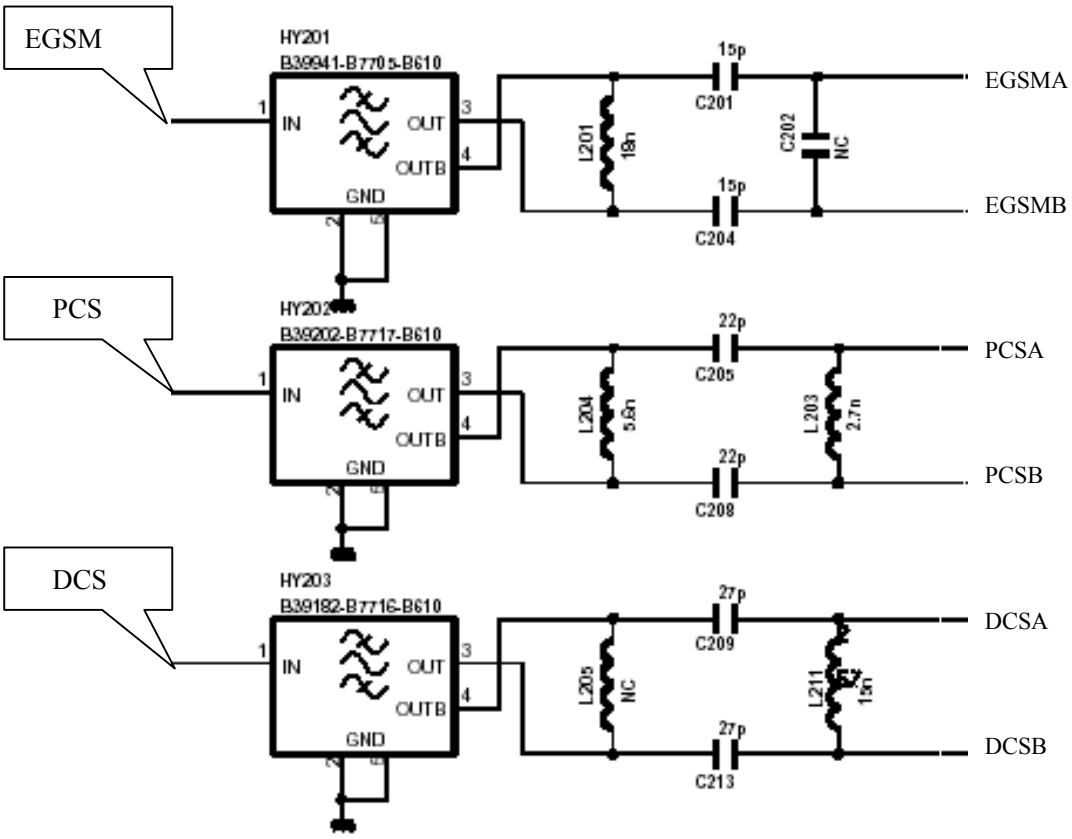


Block Diagram of Rx

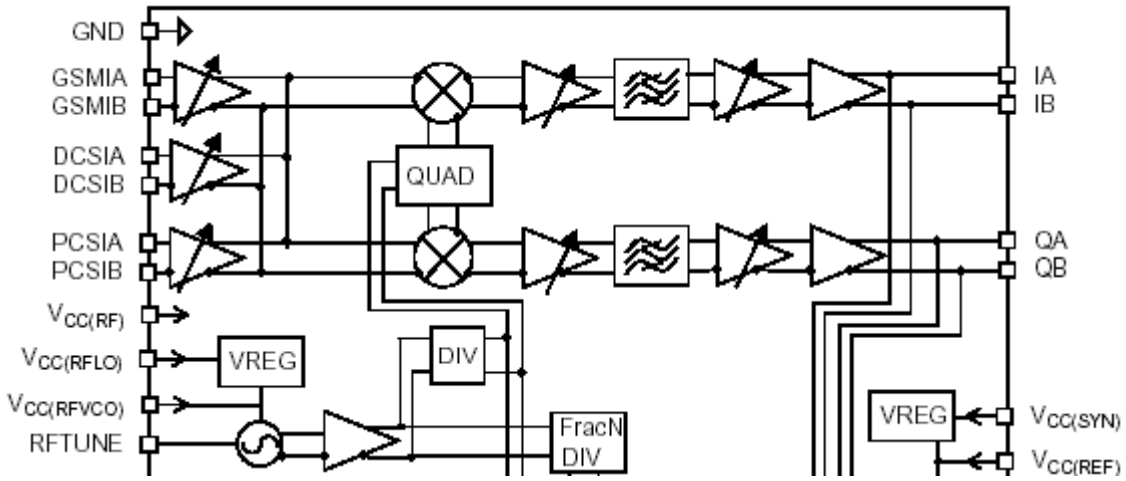
3.1.3 Signal is coming from the RF Connector. RF Connector is designed for testing; with the RF cable and equipment our test engineers can analyze the Rx/Tx signal through the RF Connector. The Signal goes into RF_Switch from the RF Connector to control the working status.



After the signal comes out from RF_Switch, it goes into the related Saw Filter, and the signal turns into two signals.



U201 is the transceiver, a very important chip set. For the receive part, it mainly completes: LNA（Low Noise Amplifier）、Mixer、baseband filter and so on. For example: signal from EGSM path comes out GSMA and GSMB. After LNA，they go into the mixer and are being demodulated perpendicularly with RX-VCO. The output baseband signals (IA、IB、QA、QB) after amplifier、filter come out of Pin6、Pin7、Pin8、Pin9 and input to the J13、J14、H13、H14 of CPU.



The baseband signals inside the CPU will be proceeded with analog to digital conversion、decoding、digital processor、digital to analog conversion, and the audio signal will be available to drive receiver.

3.1.4 Receive path circuit tuning up

Testing of the receive path includes RX LEVEL、 RX QUALITY、BER, and so on. There are mainly five possible reasons make the receive path works abnormallyt：small amplitude of the LNA 、MIXER without outputs、no RX-VCO signal、I&Q signal of U301 and CPU incorrect decoding.

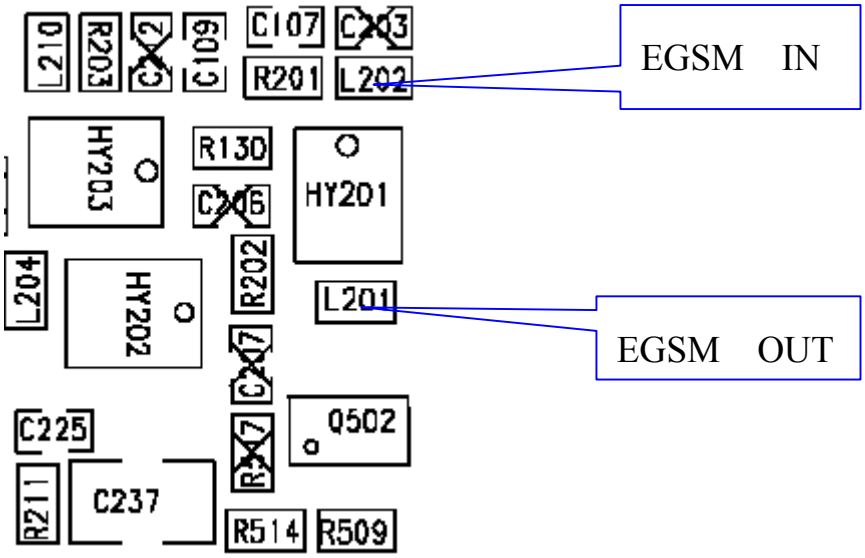
Here are the equipment we need to analyzer the problems（Such as. EGSM）：

a. Set Agilent8960 to the specific channel and set the basestation out put transmit signal to -30dbm。

b. Power on the mobile，the mobile is connected with Agilent8960 by the RF cable，and let the mobile be in the receive & testing mode.

c. Power meter and oscilloscope

Step 1：According to the signal block diagram test step by step，first get rid of HY201（Saw Filter）, in this way we can avoid the interference from the backwards and test the input signal to the HY201. If the signal is kind of small, we should check the input to HY102（RF-SW）. It might be the problem with P101，C106; otherwise it might be the problem with RF-SW CS、SS、CD or other control circuit.



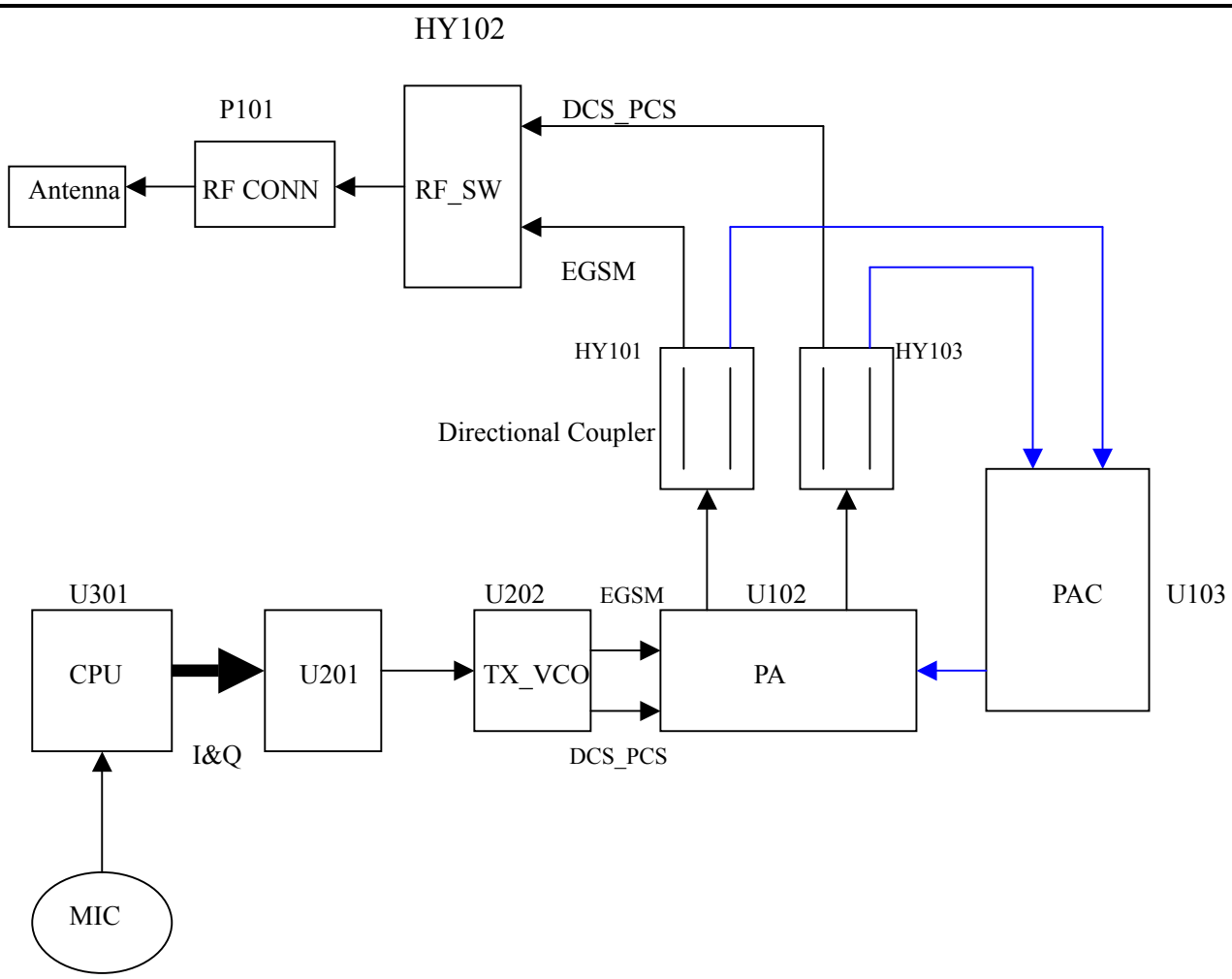
Step 2：Solder the HY201 on，test if its output signal attenuation is big，if it is big, it might have something to do with HY201-CD、SS、CS etc，or its load L201，C204，C201，U201.

Step 3：Test if RX-VCO,I&Q signals are normal or not，usually it might be the problem with C227，C230 or U201，U301—CS、CD、SS.

Step 4：If we cannot find the problem，we should changeU301，U201 or the problem with PCB.

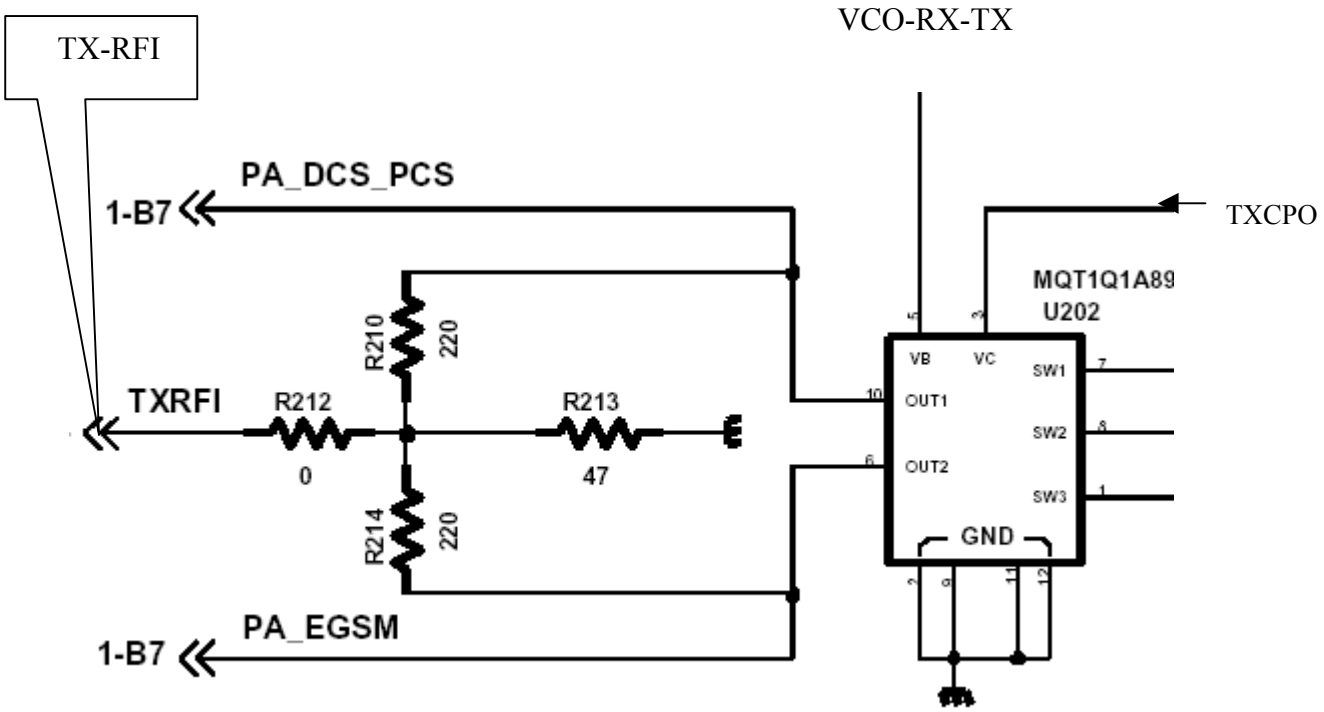
3.2 Principle of TX Circuit

3.2.1 Transmit path circuit block diagram



Transmit signal block diagram

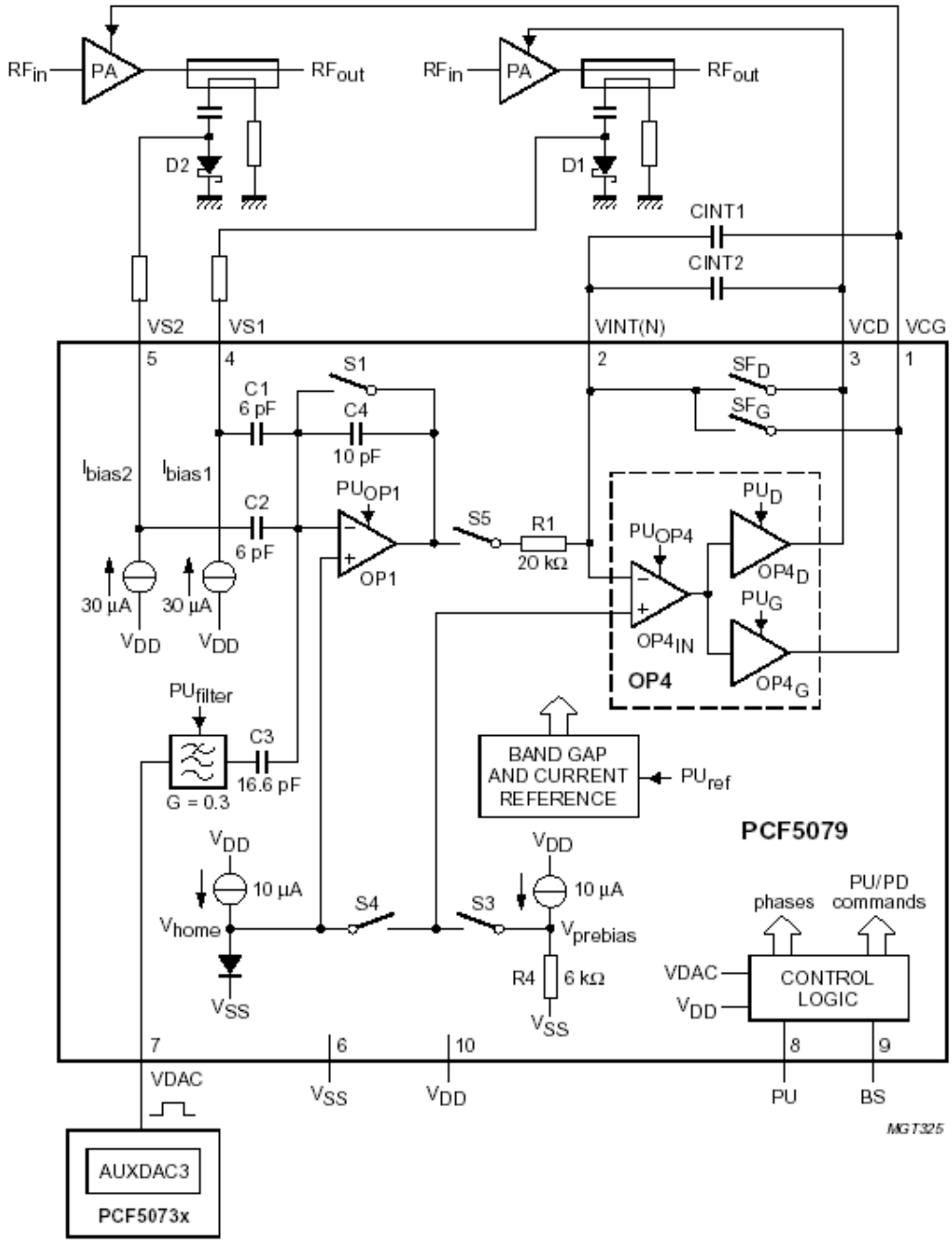
3.2.2 Audio signal turns into electrical signal by MIC，changes into baseband signals by A\D conversion、encoding、D\A conversion inside the CPU, output from J13、J14、H13、H14 and input into Pin6、Pin7、Pin8、Pin9 of U201. Baseband signals inside the U201 precede perpendicular demodulation, phase comparison etc. The output TXCPO signal，drive TX-VCO to work around the specific frequency. The TX-VCO signal from TX-RFI feeds back to U201。



TX-VCO has two outputs, one is PA-EGSM and the other is PA-DCS-PCS. They all go into PA（U102）。PA is a three-band amplifying module, the maximum gain for EGSM is 35dB; the maximum gain for DCS/PCS is 32dB. PAC controls its magnifying amplitude. PA output is connected with directional coupler，which transmits RF signal and feeds back PAC. PAC will control PA's gain by the RF signal. PAC's pin description and its Black diagram are shown as below：

SYMBOL	PIN	TYPE	DESCRIPTION
VCG	1	O and A	PA control voltage output (GSM)
VINT(N)	2	I and A	negative integrator input
VCD	3	O and A	PA control voltage (DCS)
VS1	4	I/O and A	sensor signal input 1
VS2	5	I/O and A	sensor signal input 2
VSS	6	G	reference ground

VDAC	**7**	**I and A**	**DAC input voltage**
PU	**8**	**I and D**	**power-up input**
BS	**9**	**I and D**	**band selection input**
VDD	**10**	**P**	**positive supply voltage**



RF signal comes out of RF-SW from directional coupler，and transmits from the antenna by the RF-Connector.

3.2.3 Transmit circuit tuning up

The testing of transmit path includes MAX POWER、TX-CURRENT、etc.

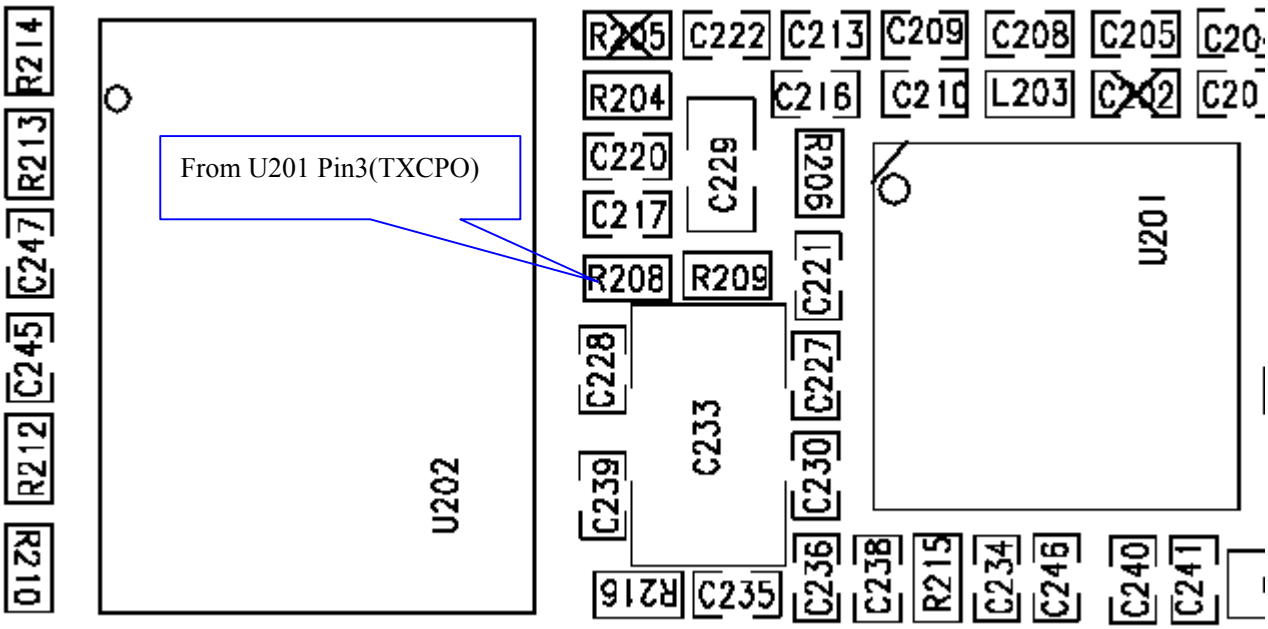
First prepare the equipment we need to analyze the mobiles with problems：（For example: EGSM）

a. Power on the mobile，enter the key and let the mobile be in the transmit/testing mode, like EGSM: Channel 1、Power Level 15；
b. Set the spectrum analyzer to the correct center frequency 890.2MHZ、bandwidth 10MHZ、and suitable scan time;
c. Power meter and oscilloscope.

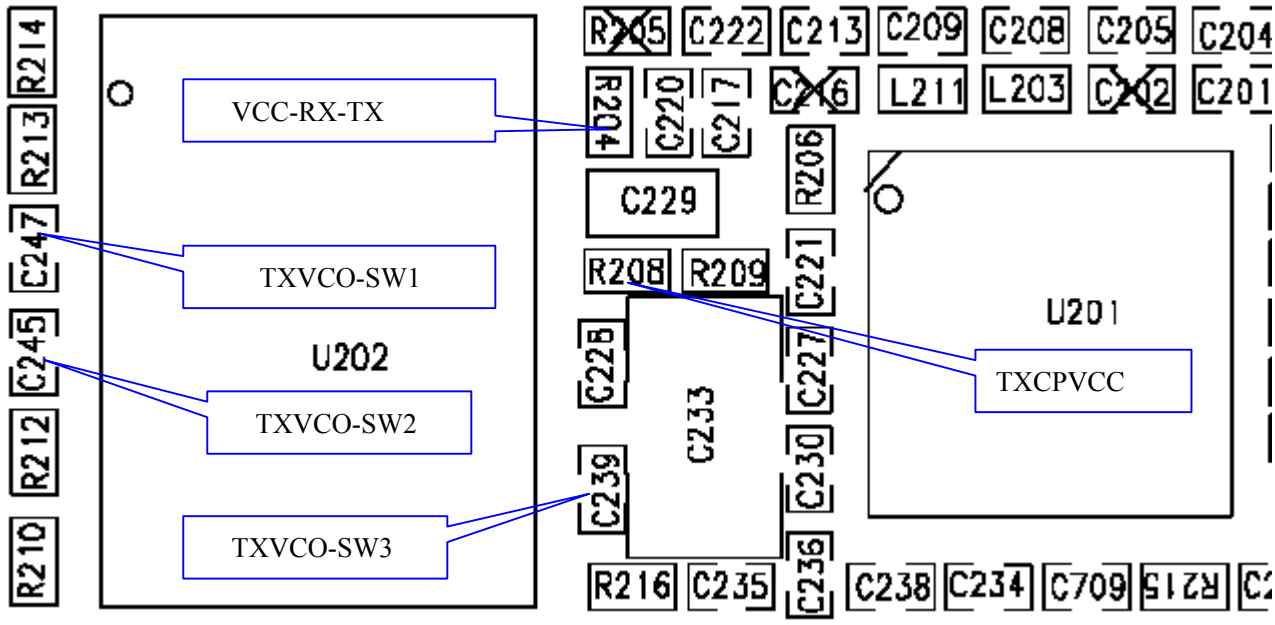
Here are the steps to check with the transmit circuit, if we are not sure about the spectrum, power or other parameter of the transmit signal, we can compare with a passed one:

Step 1: Test waveform of the IQ signal from CPU to U201 modulation/demodulation chip set. If the IQ signal is not good，we check with CPU and see if it is soldered well or not.

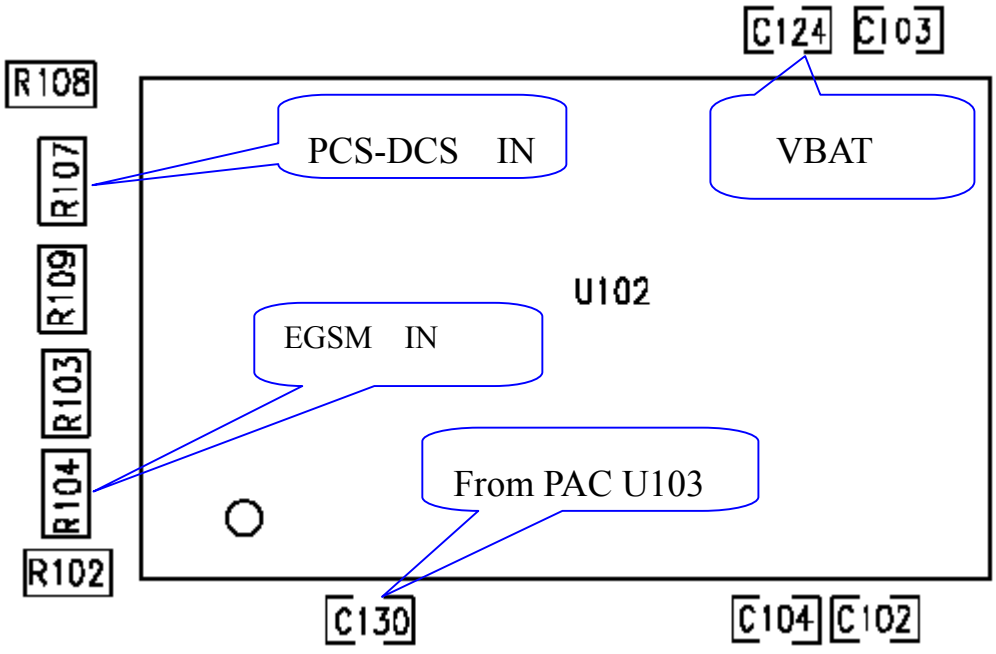
Step 2: If the IQ signal is not good，we test the TXCPO signal from U201 then. If the transmit signal is not good，check with U201; the circuit around it; and power supply voltage. If they all work well, we could think about change another U201.



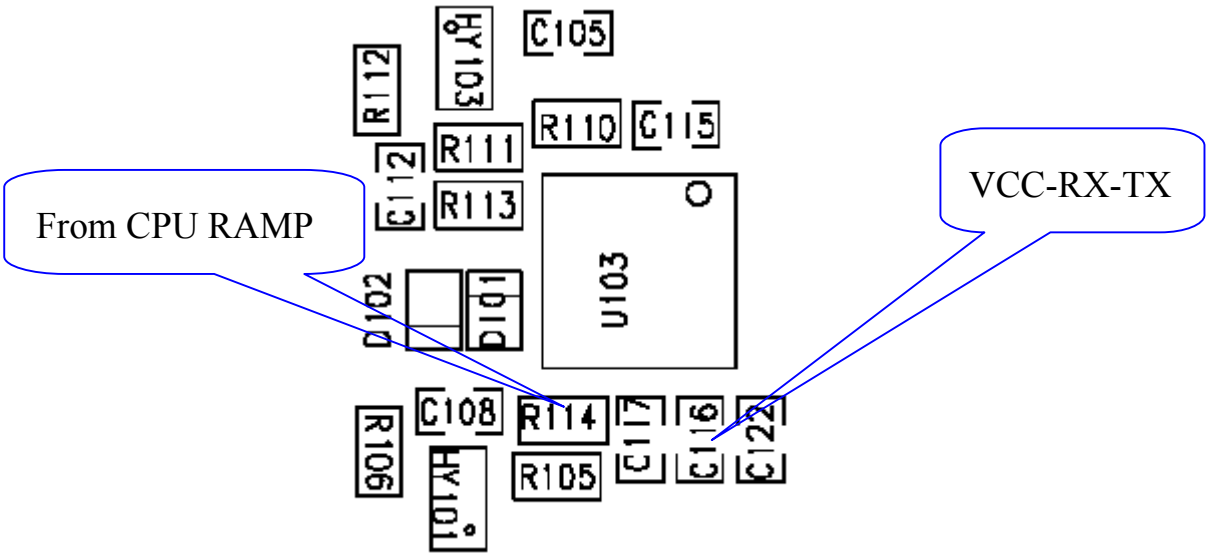
Step 3, If the output signal TXCPO from IC104 is fine, test the output of the U202：EGSM—pin 10，DCS-PCS pin6. And if the output signal is not good, test the supply voltage VCC-RX-TX of the U202 and EGSM、DCS 、PCS signal from CPU. If supply voltage signal is not good，check with U401 or change a good one; If EGSM 、DCS、PCS switching signals not nice, check with U301 or change another one. If those signals work fine，and resistance/ coil/ capacitor are all fine，then we change U202, and U201 in the end.



Step 4, If the output signal of U202 is fine，check the output signal from PA U102: for EGSM test U102 pin 5， for DCS-PCS test U102 pin 7. If the output signal from PA U102 is not good，then see if the PA is soldered well and the small stuff around it. Test VBAT of the PA and control signal RFSIG（3）。

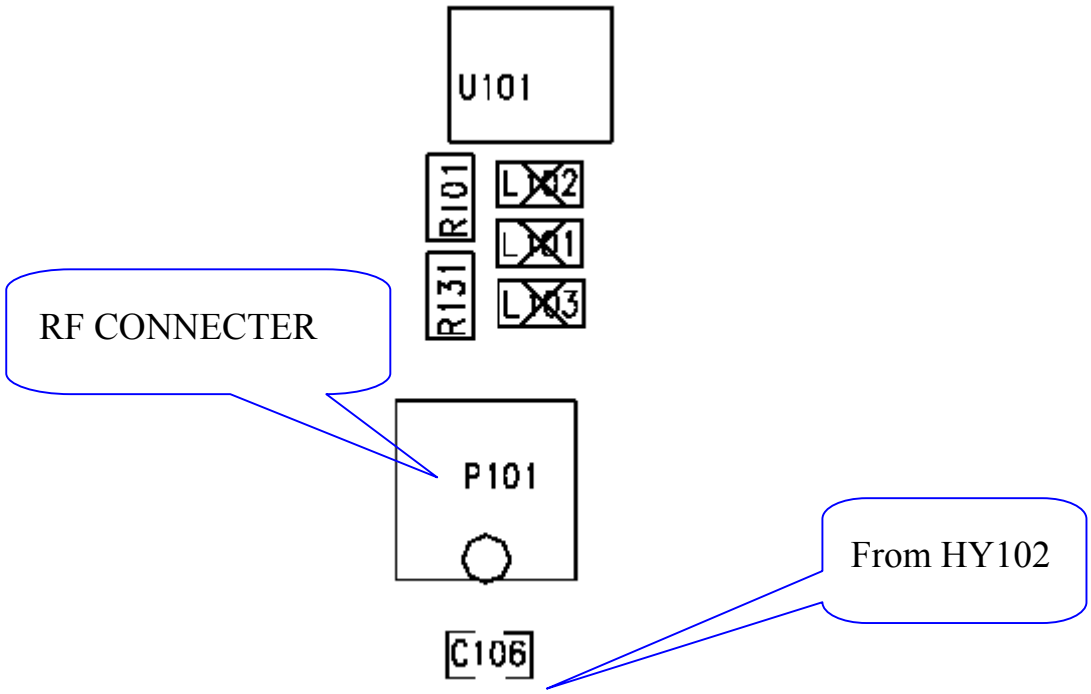


Step 5, Check PAC, U103， test VCC-RX-TX of U103 (we can test C116 instead), and see if U103 is soldered well. Check PAC and pieces around it. If they are all fine，we should change U102，U103，U201 in order.



Step 6, Test RF-SWITCH HY102 input/ output signals. Test C120 when the input signal is EGSM; test C105 when the input signal is DCS-PCS. For the output signal we could test C106. And test the supply voltage of the HY102 and its control signals.

At last, we could test the antenna，if the signal is not good from the antenna check P101，R131，R101



3.3 RF Circuit Reference

3.3.1 **UAA3536HN** Low power GSM/DCS/PCS multi-band transceiver

Features:

- Multiple band application for GSM, DCS and PCS cellular phone systems
- Compliant to GPRS class 12 operation
- Compliant to EDGE RX operation
- Low noise and wide dynamic range low IF receiver
- More than 35 dB on chip image rejection in receive
- More than 84 dB gain control range in receive
- Integrated channel filter
- Integrated TX filters
- High precision IQ modulator
- Multi-Band Tx modulation loop architecture including offset mixer and phase-frequency detector
- Fully integrated fractional N RF synthesizer with AFC control possibility
- Fully integrated RF VCO with integrated supply regulator
- Semi integrated reference oscillator with integrated coarse AFC possibility and with integrated supply regulator
- Two outputs to control RF front end switches (pin diodes)

- Fully differential design minimizing cross-talk and spurs
- Functional down to 2.4 V and up to 3.3 V
- 3-wire serial bus interface
- HVQFN40 package

Pins description：

SYMBOL	PIN	DESCRIPTION
TXRFI	1	Input from RF transmit VCOs
EXTRES	2	reference resistor for transmit modulation loop
TXCPO	3	transmit modulation loop charge-pump output
VCC(TXCP)	4	transmit modulation loop charge-pump supply
TXON	5	TX mode control pin
IA	6	baseband input-output; I path
IB	7	baseband input-output; I path
QA	8	baseband input-output; Q path
QB	9	baseband input-output; Q path
VCC(IF)	10	IF supply
CLKOUT	11	reference oscillator output
CAFCSUP	12	coarse AFC memory supply
CLKFDBX	13	reference oscillator feedback
REFGND	14	Ground for reference oscillator
REFIN	15	reference oscillator input
VCC(REF) r	16	eference oscillator supply
DATA	17	3-wire bus; DATA input
CLK	18	3-wire bus; CLOCK input
EN	19	3-wire bus; ENABLE control pin
VCC(RFCP)	20	RF charge-pump supply
RFCPO	21	RF charge-pump output
VCC(SYN)	22	synthesizer supply
RXON	23	RX mode control pin
SYNON	24	SYN mode control pin
VCC(RFVCO)	25	RF VCO supply
RFTUNE	26	tuning input of RF VCO
GNDTUNE	27	Ground for RF VCO tuning
VCC(RFLO)	28	RF LO supply
FESW1	29	frontend switch control output
FESW2	30	frontend switch control output
VCC(RF)	31	RF front-end and transmit modulation loop supply
GSMIA	32	receiver GSM RF input
GSMIB	33	receiver GSM RF input
RFGND1	34	Ground for RF frontend

PCSIA	35	receiver PCS RF input
PCSIB	36	receiver PCS RF input
RFGND2	37	Ground for RF frontend
DCSIA	38	receiver DCS RF input
DCSIB	39	receiver DCS RF input
FESWON	40	frontend switch control input

BLOCK DIAGRAM:

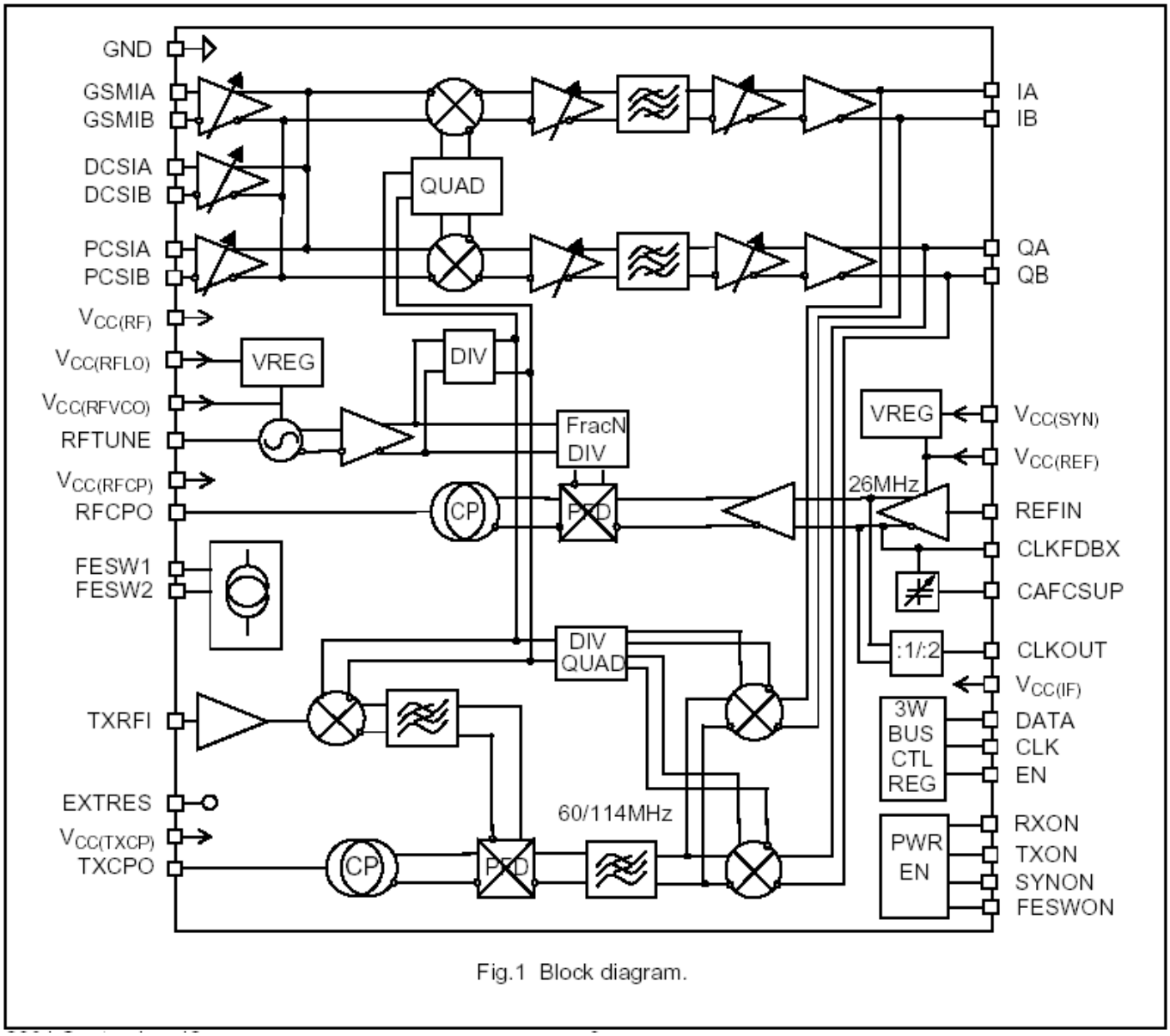


Fig.1 Block diagram.

3.4 Principle of Logic Circuit and tuning up

3.4.1 Principle of the logic circuit：

U301：OM6357EL/3C3/5 is adopted, there are two complete circuits inside the chipset，provide baseband processor、charge control、EMS memory management, etc. It includes：1、**PCF50874**：an individual System Controller with ARM, Digital Signal Processor & clock, keypad control, etc. 2、**PCF50732**：an analog baseband & audio interface，with audio processor，baseband & ancillary multi-media digital signal encoder，A/D、D/A conversers, etc. Diagram & pin description are as below：

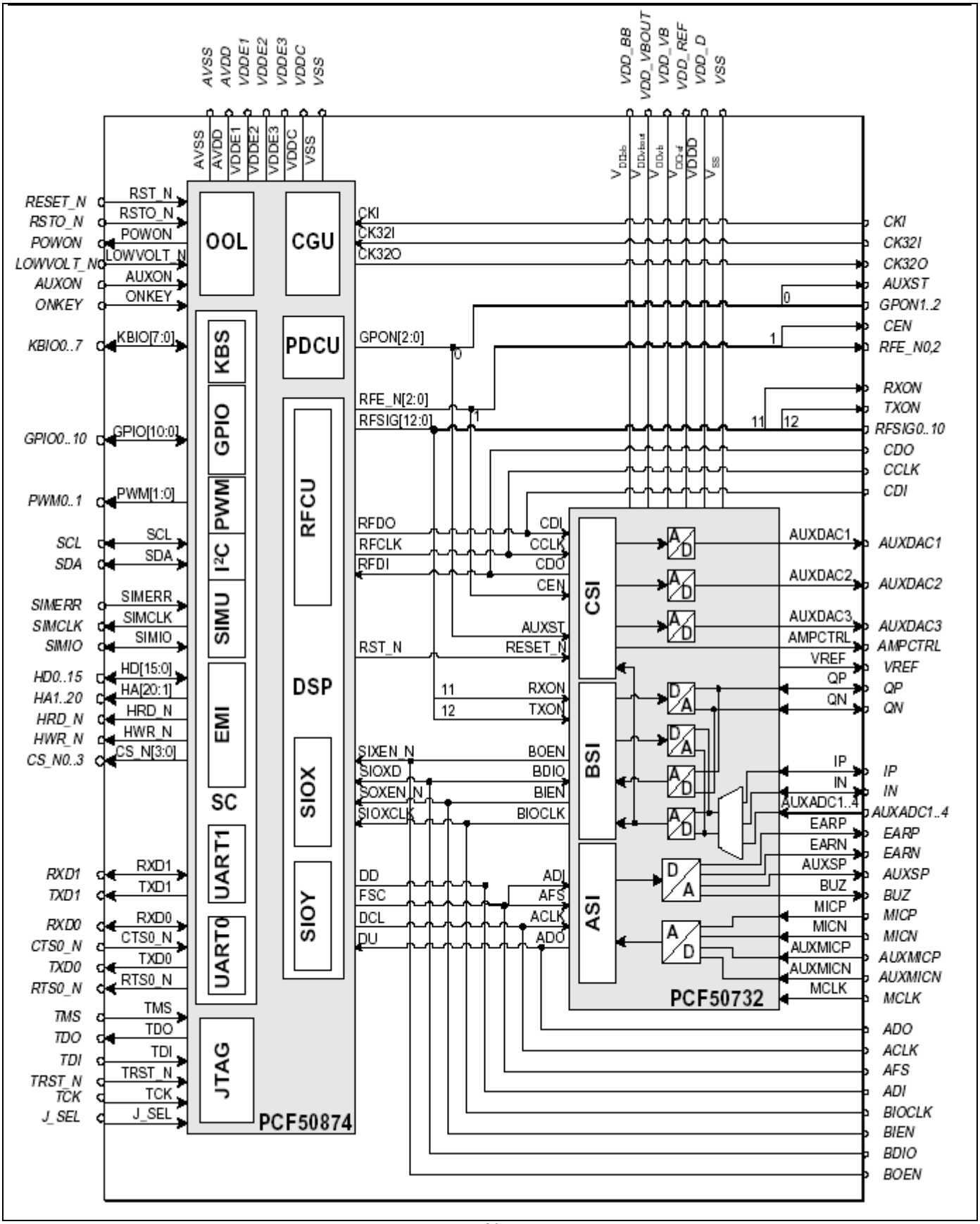


Table 6 Pin Description

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
Power and Ground								
VSS	Ground connections PCF50874	C3, E8, G1, G13, J1, K1, K7, M7, N5, N10, N11, N14, P1, P10	G		VSS			
AVSS	Analog ground PCF50874	P10	G		AVSS			
VSS_BB	Baseband analog ground	E13				G		V_{SS}
VSS_REF	Bandgap Reference ground	C13				G		V_{SS}
VSS_VB	Voiceband ground	A12				G		V_{SS}
VSS_VBOUT	Voiceband output drivers ground	C11				G		V_{SS}
VSSD	Digital ground	D11				G		V_{SS}
VDD_BB	Analog supplies PCF50732	F12				P		VDDbb
VDD_REF		D14				P		VDDref
VDD_VB		B12				P		VDDvb
VDD_VBOUT		C12				P		VDDvbout
VDD_D	Digital supply PCF50732	C9	P			P		VDDD
AVDD	Analog supply PCF50874	P12	P		AVDD			
VDDE1	Digital supplies for PCF50874	C8, H11, N12, P9	P		VDDE1			
VDDE2		P8, C1	P		VDDE2			
VDDE3		P4, M6, G2, L3	P		VDDE3			
VDDC	Digital supply for core of PCF50874	F5, N13, M8, K6	P		VDDC			
Reference Voltage								
VREF	bandgap reference for external noise decoupling	C14				I/O	VDDref	VREF
On/Off Logic								
RESET_N	chip set reset output	C10	I/O	VDDE1	RST_N	I	VDDD	RESET_N
RSTON	PCF50874 reset input	M10	I	VDDE1	RSTO_N			
LOWVOLT_N	low voltage alarm	M9	I	VDDE1	LOWVOLT_N			
POWON	power-on	K14	O	VDDE1	POWON			

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
AUXON	auxiliary power-on signal	K13	I	VDDE1	AUXON			
ONKEY	on/off key	M14	I	VDDE1	ONKEY			
Clocks								
CKI	13MHz clock input	P11	I	AVDD	CKI			
CKI32I	32kHz clock input	P13	I	VDDE1	CLK32I			
CK32O	32kHz clock output	P14	O	VDDE1	CLK32O			
MCLK	13MHz clock input	D10				I	VDDbb	MCLK
RF Control Interface								
CCLK	RF interface clock	E10	O	VDDE1	RFCLK	I	VDDD	CCLK
CDO	control serial data	E9	I	VDDE1	RFDI	O	VDDD	CDO
CDI	control serial data	D8	O	VDDE1	RFDO	I	VDDD	CDI
CEN	enable ctrl. serial	D9	O	VDDE1	RFE_N1	I	VDDD	CEN
RFE_N2	additional RF interface enables	K11	O	VDDE1	RFE_N2			
RFE_N0		J12	O	VDDE1	RFE_N0			
TXON	baseband transmit active	G12	O	VDDE1	RFSIG12	I	VDDD	TXON
RXON	baseband receive active	H12	O	VDDE1	RFSIG11	I	VDDD	RXON
RFSIG10	signal generator output	D7	O	VDDE1	RFSIG10			
RFSIG9		K9	O	VDDE1	RFSIG9			
RFSIG8		E7	O	VDDE1	RFSIG8			
RFSIG7		C6	O	VDDE2	RFSIG7			
RFSIG6		B7	O	VDDE2	RFSIG6			
RFSIG5		C7	O	VDDE2	RFSIG5			
RFSIG4		A7	O	VDDE2	RFSIG4			
RFSIG3		B6	O	VDDE2	RFSIG3			
RFSIG2		D6	O	VDDE2	RFSIG2			
RFSIG1		A6	O	VDDE2	RFSIG1			
RFSIG0		D5	O	VDDE2	RFSIG0			
Baseband Interface								
BIOCLK	interface clock	F11	I	VDDE1	SIOXCLK	O	VDDD	BIOCLK
BOEN	baseband serial data enable RX	G11	I	VDDE1	SIXEN_N	O	VDDD	BOEN
BDIO	baseband serial data	E11	I/O	VDDE1	SIOXD	I/O	VDDD	BDIO
BIEN	baseband serial data enable TX	F10	I	VDDE1	SOXEN_N	O	VDDD	BIEN

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
Audio Interface								
ACLK	audio serial interface clock	B8	I/O	VDDE1	DCL	I	VDDD	ACLK
AFS	audio serial frame	B9	I/O	VDDE1	FSC	I	VDDD	AFS
ADO	TX audio serial	A9	I	VDDE1	DU	O	VDDD	ADO
ADI	RX audio serial	A8	O	VDDE1	DD	I	VDDD	ADI
I²C Bus								
SCL	interface clock	C2	I/O	VDDE2	SCL			
SDA	data transfer	B3	I/O	VDDE2	SDA			
Memory Interface								
HA1	memory address bus	M4	O	VDDE3	HA1			
HA2		P3	O	VDDE3	HA2			
HA3		L4	O	VDDE3	HA3			
HA4		N3	O	VDDE3	HA4			
HA5		K5	O	VDDE3	HA5			
HA6		M3	O	VDDE3	HA6			
HA7		P2	O	VDDE3	HA7			
HA8		N2	O	VDDE3	HA8			
HA9		M1	O	VDDE3	HA9			
HA10		N1	O	VDDE3	HA10			
HA11		L2	O	VDDE3	HA11			
HA12		L1	O	VDDE3	HA12			
HA13		M2	O	VDDE3	HA13			
HA14		J2	O	VDDE3	HA14			
HA15		J5	O	VDDE3	HA15			
HA16		K3	O	VDDE3	HA16			
HA17		J4	O	VDDE3	HA17			
HA18		K4	O	VDDE3	HA18			
HA19		K2	O	VDDE3	HA19			
HA20		G4	O	VDDE3	HA20			

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
HD0	memory data bus	H4	I/O	VDDE3	HD0			
HD1		H3	I/O	VDDE3	HD1			
HD2		H2	I/O	VDDE3	HD2			
HD3		J3	I/O	VDDE3	HD3			
HD4		E5	I/O	VDDE3	HD4			
HD5		H1	I/O	VDDE3	HD5			
HD6		B1	I/O	VDDE3	HD6			
HD7		E4	I/O	VDDE3	HD7			
HD8		F3	I/O	VDDE3	HD8			
HD9		F2	I/O	VDDE3	HD9			
HD10		F1	I/O	VDDE3	HD10			
HD11		E1	I/O	VDDE3	HD11			
HD12		D1	I/O	VDDE3	HD12			
HD13		E3	I/O	VDDE3	HD13			
HD14		E2	I/O	VDDE3	HD14			
HD15		B2	I/O	VDDE3	HD15			
HWR_N	memory control signals	L5	O	VDDE3	HWR_N			
HRD_N		H5	O	VDDE3	HRD_N			
CS_N0		N4	O	VDDE3	CS0_N			
CS_N1		G5	O	VDDE3	CS1_N			
CS_N2		M5	O	VDDE3	CS2_N			
CS_N3		G3	O	VDDE3	CS3_N			
Keyboard scanner								
KBIO7	keyboard matrix	L14	I/O	VDDE1	KBIO7			
KBIO6		L12	I/O	VDDE1	KBIO6			
KBIO5		L13	I/O	VDDE1	KBIO5			
KBIO4		L11	I/O	VDDE1	KBIO4			
KBIO3		J11	I/O	VDDE1	KBIO3			
KBIO2		K12	I/O	VDDE1	KBIO2			
KBIO1		J10	I/O	VDDE1	KBIO1			
KBIO0		K10	O	VDDE1	KBIO0			
UART0								
CTS0_N	clear to send	B5	I	VDDE2	CTS0_N			
RTS0_N	request to send	A5	O	VDDE2	RTS0_N			
TXD0	transmit data	C5	O	VDDE2	TXD0			
RXD0	receive data	C4	I/O	VDDE2	RXD0			

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
UART1								
TXD1	transmit data	A4	O	VDDE2	TXD1			
RXD1	receive data	D4	I/O	VDDE2	RXD1			
SIM Interface								
SIMCLK	interface clock	M13	O	VDDE1	SIMCLK			
SIMIO	data transfer	M12	I/O	VDDE1	SIMIO			
SIMERR	error removal	M11	I	VDDE1	SIMERR			
General Purpose I/O Port								
GPIO10	general purpose signal	K8	I/O	VDDE2	GPIO10			
GPIO9		N8	I/O	VDDE2	GPIO9			
GPIO8		P6	I/O	VDDE2	GPIO8			
GPIO7		N7	I/O	VDDE2	GPIO7			
GPIO6		L9	I/O	VDDE2	GPIO6			
GPIO5		L7	I/O	VDDE2	GPIO5			
GPIO4		P7	I/O	VDDE2	GPIO4			
GPIO3		N6	I/O	VDDE2	GPIO3			
GPIO2		L8	I/O	VDDE2	GPIO2			
GPIO1		L6	I/O	VDDE2	GPIO1			
GPIO0		P5	I/O	VDDE2	GPIO0			
Pulse Width Modulator								
PWM1	pulse width modulator signal	E6	O	VDDE2	PWM1			
PWM0		F4	O	VDDE2	PWM0			
JTAG and Test Access Port								
TCK	interface clock	A3	I	VDDE2	TCK			
TMS	test mode select	A2	I	VDDE2	TMS			
TDI	test data input	D2	I	VDDE2	TDI			
TDO	test data output	D3	O	VDDE2	TDO			
TRST_N	reset	A1	I	VDDE2	TRST_N			
J_SEL	controller select BBP DSP or BBP SC	B4	I	VDDE2	J_SEL			
Power-Down Control								
GPON2	general purpose power down signal	N9	O	VDDE2	GPON2			
GPON1		L10	O	VDDE2	GPON1			
AUXST		G10	O	VDDE1	GPON0	I	VDDD	AUXST
PCF50732 General Purpose Output								
AMPCTRL		H10				O	VDDD	AMPCTRL

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
IF Signals								
IP	baseband differential I signal	J13				I/O	VDDA1	IP
IN		J14				I/O	VDDA1	IN
QP	baseband differential Q signal	H13				I/O	VDDA1	QP
QN		H14				I/O	VDDA1	QN
Auxiliary Functions								
AUXADC1	auxiliary ADC input	F14				I	VDDD	AUXADC1
AUXADC2		G14				I	VDDD	AUXADC2
AUXADC3		E14				I	VDDD	AUXADC3
AUXADC4		F13				I	VDDD	AUXADC4
AUXDAC1	auxiliary DAC outputs	E12				O	VDDA1	AUXDAC1
AUXDAC2		D13				O	VDDA1	AUXDAC2
AUXDAC3		D12				O	VDDA1	AUXDAC3
Voiceband Codec								
MICP	microphone differential input	A13				I	VDDA3	MICP
MICN		B13				I	VDDA3	MICN
AUXMICP	auxiliary microphone differential input	B14				I	VDDA3	AUXMICP
AUXMICN		A14				I	VDDA3	AUXMICN
EARN	earphone differential output	A11				O	VDDA4	EARN
EARP		B10				O	VDDA4	EARP
AUXSP	auxiliary earphone differential output	A10				O	VDDA4	AUXSP
BUZ		B11				O	VDDA4	BUZ

Notes：TYPE I：Input signal

O：Output signal

I/O：Duplexer signal

P：Power

G：Ground

Table 7 Power supply domains for LFBGA180 package

TYPE	NUMBER	DESCRIPTION	PIN
VDDC	4	core power supply pins	F5, N13, M8, K6
VDDE1	4	IO power supply pins	C8, H11, N12, P9
VDDE2	2	IO power supply pins with level shifter	P8, C1
VDDE3	4	IO power supply pins with level shifter	G2, L3, P4, M6
VSS, VSS_VB, VSS_VBOUT, VSS_REF, VSSD, VSS_BB, AVSS	19	ground pins	A12, C3, C11, C13, D11, E8, E13, G1, G13, J1, K1, K7, M7, N5, N10, N11, N14, P1, P10
VDD_D	1	Digital Supply of PCF50732	C9
VDD_VB, VDD_VBOUT, VDD_REF, VDD_BB	4	Analog supplies of PCF50732	F12, D14, B12, C12
AVDD	1	PLL supply pin	P12

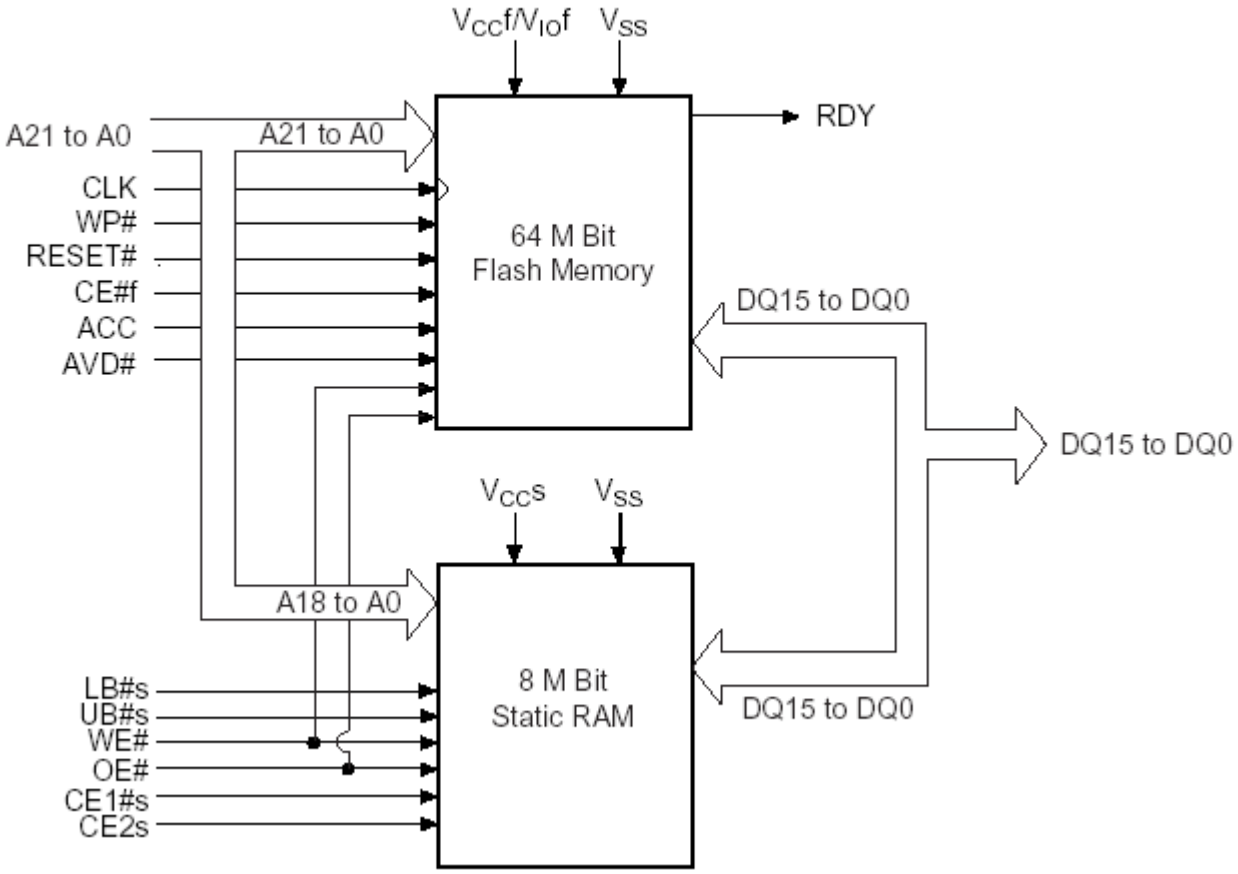
9 Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 134).

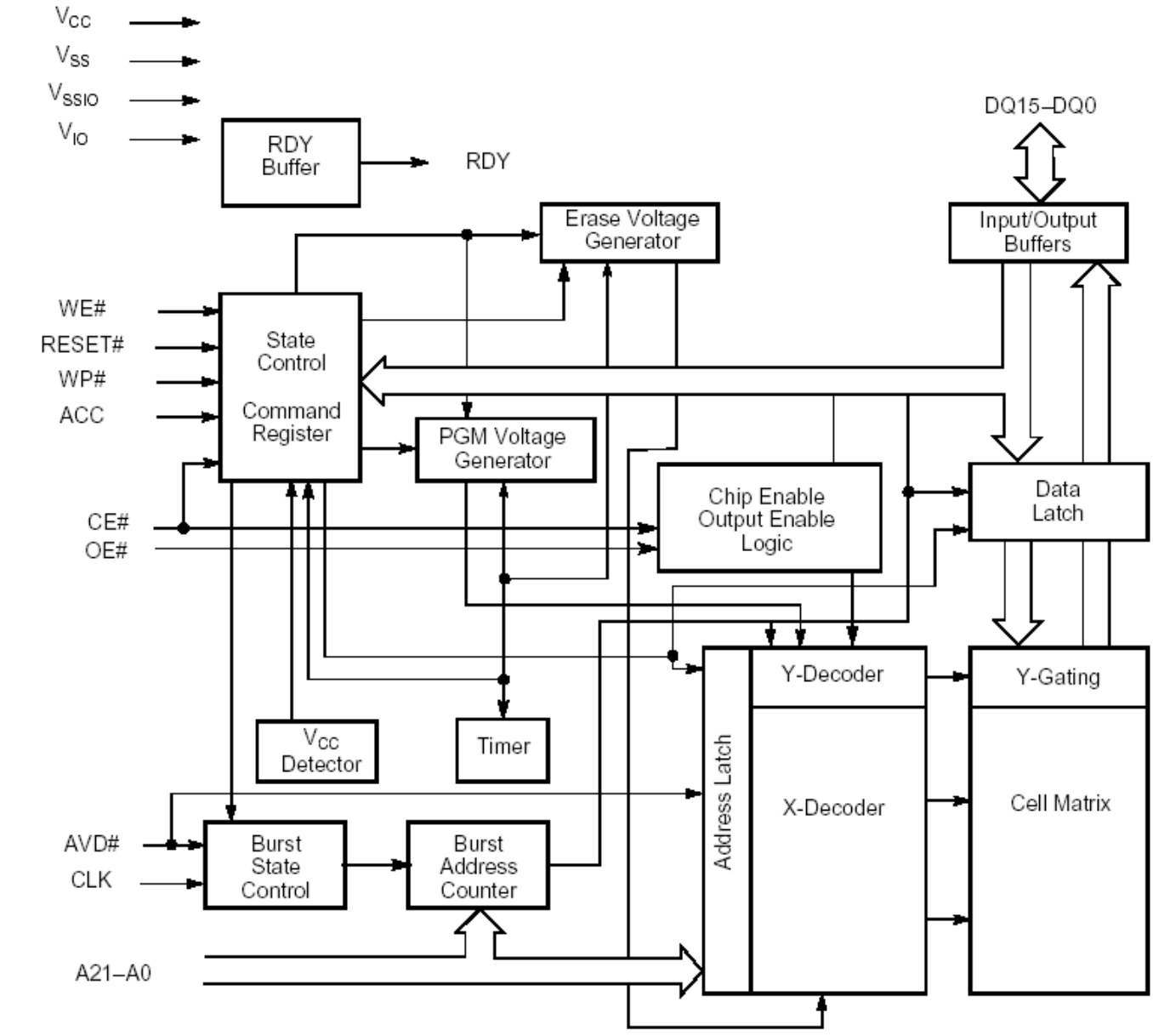
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}C$	PCF50874 Core supply voltage	–0.5	+3.3	V
VDDD VDD_BB VDD_VB VDD_VBOUT VDD_REF	PCF50732 Digital and Analog supplies	-0.5	+3.3	V
VDDE1	PCF50874 IOs supply voltage VDDE1	-0.5	+3.3	V
VDDE2	PCF50874 IOs supply voltage VDDE2	-0.5	+3.6	V
VDDE3	PCF50874 IOs supply voltage VDDE3	-0.5	+3.6	V
V_I	Input voltage on any pin with respect to ground (VSS)	–0.5	VDDx+0.5	V
IIBBI1	PCF50732 DC current into any pin (except EARP/EARN,AUX,BUZ)	-10	+10	mA
IIBBI2	PCF50732 DC current into EARP/EARN, AUX, BUZ	-100	+100	mA
I_I, I_O	DC current into any input or output	–10	+10	mA
P_{tot}	total power dissipation	–	1.36	W
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
T_j	operating junction temperature range	–	+125	°C

U500：Memory chip adopts AM42BDS6408GT89I. It integrates with 64M Bit Flash Memory and 8M Bit SRAM。

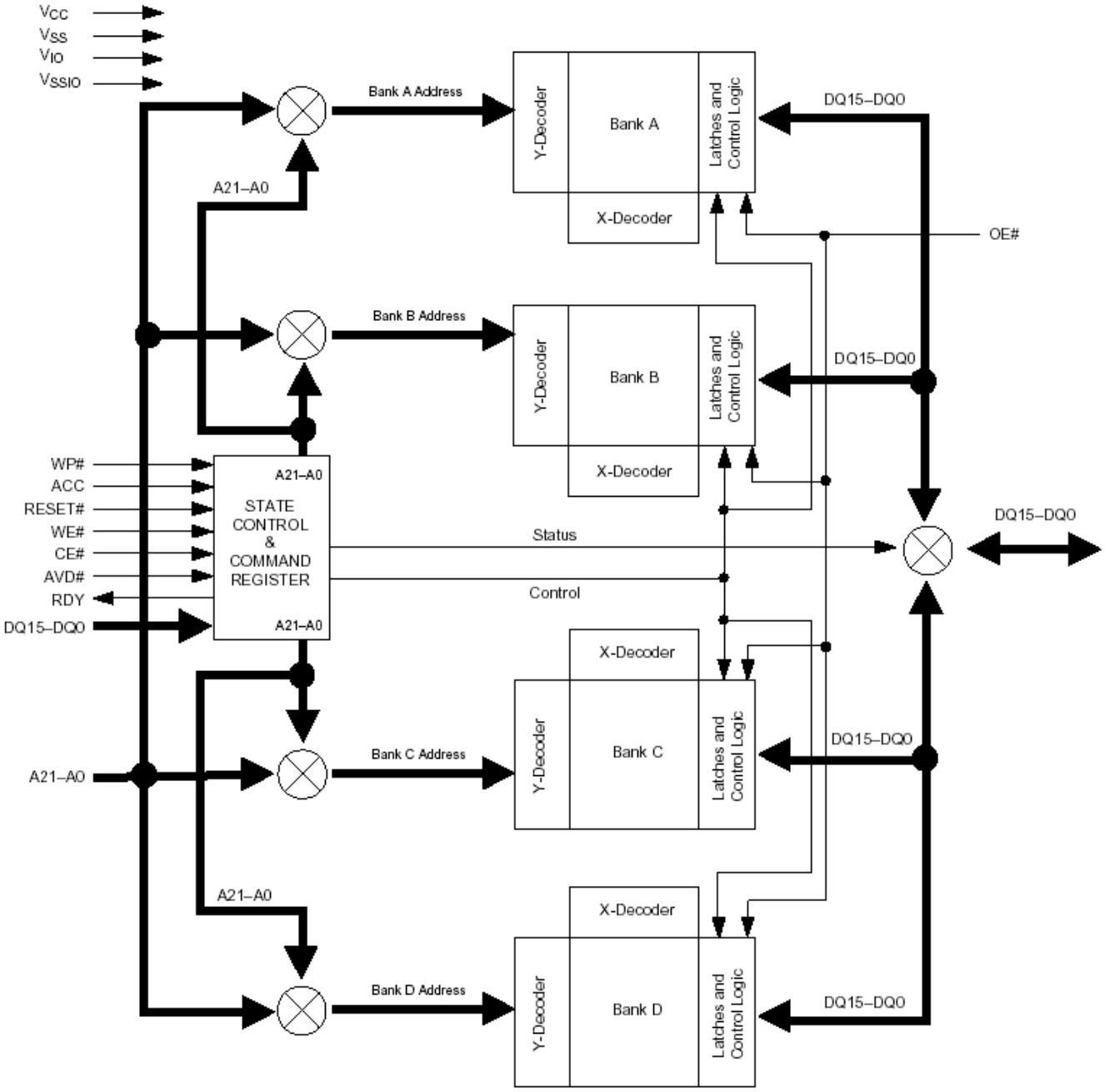
BLOCK DIAGRAM



FLASH MEMORY BLOCK DIAGRAM



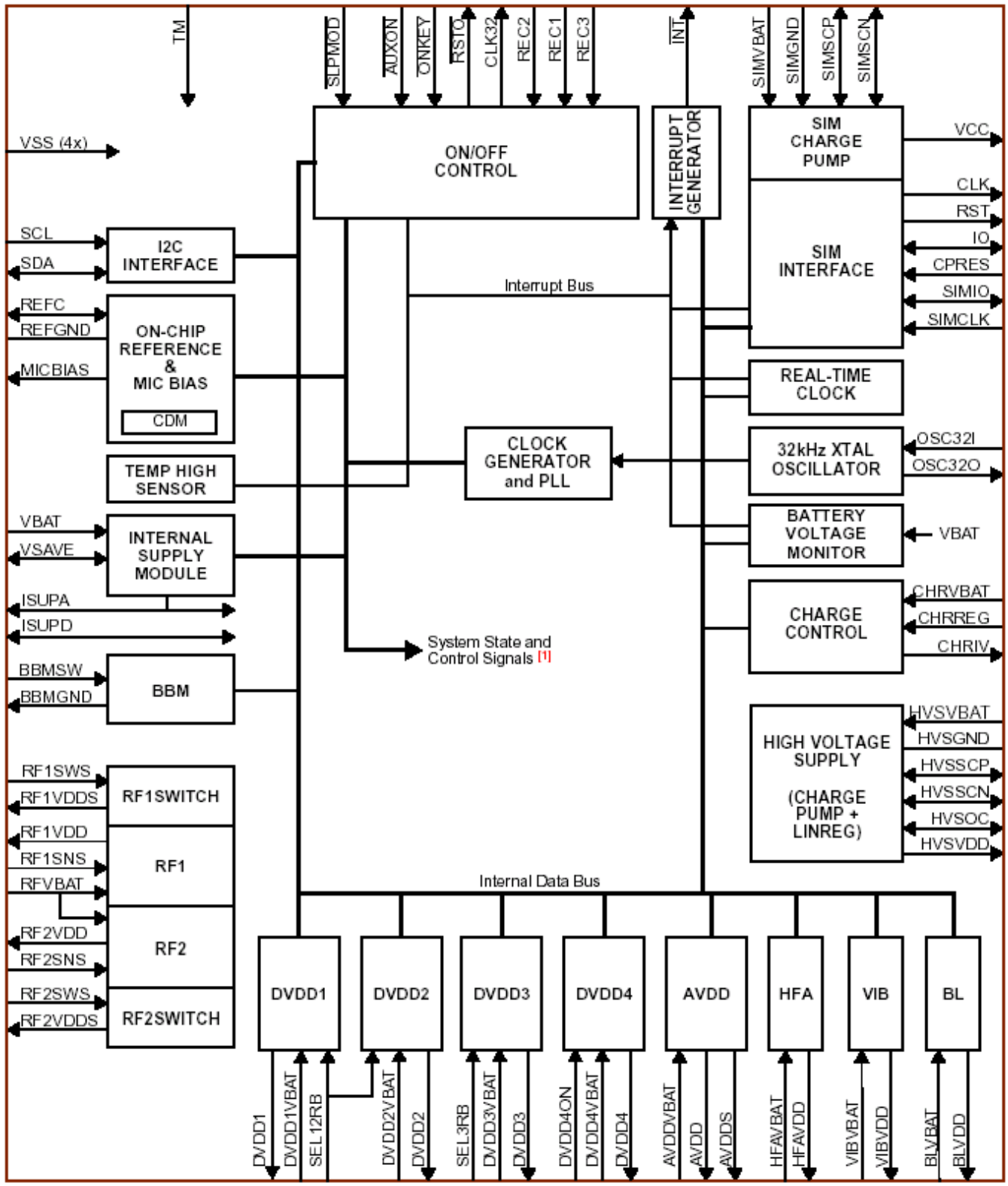
FLASH MEMORY SIMULTANEOUS OPERATION DIAGRAM



Pins description is as below：

A18–A0	19 Address Inputs (Common)
A21–A19	3 Address Inputs (Flash)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (SRAM)
CE2s	Chip Enable 2 (SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
UB#s	Upper Byte Control (SRAM)
LB#s	Lower Byte Control (SRAM)
RESET#	Hardware Reset Pin, Active Low
VCCf	Flash 1.8 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
VIOf	Input & Output Buffer Power Supply must be tied to VCC.
VCCs	SRAM Power Supply
VSSIOf	Output Buffer Ground
VSS	Device Ground (Common)
NC	Pin Not Connected Internally
RDY	Ready output; indicates the status of the Burst read.
	Low = data not valid at expected time.
	High = data valid.
CLK	CLK is not required in asynchronous mode. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (A21–A0).
	Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.
	High = device ignores address inputs
WP#	Hardware write protect input. At VIL, disables program and erase functions in the two outermost sectors. Should be at VIH for all other conditions.
ACC	At VID, accelerates programming; automatically places device in unlock bypass mode. At VIL, locks all sectors. Should be at VIH for all other conditions.

U401：POWE-SIM-MANAGEMENT adopts PCF50601ET-C2。It mainly provides Baseband power supply, RF power supply, SIM interface and so on. Diagram and pin description are shown below：



Symbol[1]	Ball	Supply	Description/Remarks
Linear regulators			
RFVBAT	G8	-	Input for RF1 and RF2 linear regulators
RF1SNS	F8	-	Voltage sense input for RF1; shall be connected to RF1VDD
RF2SNS	H8	-	Voltage sense input for RF2; shall be connected to RF2VDD
RF1SWS	E6	DVDD1	Output switch enable input for RF1; switches the RF1VDDS on.
RF2SWS	F6	DVDD2	Output switch enable input for RF2; switches the RF2VDDS on.
RF1VDD	F9	-	RF1 linear regulator 1 output voltage
RF1VDDS	E9	-	RF1 linear regulator switched output voltage
RF2VDD	G9	-	RF2 linear regulator 2 output voltage
RF2VDDS	H9	-	RF2 linear regulator switched output voltage
SEL12RB	E7	DVDD2	Select register B for DVDD1&2; note that this signal shall be stable at start-up.
DVDD1VBAT	F2	-	Input for DVDD1 linear regulator
DVDD1	F1	-	DVDD1 linear regulator output voltage
DVVD2VBAT	G2	-	Input for DVDD2 linear regulator
DVDD2	G1	-	DVDD2 linear regulator output voltage
SEL3RB	E5	ISUPD	Select Control Register B for DVDD3; note that this signal shall be stable at start-up.
DVDD3VBAT	H2	-	Input for DVDD3 linear regulator
DVDD3	H1	-	DVDD3 linear regulator output voltage
DVDD4VBAT	B4	-	Input for DVDD4 linear regulator
DVDD4	A4	-	DVDD4 linear regulator output voltage
DVDD4ON	F7	DVDD2	Switches DVDD4 linear regulator on; pin has pull-down resistor to VSS.
AVDDVBAT	H7	-	Input for AVDD linear regulator
AVDD	J7	-	AVDD linear regulator output voltage
AVDDS	G7	-	AVDD linear regulator switched output voltage
HFAVBAT	B5	-	Input for hands-free audio linear regulator
HFAVDD	A5	-	Hands-free audio linear regulator output voltage
VIBVBAT	B3	-	Input for vibrator linear regulator
VIBVDD	A3	-	Vibrator linear regulator output voltage

Backlight supply and control			
BLVBAT	B6	-	Input for backlight linear regulator
BLVDD	A6	-	Backlight linear regulator output voltage
BBMGND	B7	-	Backlight brightness modulator ground
BBMSW	A7	BLVDD	Backlight brightness modulator switch
Control interfaces			
$\overline{\text{SLPMOD}}$	D5	DVDD1	Signal switches the system to SLEEP state. At start up this signal is ignored until enabled by the system controller (see OOCC2 register).
TM	F5	ISUPD	Test mode selection; shall be connected to ground for normal operation.
$\overline{\text{RSTO}}$	D6	DVDD1	Active-low reset for logic supplied by DVDD1
$\overline{\text{ONKEY}}$	F4	ISUPD	Active Low On-key input with debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Edge sensitive input.
$\overline{\text{AUXON}}$	G4	ISUPD	Active Low Auxiliary On-Key input with 62 msec debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Level sensitive input.
CLK32	B8	DVDD1	32.768 kHz digital clock output; note that this output is only available when system is in ACTIVE or SLEEP state and DVDD1 is on.
$\overline{\text{INT}}$	D7	DVDD1	Interrupt to system controller; this active low signal is realized as an open drain output. Requires external pull-up resistor.
REC1	J2	DVDD2	Accessory recognition with interrupt; these inputs have selectable debounce filters (0, 14 or 62 ms) to prevent multiple interrupt generation
REC2	H3	DVDD2	
REC3	G3	DVDD2	
32.768 kHz oscillator			
OSC32I	J8	ISUPA	32.768 kHz oscillator input
OSC32O	J9	ISUPA	32.768 kHz oscillator output
Internal supply			
ISUPA	H5	-	Internal supply voltage output
ISUPD	G5	-	Internal supply voltage for digital logic. This pin shall be connected to ISUPA.
VSAVE	J4	-	Backup (auxiliary) battery
VBAT	J3	-	Main battery connection for general internal usage

VPROG	(G6)	-	Supply to program the internal OTP memory. Shall not be connected in the application. Will be removed for BGA production version.
Reference and Mic Bias Generator			
REFC	H6	-	Reference capacitor; a ceramic capacitor of 100 nF shall be connected to this pin.
MICBIAS	J5	-	Microphone Bias Generator output
REFGND	J6	-	Ground reference for analog circuits; shall be connected to system ground. This voltage is the reference for all voltages in this document unless stated otherwise.
High voltage supply			
HVSVBAT	C8	-	Input voltage for HVS charge pump
HVSGND	A9	-	Ground for HVS charge pump
HVSVDD	D9	-	HVS regulator output
HVSSCP	C9	-	HVS switching capacitor positive side
HVSSCN	B9	-	HVS switching capacitor negative side
HVSOC	D8	-	HVS output capacitor. Note that this pin is also the input voltage for the HVS regulator.
SIM interface and charge pump			
SIMIO	C7	DVDD1	Bi-directional data line to system controller; has an internal pull-up resistor to DVDD1.
SIMCLK	C6	DVDD1	SIM clock from system controller
IO	D1	V_{CC}	I/O line to/from SIM card. Internal pull-up resistor to V_{CC}.
CLK	D2	V_{CC}	Clock to SIM card
CPRES	D3	ISUPD	Switch contact in SIM socket; high level enables SIM, low level stops SIM (emergency deactivation). Input has internal pull-up resistor to ISUPD.
RST	C1	V_{CC}	Reset for SIM card
VCC	C2	-	Supply voltage for SIM card
SIMSCP	B1	-	SIM charge pump switching capacitor positive side
SIMSCN	A1	-	SIM charge pump switching capacitor negative side
SIMVBAT	B2	-	Input for SIM charge pump
SIMGND	A2	-	Ground for SIM charge pump (it is not recommended to use this ground for the card)
I^2C-bus interface			
SDA	F3	DVDD2	Data line
SCL	E4	DVDD2	Clock line

Battery charging control			
CHRIV	E3	-	Charger I/V control
CHRREG	E2	-	Battery pack regulation loop control
CHRVBAT	E1	-	Charger input voltage
General grounds			
VSS	C3, H4, E8, C5, A8, J1		Ground

3.4.2 Logic circuit tuning up：

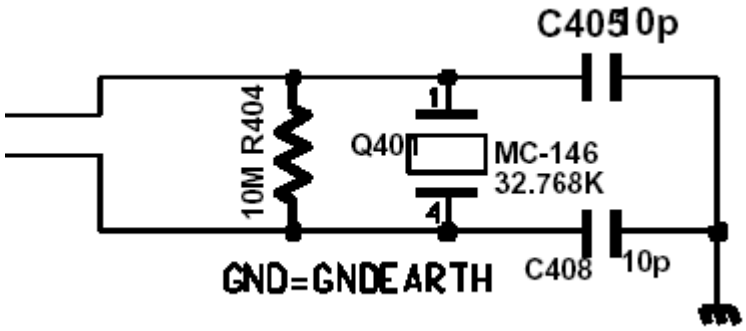
Cannot power on

a. Turn on power supply，test the pin-VBAT of U401，if the voltage is not correct; check the battery or the power supply voltage.

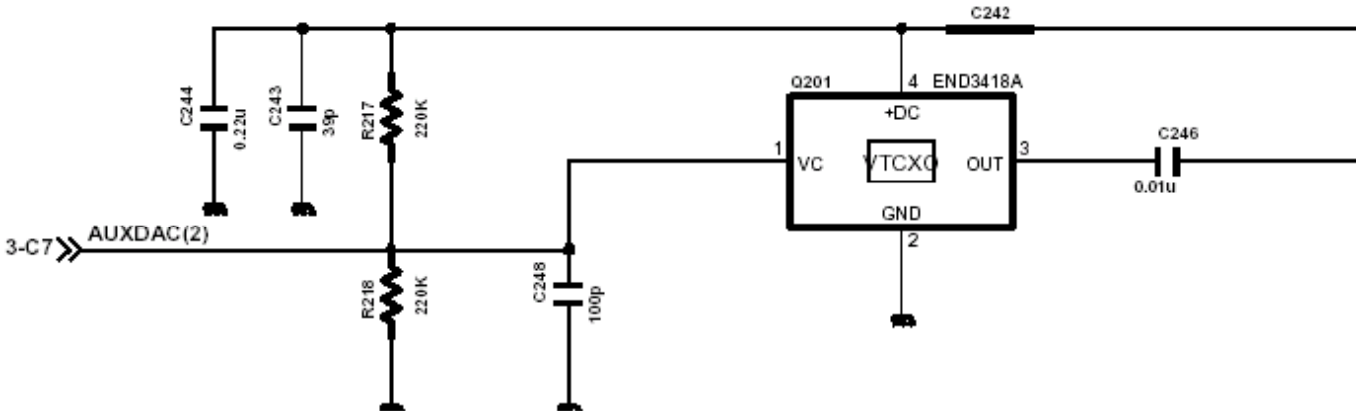
b. Check the battery contacts and see if it was cold soldered or unsoldered.

c. Check the Baseband supply and RF power supply of U401，change another U401 if necessary.

d. Test if 32KHz crystal oscillator clock works, otherwise change Q401, and check C408，C405，R404，U401



e. Check if 26M crystal oscillator works, otherwise change Q201 and check with C244，C243，R217，R218，C248，C246; Check AUXDAC（2）signal；change another U201 if necessary.



13M-crystal oscillator

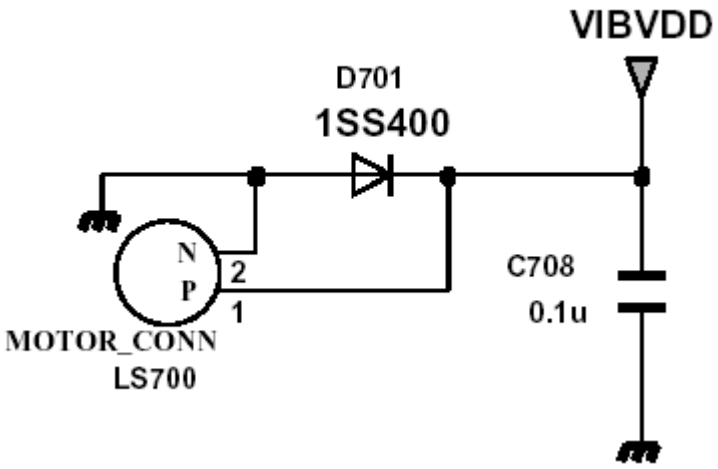
f. Check the signal from Memory or change another U500, U301 step by step

Do not vibrate

1. Check with the vibrator. And change it, if necessary.

2. Check if C708, R705, D701 are cold soldered or unsoldered.

3. Check with the supply voltage –VIBVDD. If the voltage is abnormal, change another U401. Or check the VIB of U701.

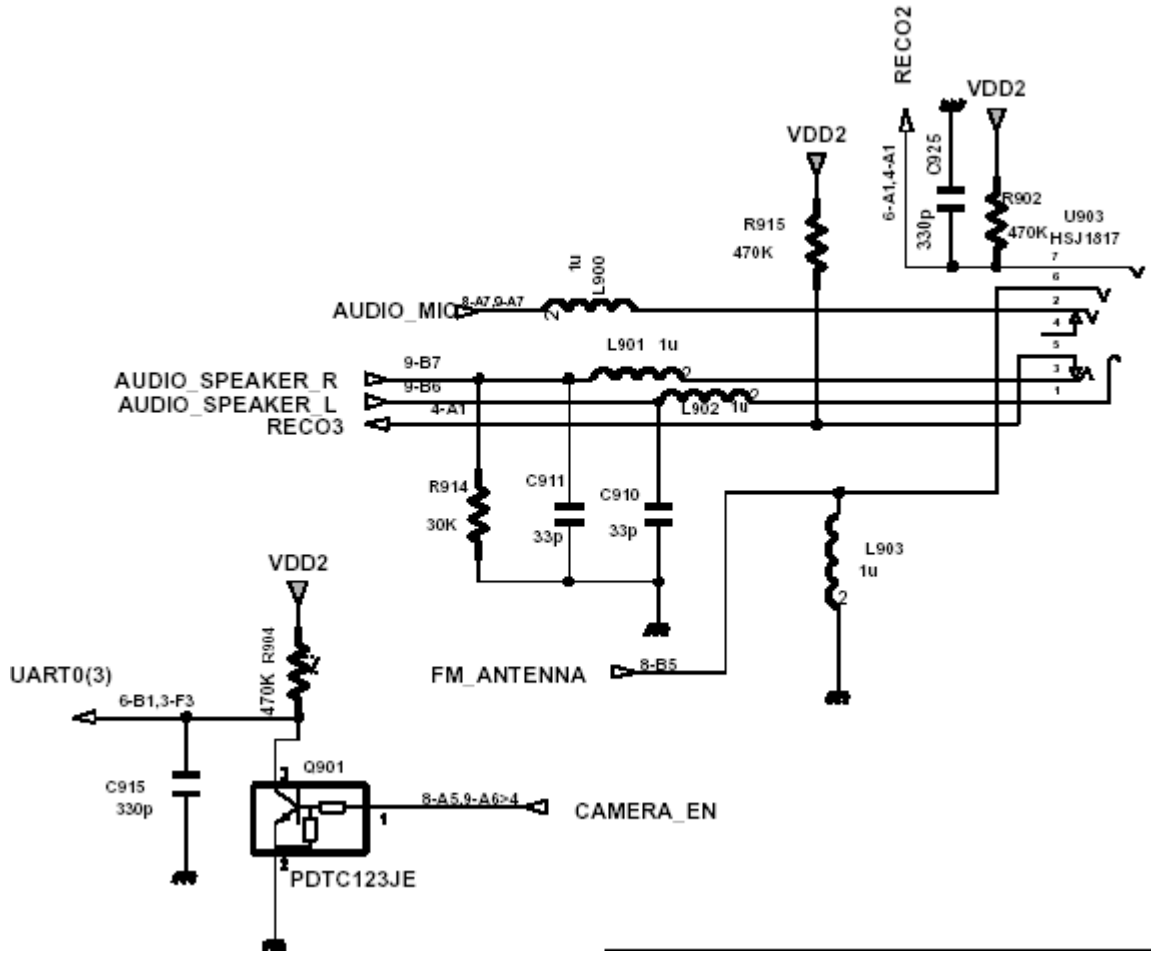


No keypad function

1. Check the connection between keypad and PCB
2. Check if the key board is placed above the shielding case nicely
3. Check if the connectors of the key board are cold soldered or damaged
4. Check if the connectors in the main PCB are cold soldered or damaged
5. Check if the contacts of the keypad are being oxygenated or not smooth
6. Check the signals on the main PCB
7. If the signal is incorrect, it might be the problem with cold soldered or unsoldered

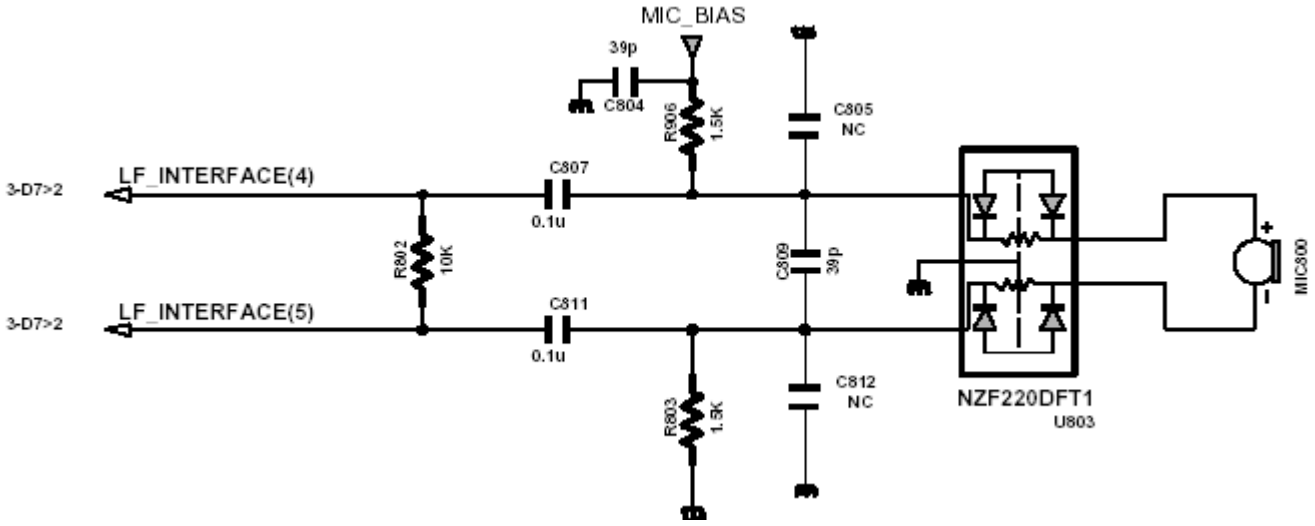
No hands free function

1. Check if the pieces are cold soldered、unsoldered or damaged
2. Check with the control signals
3. Check with the relevant chipset
4. Check if the problem with earpiece's contact or other component



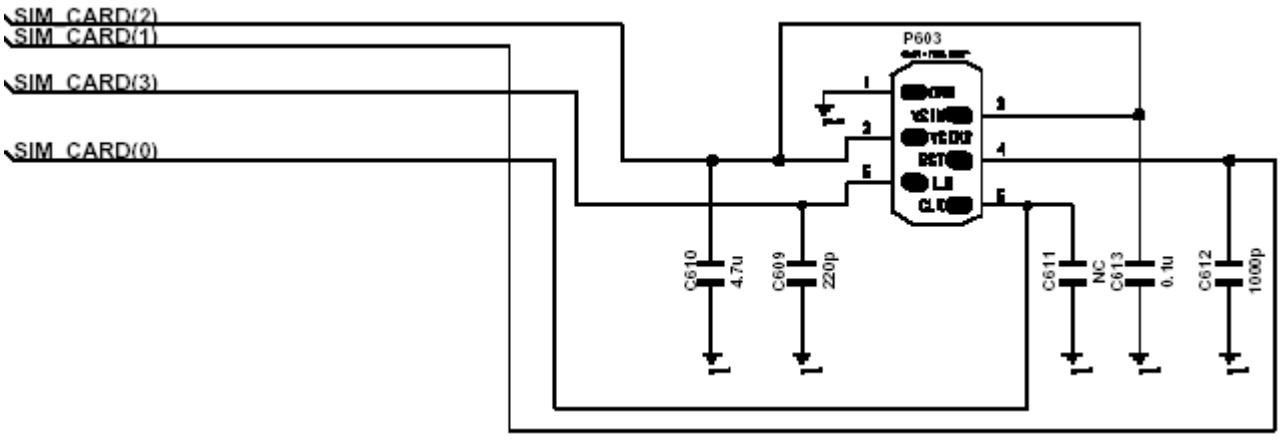
MIC does not work

1. Check if the MIC is placed nicely
2. Test if the signal of MIC contact is right or not
3. If the signal is incorrect，check the components of the path are soldered well or not
4. Check if voltage of MIC-BIAS is correct or not，or change U803
5. In the end check with the relevant chipset



SIM card invalid

1. Check if the SIM can work
2. Check if the SIM holder is soldered well
3. Check if the contacts of the SIM can be touched
4. Check if the contacts of the SIM with the same level
5. Check the signal of the power supply
6. Check the clock of the SIM
7. Check if the data information is correct



No backlight：

1. Check if the backlight is a good one

2. Check with the power supply voltage，if the voltage is not correct, change the power supply chipset U401.

3. Check with the relevant small components

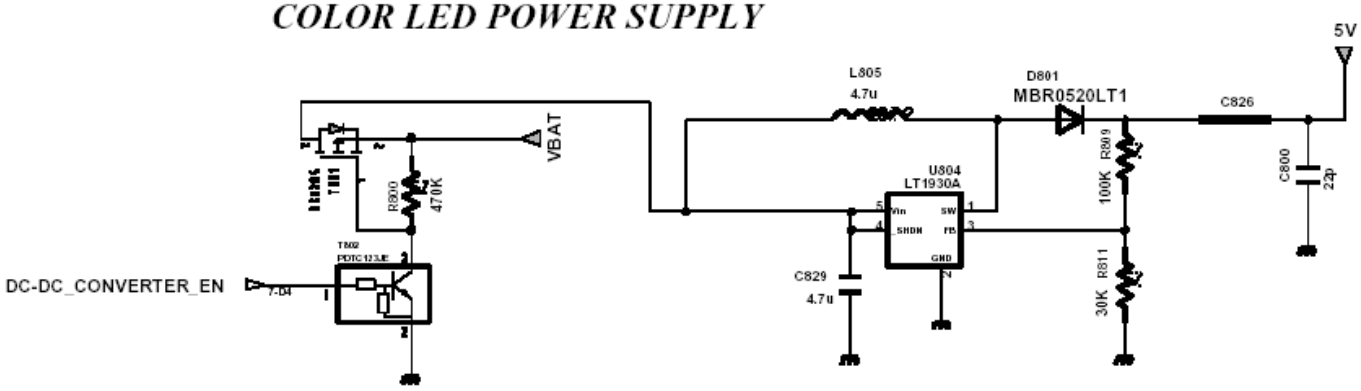
No color LED：

1. Check with the power supply circuit of the color LED

2. Check with control circuit of the color LED U701

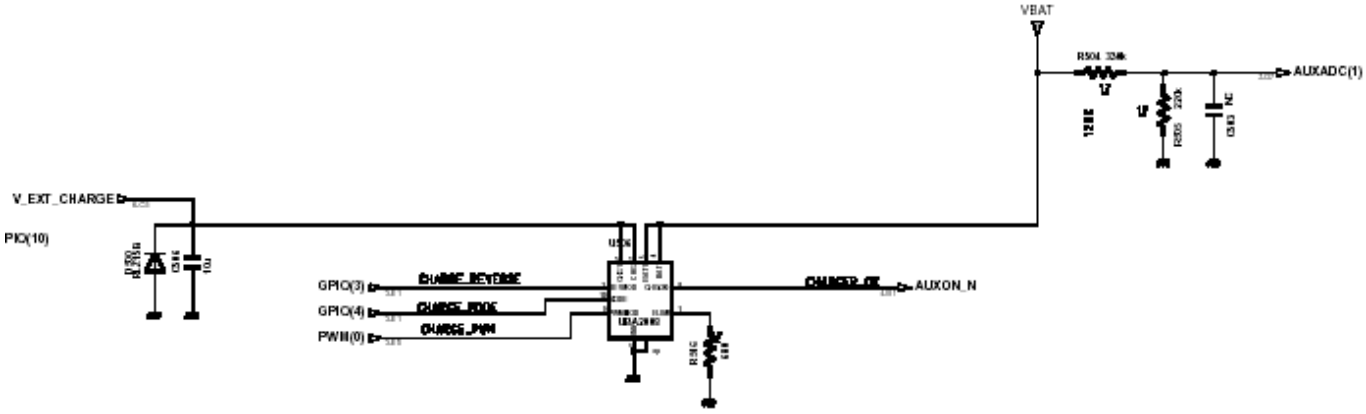
3. Check with the relevant components

COLOR LED POWER SUPPLY

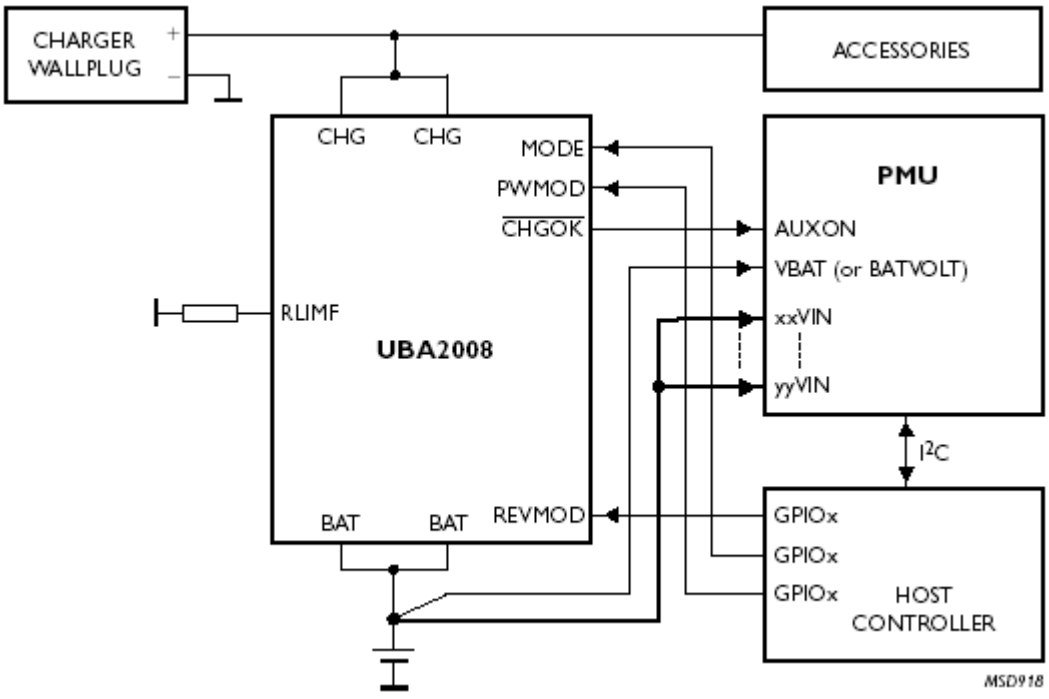


Can not charge：

1. Check with the battery contacts
2. Check with the charge control chipset U506
3. Check with the relevant components
4. In the end, change U401，U301 step by step

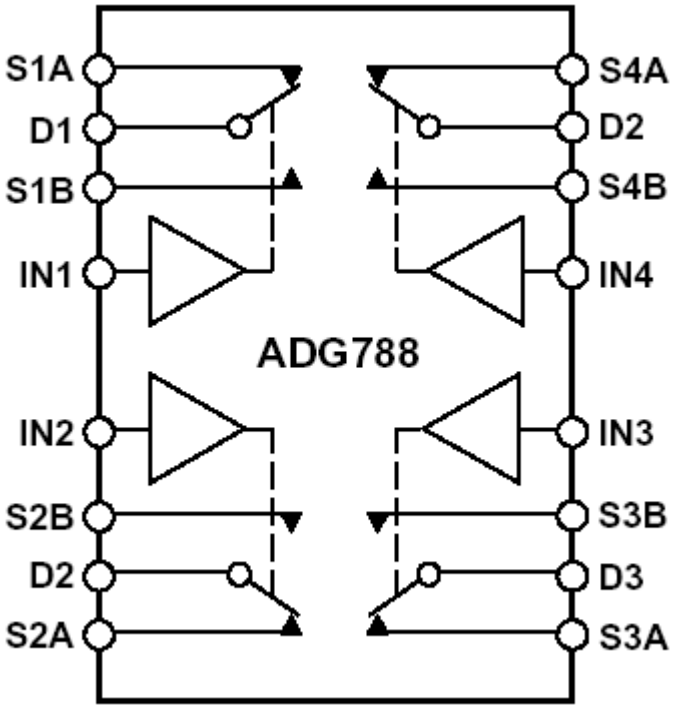


Block diagram of the charging circuit：

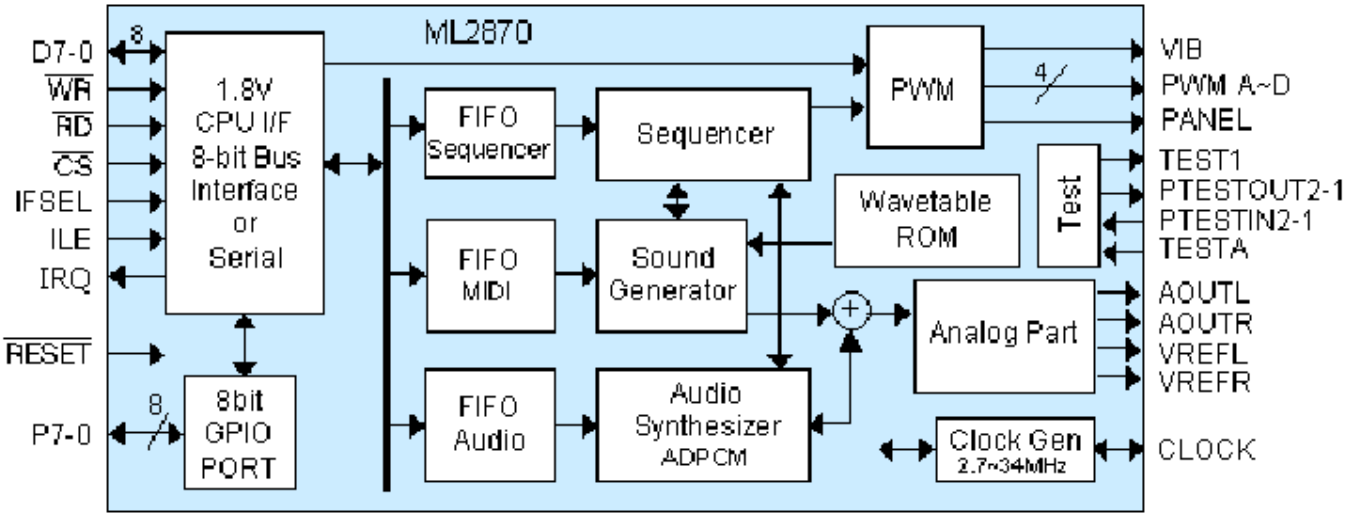


4.0 Reference

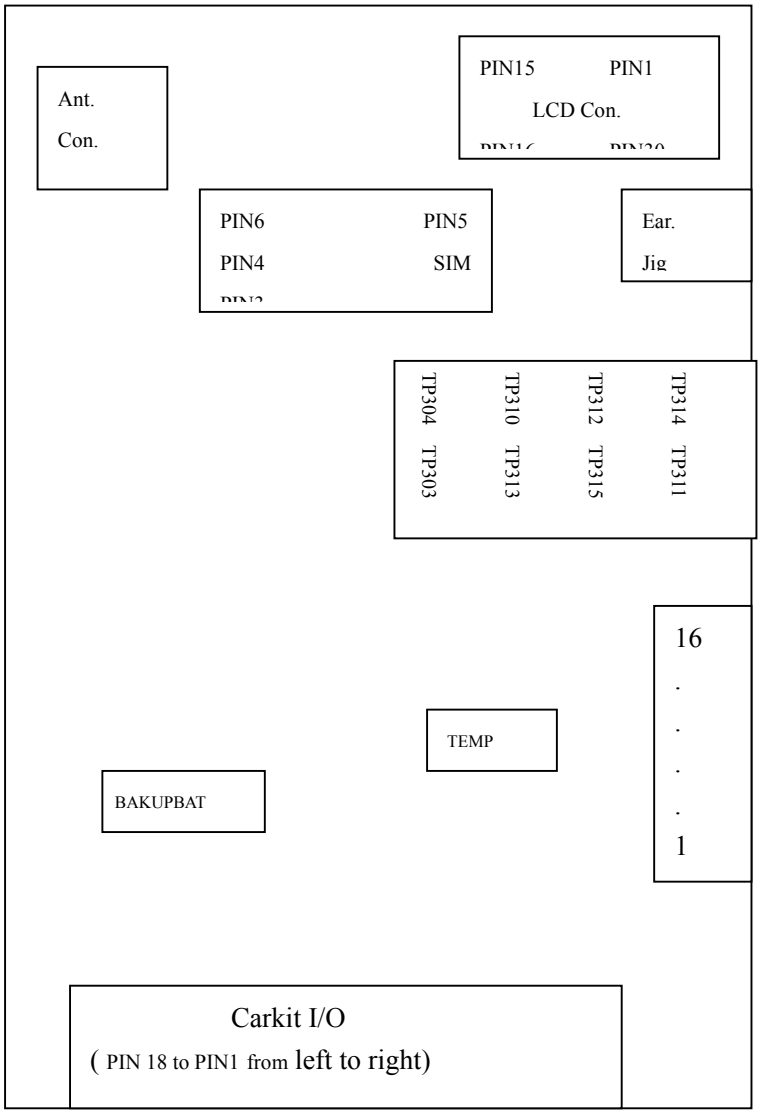
U906-ADG788 function diagram:



U701-ML2870 MIDI function diagram:

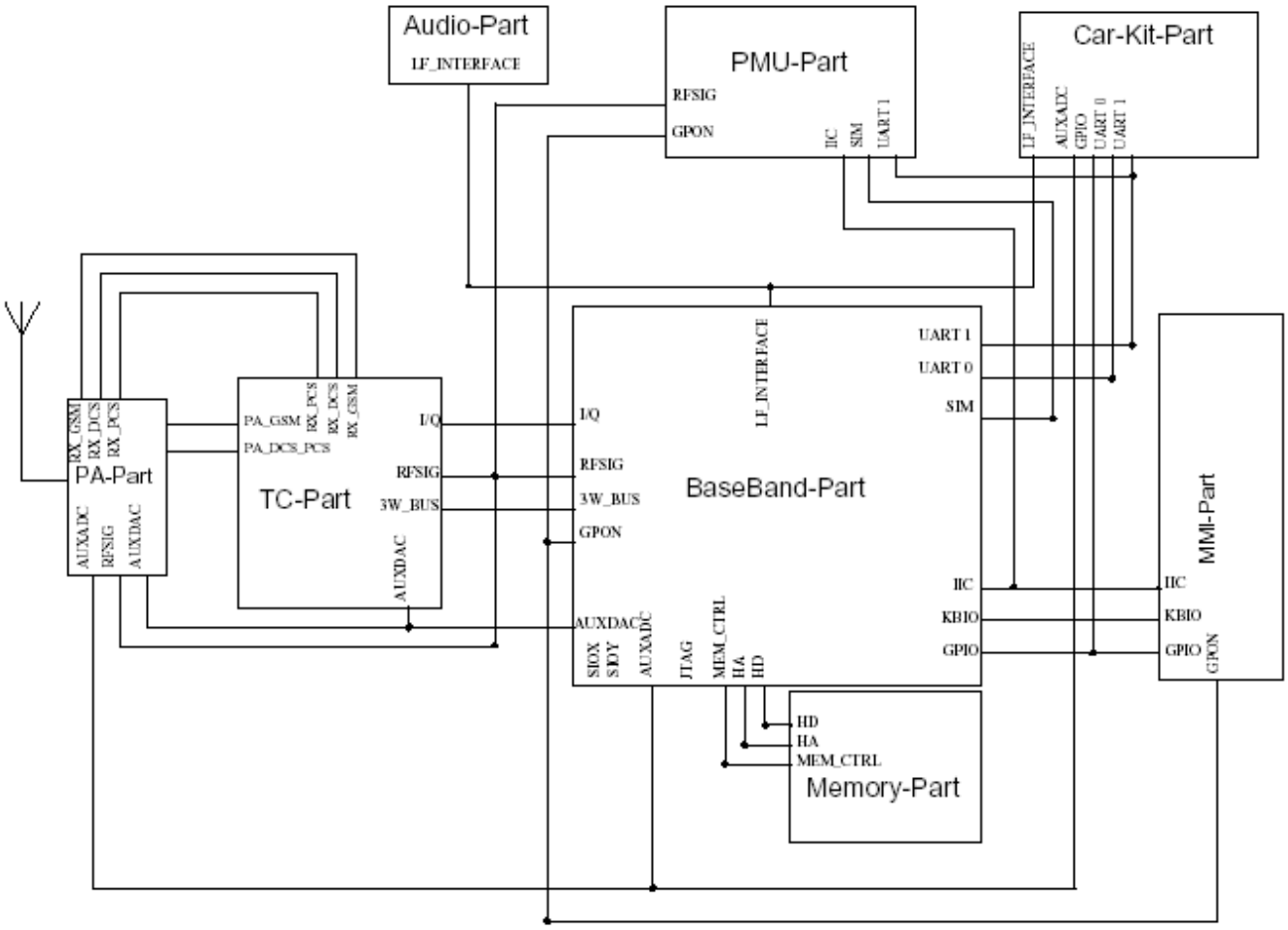


Main board connector:



5.0 Operational Manual

In this part, the operation process is explained by the interfaces.



Solution and its interfaces

5.1 GPIO

The GPIO signals are used as general-purpose I/O pins for various functions. A description of the usage of these pins is shown in table 5.1

GPIO	Name/definition
GPIO(0)	SPEED_MODE
GPIO(1)	FM_DATA
GPI0(2)	AMP_EN
GPIO(3)	CHARGE_REVERSE
GP1O(4)	CHARGE_MODE
GPIO(5)	CAMERA_EN
GPIO(6)	FM_CLK
GPIO(7)	FLIP_SENSE

GPIO(8)	FM_NR_W
GPIO(9)	TEST_CTS(CTS 0)
GPIO(10)	CHARGE_PULSE_IT

Table 5.1 GPIO Interfaces

5.2 GPON

The GPON signals are used as general purpose on pins. A description of the usage of these pins is shown in table 5.2.

Line	Name in schematics	Description
GPON[0]	REF_ON	activation of BAI (inside the OM63xx), sleep mode of PMU
GPON[1]	AUXON	not used
GPON[2]	RSTN_LCD	reset LCD

Table 5.2 GPON Interfaces

5.3 RFSIG

The RFSIG signals are used to control the various functions of the RF-part. A description of the Usage of these pins is shown in table 5.3

Line	Name in schematics	Description
RFSIG[0]	TXVCO_SW1	control line 1 for TXVCO
RFSIG[1]	TXVCO_SW2	control line 2 for TXVCO
RFSIG[2]	TXVCO_SW3	control line 3 for TXVCO
RFSIG[3]	FSW3	control line 3 for Antenna Switchplexer
RFSIG[4]	PON_TX	power on/off TX mode of TC and PA control
RFSIG[5]	(not used)	
RFSIG[6]	FSW2	control line 2 for Antenna Switchplexer
RFSIG[7]	FSW1	control line 1 for Antenna Switchplexer
RFSIG[8]	PON_SYN	power on/off Synthesizer
RFSIG[9]	PON_RF1SW (not used)	test signal to control the switched regulator output RF1SW
RFSIG[10]	TC_RXON	power on/off RX mode of TC
RFSIG[11]	BAI_RXON	power on/off RX mode of BAI
RFSIG[12]	BAI_TXON	power on/off TX mode of BAI

Table 5.3 RFSIG descriptions

5.4 AUXDAC / AUXADC

The AUXDAC / AUXADC signals are used to control and measure some functions of the RF-part. A description of the usage of these pins is shown in table 5.4.

Line	Name in schematics	Description
AUXDAC1	(not used)	
AUXDAC2	AFC	automatic frequency control to adjust the reference clk
AUXDAC3	RAMP	ramping signal for PA controller
AUXADC3	TEMP_PRODUCT	to measure the temperature

Table 5.4 AUXDAC/AUXADE Interfaces

5.5 3WBUS

The 3-wire bus is used to program the transceiver and baseband. These signals are also available on the ST1 connector in the emulation part.

Line	Name in schematics	Description
3WBUS[1]	RF_BBI_CLK	clock
3WBUS[2]	BAI_DO	data line (BAI output data)
3WBUS[3]	RF_BBI_DATA	data line (baseband input data)
3WBUS[4]	RF_EN_TC	enable TC
3WBUS[5]	EN_BBI_IN	enable BAI
3WBUS[6]	(not used)	

Table 5.5 3WBUS Interfaces

5.6 SIOX / SIOY

The SIOX and the SIOY bus are used for communication between BB and BAI. Testing is provided by test points inside the phone application area and by signals on ST1 in the emulation part.

Line	Name in schematics	Test point	Description
SIOX0	BIOCLK	TP22	baseband serial interface clock
SIOX1	BIEN	TP21	baseband serial data enable TX
SIOX2	BOEN	TP20	baseband serial data enable RX
SIOX3	BDIO	TP19	baseband serial data
SIOY0	DU (ADO)	TP18	audio serial TX
SIOY1	DD (ADI)	TP17	audio serial RX
SIOY2	DCL (ACLK)	TP16	audio serial interface clock
SIOY3	FSC (AFS)	TP15	audio serial frame

Table 5.6 SIOX/SIOY Interfaces

5.7 UART0 / UART1

The UART0 part provides an interface for communication with an external terminal. This communication uses automatic baud-rate detection and hardware handshake.
The UART0 can be switched off by software using the line CMD_UART (GPIO 6) if this option is implemented. In that case, lines TEST_RXD and TEST_TXD are disconnected from bottom connector (BU2). Power supply for the UART0 block is VDD2.
The UART1 part provides interface for communication with an external terminal and can be

used only for tracking and testing. This UART does not provide any hardware handshake or automatic baud-rate detection. The signal RXD1 will be used for recognizing future external devices. Power supply for the UART1 block is VDD2.

Line	Name in schematics	Description
UART0_0	TEST_RXD	receive data
UART0_1	TEST_TXD	transmit data
UART0_2	TEST_RTS	request to send
UART0_3	TEST_CTS	clear to send
UART1_0	RXD1	receive data
UART1_1	TXD1	transmit data

Table 5.7 UART Interfaces

5.8 LF_INTERFACE

The LF_INTERFACE signals are used for audio signals from the microphone and to the earpiece as well as for the hands free. A description of the usage of these signals is shown in table 5.8.

Line	Name in schematics	Description
LF_INTERFACE0	EARP1	outputsignal for earpiece
LF_INTERFACE1	EARP2	outputsignal for earpiece
LF_INTERFACE2	AUX_SPK	auxiliary speaker for car kit
LF_INTERFACE3	BUZZER	
LF_INTERFACE4	MIC_AMP_P	amplifier inputsignal from microphone
LF_INTERFACE5	MIC_AMP_N	amplifier inputsignal from microphone
LF_INTERFACE6	AUX_MIC_P	auxiliary microphone input for car kit
LF_INTERFACE7	AUX_MIC_N	auxiliary microphone input for car kit

Table 5.8 LF Interfaces

5.9 SIM

On the K570 Design there are two SIM card connectors. One is in the “phone application” area (ST4) to show the position inside the design and the second one (ST5) is in the emulation area

for testing the K570 Reference Design.
The SIM-card is accessed via the SIM interface. A description of the usage of these signals is shown in table 5.9

Pins	Definition
Pin1	
Pin2	VCC for SIM
Pin3	VCC for SIM
Pin4	Reset for SIM
Pin5	Data line of SIM
Pin6	Clock for SIM

Table 5.9 SIM definitions

5.10 KBIO

The keyboard is organized as a triangular matrix as shown in Table 5.10.
The KBIO pins are available on the EVITA connector (ST2) and on separate KEYBOARD connector (ST3) in the emulation area to have the possibility to connect an external keyboard for ease of use (see figure 5.1).

O\I	KBIO_0	KBIO_1	KBIO_2	KBIO_3	KBIO_4	KBIO_5	KBIO_6	KBIO_7
KBIO_0	-	SEND	-	*	7	4	1	Clear
KBIO_1	-	-	-	0	8	5	2	-
KBIO_2	-	-	-	#	9	6	3	MENU
KBIO_3	-	-	-	-	-	-	-	-
KBIO_4	-	-	-	-	-	J_U	-	J_R
KBIO_5	-	-	-	-	-	-	J_L	-
KBIO_6	-	-	-	-	-	-	-	J_D
KBIO_7	-	-	-	-	-	-	-	-

Table 5.10 KBIO Interfaces

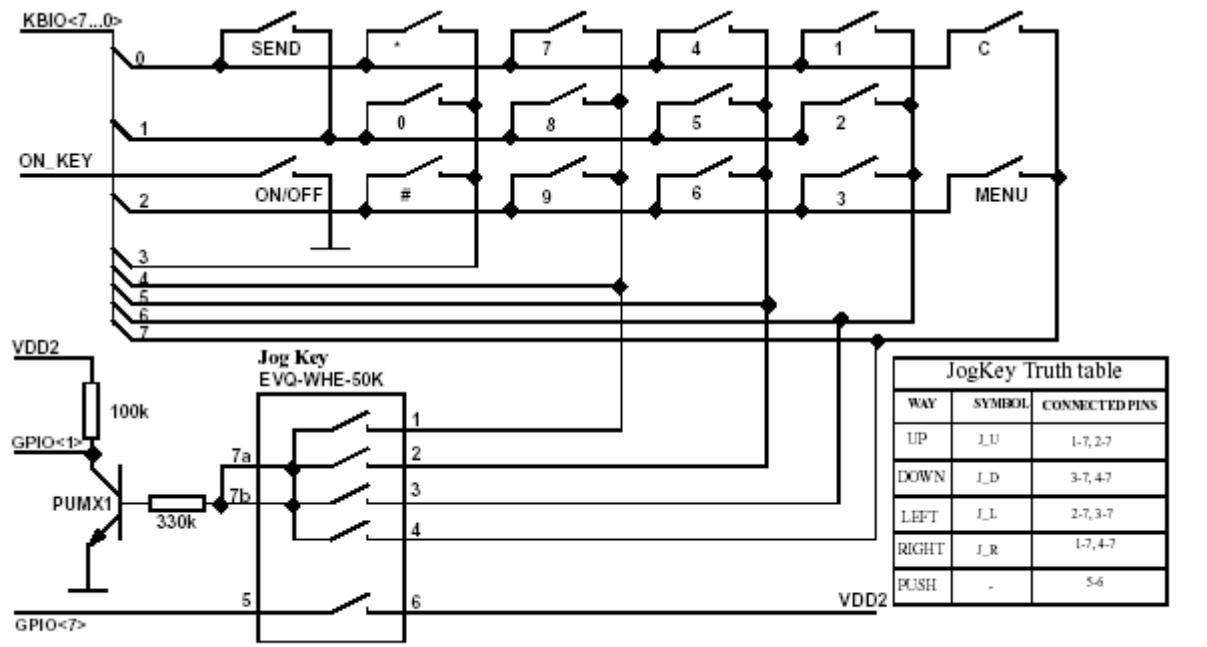


Figure 5.1 KEYBOARD

5.11 I/Q

A description of the usage of the I/Q signals is shown in table 5.11.

Line	Name in schematics	Description
IA	IA	BB differential I signal
IB	IB	BB differential I signal
QA	QA	BB differential Q signal
QB	QB	BB differential Q signal

Table 5.11 I/Q Interfaces

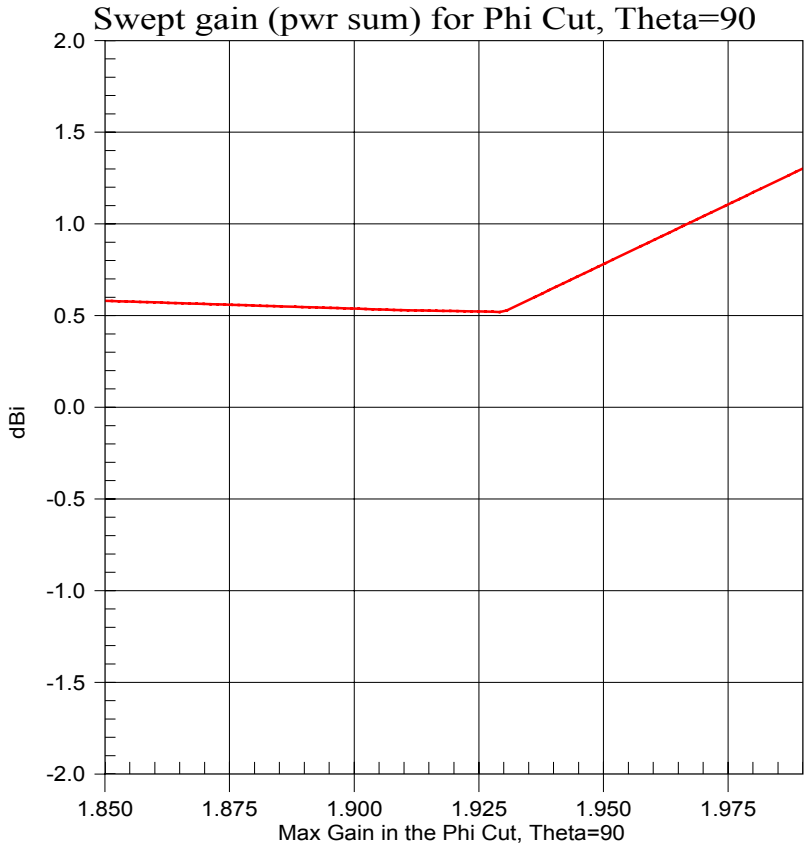
5.12 IIC

The IIC-bus is used for communication between the BB-processor, the PMU and the LCD. A description of the usage of these signals is shown in table 5.12.

Line	Name in schematics	Description
IIC<0>	SCL	IIC clock
IIC<1>	SDA	IIC data

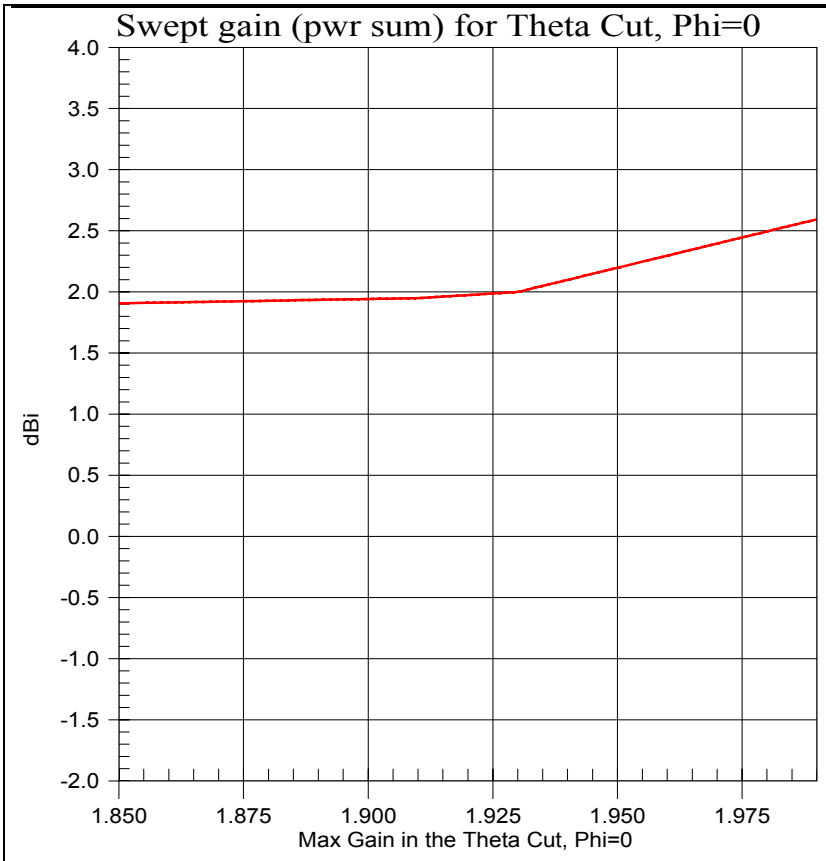
Table 5.12 IIC Interfaces

5.13 Antenna Features of K570



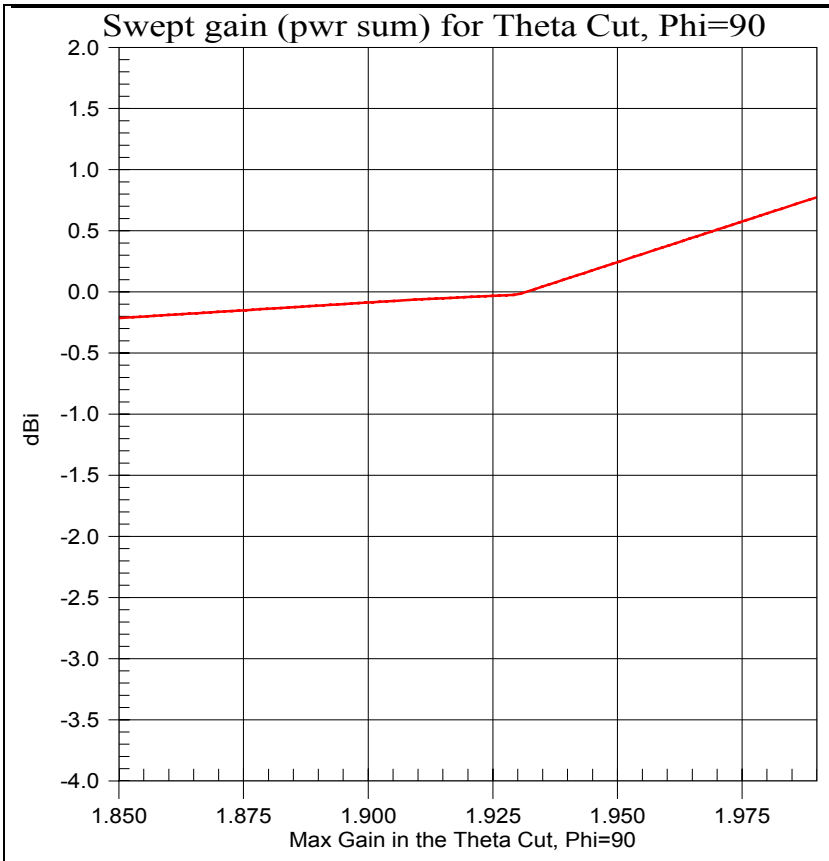
Swept gain (pwr sum) for Phi Cut, Theta=90

PCS band of K570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 0.746dBi



Swept gain (pwr sum) for Theta Cut, Phi=0

PCS band of K570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 2.121dBi



Swept gain (pwr sum) for Theta Cut, Phi=90

PCS band of K570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 0.136dBi

Gain Summary for : Phi Cut, Theta=90

Frequency	Pwr Gn Peak (dBi)	Pwr Gn Ave (dBi)	Pol 1 Peak (dBi)	Pol 1 Ave (dBi)	Pol 2 Peak (dBi)	Pol 2 Ave(dBi)
1.85 GHz	0.580	-3.215	-6.665	-8.442	-0.310	-4.764
1.91 GHz	0.529	-3.328	-5.984	-7.915	-0.555	-5.185
1.93 GHz	0.520	-3.428	-5.928	-7.981	-0.576	-5.303
1.99 GHz	1.302	-2.910	-5.082	-7.147	0.183	-4.964

Gain Summary for : Theta Cut, Phi=0

Frequency	Pwr Gn Peak (dBi)	Pwr Gn Ave (dBi)	Pol 1 Peak (dBi)	Pol 1 Ave (dBi)	Pol 2 Peak (dBi)	Pol 2 Ave(dBi)
1.85 GHz	1.906	-2.151	-3.798	-8.531	0.963	-3.287
1.91 GHz	1.949	-2.574	-2.543	-7.862	0.441	-4.098
1.93 GHz	1.999	-2.719	-2.153	-7.817	0.198	-4.326
1.99 GHz	2.594	-2.568	-0.878	-6.951	0.200	-4.536

Gain Summary for : Theta Cut, Phi=90

Frequency	Pwr Gn Peak (dBi)	Pwr Gn Ave (dBi)	Pol 1 Peak (dBi)	Pol 1 Ave (dBi)	Pol 2 Peak (dBi)	Pol 2 Ave(dBi)
1.85 GHz	-0.215	-4.904	-0.271	-5.249	-10.968	-16.078
1.91 GHz	-0.062	-4.966	-0.112	-5.324	-9.632	-15.986
1.93 GHz	-0.023	-5.006	-0.074	-5.357	-9.227	-16.107
1.99 GHz	0.775	-4.390	0.739	-4.743	-8.129	-15.462

Pwr Gn Peak: Power Gain Peak
Pwr Gn Ave: Power Gain Average
Pol 1 Peak: Polarity 1 Peak
Pol 1 Ave: Polarity 1 Average
Pol 2 Peak: Polarity 2 Peak
Pol 2 Ave: Polarity 2 Average