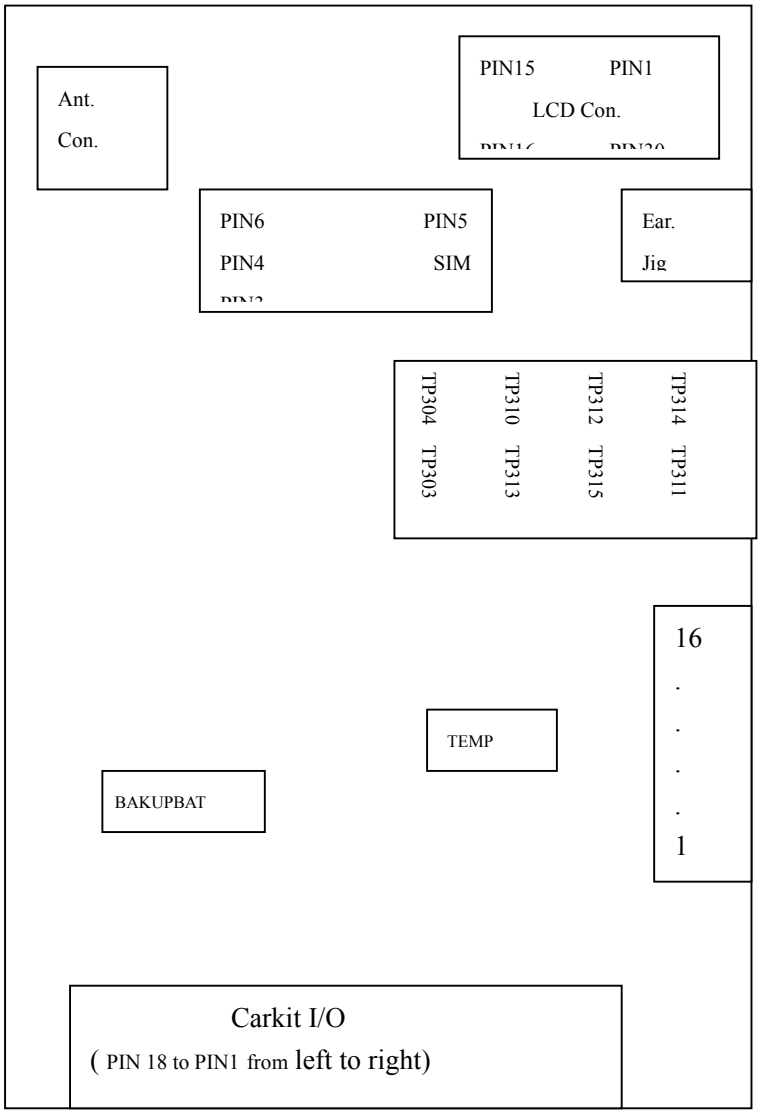
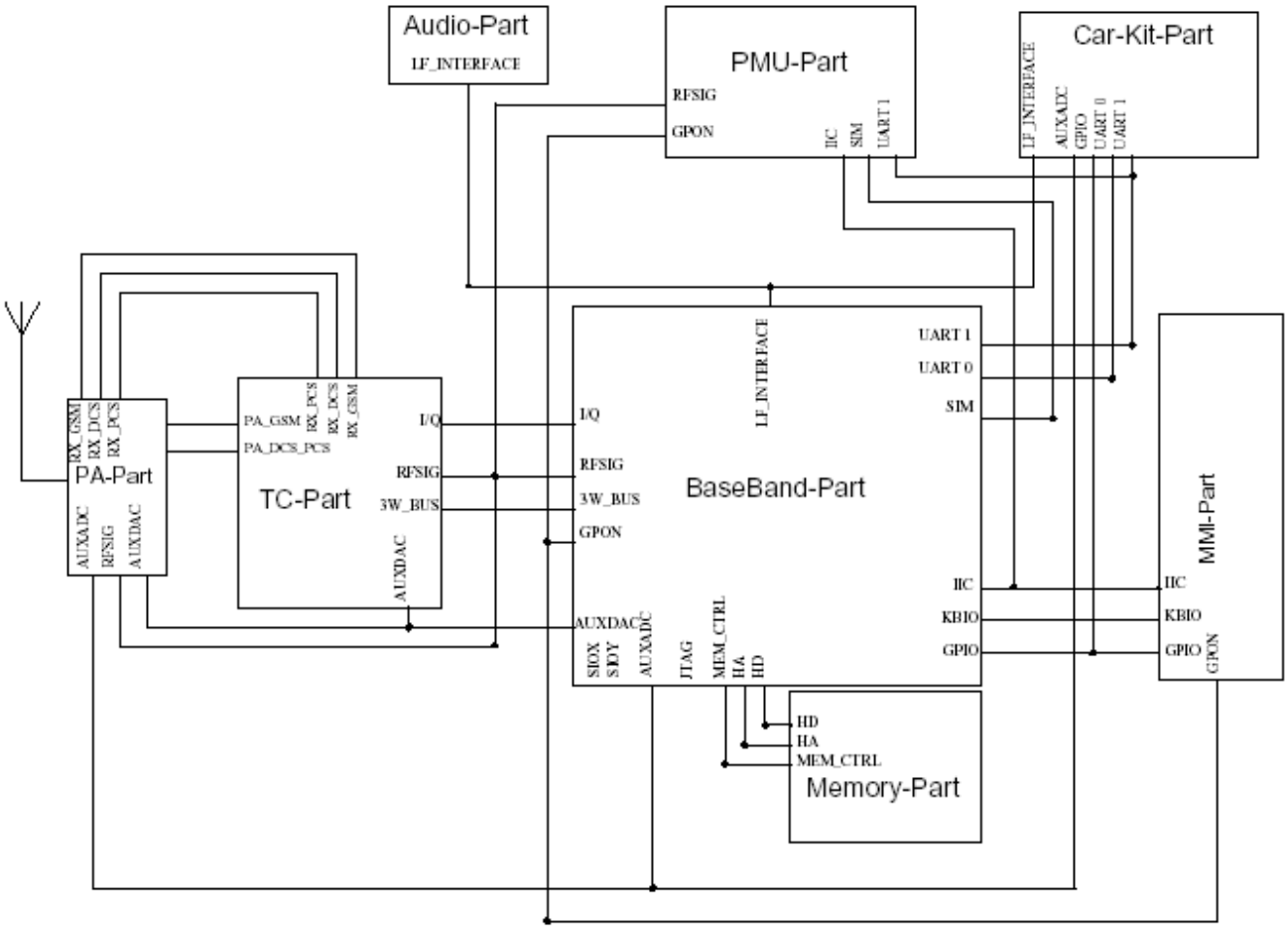
Main board connector:




## 5.0 Operational Manual

In this part, the operation process is explained by the interfaces.




Solution and its interfaces

## 5.1 GPIO

The GPIO signals are used as general-purpose I/O pins for various functions. A description of the usage of these pins is shown in table 5.1

| GPIO | Name/definition |
|---|---|
| GPIO(0) | SPEED_MODE |
| GPIO(1) | FM_DATA |
| GPI0(2) | AMP_EN |
| GPIO(3) | CHARGE_REVERSE |
| GP1O(4) | CHARGE_MODE |
| GPIO(5) | CAMERA_EN |
| GPIO(6) | FM_CLK |
| GPIO(7) | FLIP_SENSE |

| | |
|---|---|
| GPIO(8) | FM_NR_W |
| GPIO(9) | TEST_CTS(CTS 0) |
| GPIO(10) | CHARGE_PULSE_IT |

Table 5.1 GPIO Interfaces

5.2 GPON

The GPON signals are used as general purpose on pins. A description of the usage of these pins is shown in table 5.2.

| Line | Name in schematics | Description |
|---|---|---|
| GPON[0] | REF_ON | activation of BAI (inside the OM63xx), sleep mode of PMU |
| GPON[1] | AUXON | not used |
| GPON[2] | RSTN_LCD | reset LCD |

Table 5.2 GPON Interfaces

5.3 RFSIG

The RFSIG signals are used to control the various functions of the RF-part. A description of the Usage of these pins is shown in table 5.3

| Line | Name in schematics | Description |
|---|---|---|
| RFSIG[0] | TXVCO_SW1 | control line 1 for TXVCO |
| RFSIG[1] | TXVCO_SW2 | control line 2 for TXVCO |
| RFSIG[2] | TXVCO_SW3 | control line 3 for TXVCO |
| RFSIG[3] | FSW3 | control line 3 for Antenna Switchplexer |
| RFSIG[4] | PON_TX | power on/off TX mode of TC and PA control |
| RFSIG[5] | (not used) | |
| RFSIG[6] | FSW2 | control line 2 for Antenna Switchplexer |
| RFSIG[7] | FSW1 | control line 1 for Antenna Switchplexer |
| RFSIG[8] | PON_SYN | power on/off Synthesizer |
| RFSIG[9] | PON_RF1SW (not used) | test signal to control the switched regulator output RF1SW |
| RFSIG[10] | TC_RXON | power on/off RX mode of TC |
| RFSIG[11] | BAI_RXON | power on/off RX mode of BAI |
| RFSIG[12] | BAI_TXON | power on/off TX mode of BAI |

Table 5.3 RFSIG descriptions

## 5.4 AUXDAC / AUXADC

The AUXDAC / AUXADC signals are used to control and measure some functions of the RF-part. A description of the usage of these pins is shown in table 5.4.

| Line | Name in schematics | Description |
|---|---|---|
| AUXDAC1 | (not used) | |
| AUXDAC2 | AFC | automatic frequency control to adjust the reference clk |
| AUXDAC3 | RAMP | ramping signal for PA controller |
| AUXADC3 | TEMP_PRODUCT | to measure the temperature |

Table 5.4 AUXDAC/AUXADE Interfaces

## 5.5 3WBUS

The 3-wire bus is used to program the transceiver and baseband. These signals are also available on the ST1 connector in the emulation part.

| Line | Name in schematics | Description |
|---|---|---|
| 3WBUS[1] | RF_BBI_CLK | clock |
| 3WBUS[2] | BAI_DO | data line (BAI output data) |
| 3WBUS[3] | RF_BBI_DATA | data line (baseband input data) |
| 3WBUS[4] | RF_EN_TC | enable TC |
| 3WBUS[5] | EN_BBI_IN | enable BAI |
| 3WBUS[6] | (not used) | |

Table 5.5 3WBUS Interfaces

## 5.6 SIOX / SIOY

The SIOX and the SIOY bus are used for communication between BB and BAI. Testing is provided by test points inside the phone application area and by signals on ST1 in the emulation part.

| Line | Name in schematics | Test point | Description |
|---|---|---|---|
| SIOX0 | BIOCLK | TP22 | baseband serial interface clock |
| SIOX1 | BIEN | TP21 | baseband serial data enable TX |
| SIOX2 | BOEN | TP20 | baseband serial data enable RX |
| SIOX3 | BDIO | TP19 | baseband serial data |
| SIOY0 | DU (ADO) | TP18 | audio serial TX |
| SIOY1 | DD (ADI) | TP17 | audio serial RX |
| SIOY2 | DCL (ACLK) | TP16 | audio serial interface clock |
| SIOY3 | FSC (AFS) | TP15 | audio serial frame |

Table 5.6 SIOX/SIOY Interfaces

## 5.7 UART0 / UART1

The UART0 part provides an interface for communication with an external terminal. This communication uses automatic baud-rate detection and hardware handshake.
The UART0 can be switched off by software using the line CMD_UART (GPIO 6) if this option is implemented. In that case, lines TEST_RXD and TEST_TXD are disconnected from bottom connector (BU2). Power supply for the UART0 block is VDD2.
The UART1 part provides interface for communication with an external terminal and can be

used only for tracking and testing. This UART does not provide any hardware handshake or automatic baud-rate detection. The signal RXD1 will be used for recognizing future external devices. Power supply for the UART1 block is VDD2.

| Line | Name in schematics | Description |
|---|---|---|
| UART0_0 | TEST_RXD | receive data |
| UART0_1 | TEST_TXD | transmit data |
| UART0_2 | TEST_RTS | request to send |
| UART0_3 | TEST_CTS | clear to send |
| UART1_0 | RXD1 | receive data |
| UART1_1 | TXD1 | transmit data |

Table 5.7 UART Interfaces

## 5.8 LF_INTERFACE

The LF_INTERFACE signals are used for audio signals from the microphone and to the earpiece as well as for the hands free. A description of the usage of these signals is shown in table 5.8.

| Line | Name in schematics | Description |
|---|---|---|
| LF_INTERFACE0 | EARP1 | outputsignal for earpiece |
| LF_INTERFACE1 | EARP2 | outputsignal for earpiece |
| LF_INTERFACE2 | AUX_SPK | auxiliary speaker for car kit |
| LF_INTERFACE3 | BUZZER | |
| LF_INTERFACE4 | MIC_AMP_P | amplifier inputsignal from microphone |
| LF_INTERFACE5 | MIC_AMP_N | amplifier inputsignal from microphone |
| LF_INTERFACE6 | AUX_MIC_P | auxiliary microphone input for car kit |
| LF_INTERFACE7 | AUX_MIC_N | auxiliary microphone input for car kit |

Table 5.8 LF Interfaces

## 5.9 SIM

On the C570 Design there are two SIM card connectors. One is in the “phone application” area (ST4) to show the position inside the design and the second one (ST5) is in the emulation area

for testing the C570 Reference Design.
The SIM-card is accessed via the SIM interface. A description of the usage of these signals is shown in table 5.9

| Pins | Definition |
|---|---|
| Pin1 | |
| Pin2 | VCC for SIM |
| Pin3 | VCC for SIM |
| Pin4 | Reset for SIM |
| Pin5 | Data line of SIM |
| Pin6 | Clock for SIM |

Table 5.9 SIM definitions

5.10 KBIO

The keyboard is organized as a triangular matrix as shown in Table 5.10.
The KBIO pins are available on the EVITA connector (ST2) and on separate KEYBOARD connector (ST3) in the emulation area to have the possibility to connect an external keyboard for ease of use (see figure 5.1).

| O\I | KBIO_0 | KBIO_1 | KBIO_2 | KBIO_3 | KBIO_4 | KBIO_5 | KBIO_6 | KBIO_7 |
|---|---|---|---|---|---|---|---|---|
| KBIO_0 | - | SEND | - | * | 7 | 4 | 1 | Clear |
| KBIO_1 | - | - | - | 0 | 8 | 5 | 2 | - |
| KBIO_2 | - | - | - | # | 9 | 6 | 3 | MENU |
| KBIO_3 | - | - | - | - | - | - | - | - |
| KBIO_4 | - | - | - | - | - | J_U | - | J_R |
| KBIO_5 | - | - | - | - | - | - | J_L | - |
| KBIO_6 | - | - | - | - | - | - | - | J_D |
| KBIO_7 | - | - | - | - | - | - | - | - |

Table 5.10 KBIO Interfaces

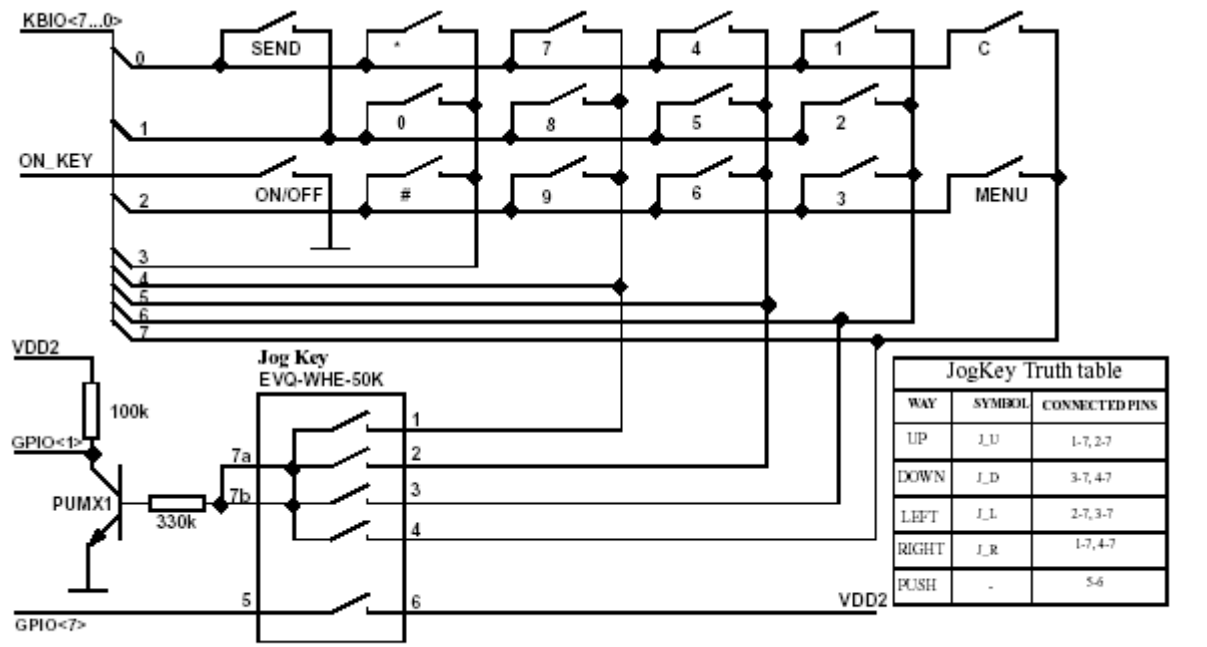



Figure 5.1 KEYBOARD

## 5.11 I/Q

A description of the usage of the I/Q signals is shown in table 5.11.

| Line | Name in schematics | Description |
|---|---|---|
| IA | IA | BB differential I signal |
| IB | IB | BB differential I signal |
| QA | QA | BB differential Q signal |
| QB | QB | BB differential Q signal |

Table 5.11 I/Q Interfaces

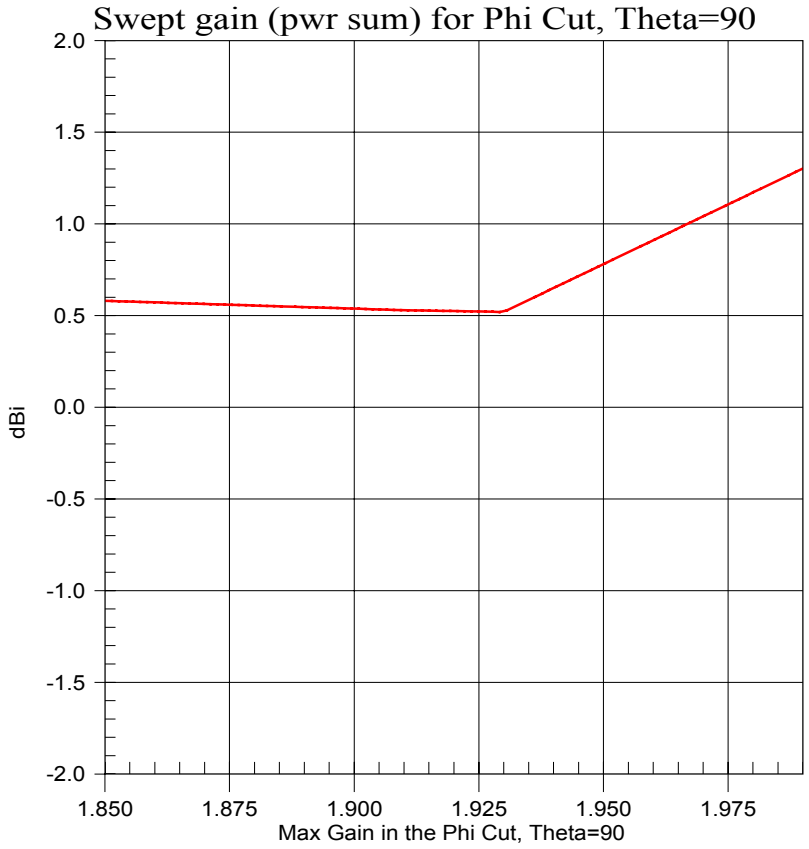
## 5.12 IIC

The IIC-bus is used for communication between the BB-processor, the PMU and the LCD. A description of the usage of these signals is shown in table 5.12.

| Line | Name in schematics | Description |
|---|---|---|
| IIC<0> | SCL | IIC clock |
| IIC<1> | SDA | IIC data |

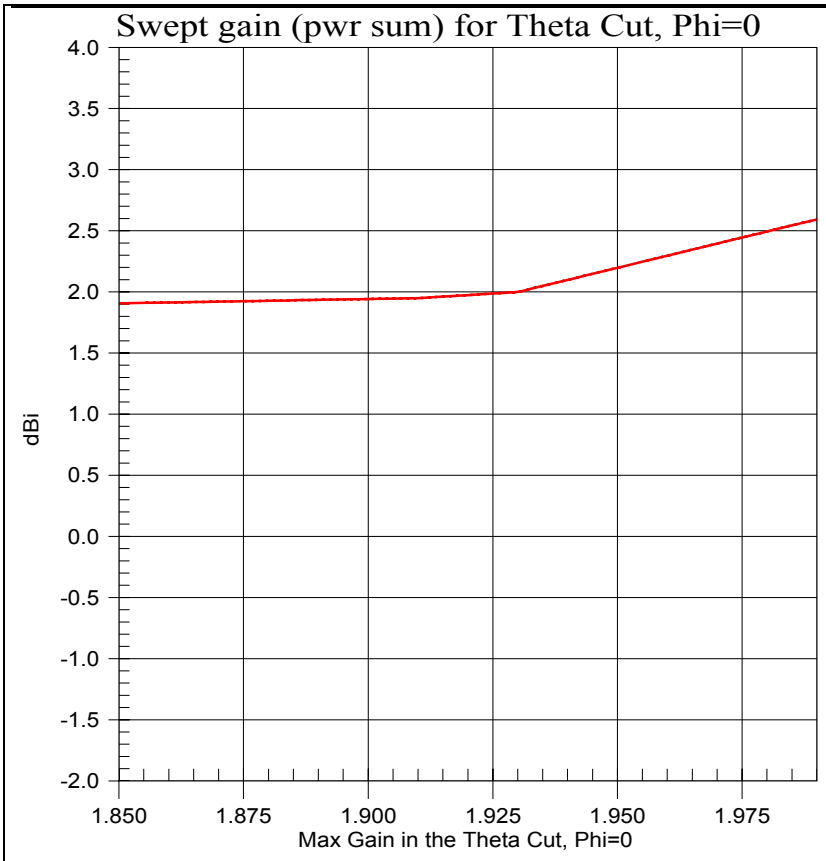
Table 5.12 IIC Interfaces

## 5.13 Antenna Features of C570



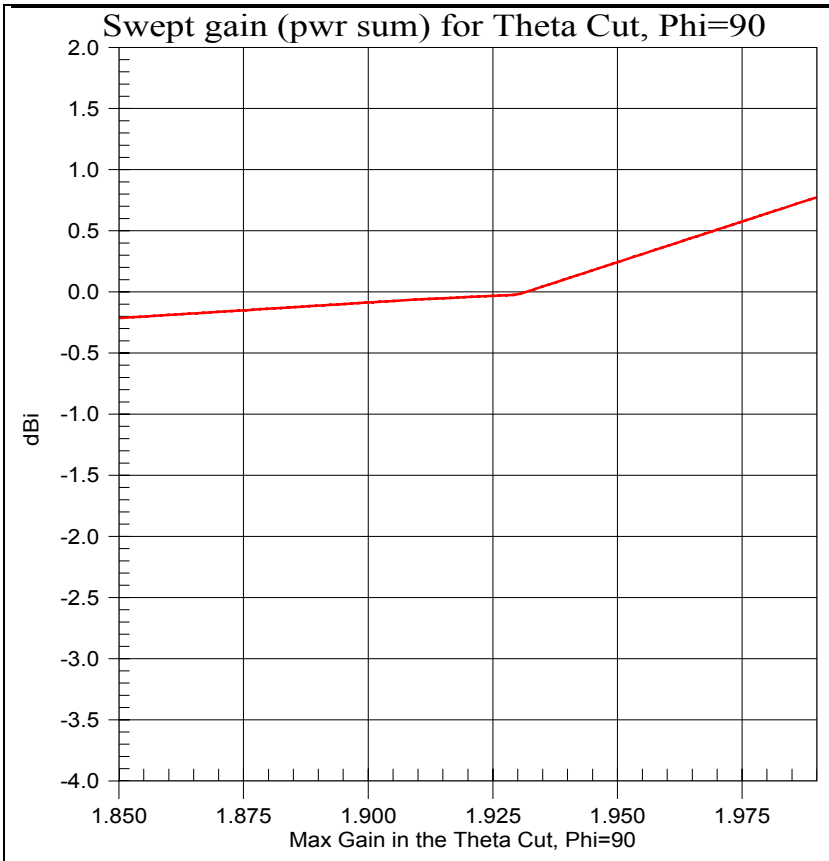

Swept gain (pwr sum) for Phi Cut, Theta=90

PCS band of C570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 0.746dBi




Swept gain (pwr sum) for Theta Cut, Phi=0

PCS band of C570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 2.121dBi




Swept gain (pwr sum) for Theta Cut, Phi=90

PCS band of C570
Computed values are terminal gains - AUT S11 not backed out
Average gain over this frequency range = 0.136dBi

## Gain Summary for : Phi Cut, Theta=90

| Frequency | Pwr Gn Peak (dBi) | Pwr Gn Ave (dBi) | Pol 1 Peak (dBi) | Pol 1 Ave (dBi) | Pol 2 Peak (dBi) | Pol 2 Ave(dBi) |
|---|---|---|---|---|---|---|
| 1.85 GHz | 0.580 | -3.215 | -6.665 | -8.442 | -0.310 | -4.764 |
| 1.91 GHz | 0.529 | -3.328 | -5.984 | -7.915 | -0.555 | -5.185 |
| 1.93 GHz | 0.520 | -3.428 | -5.928 | -7.981 | -0.576 | -5.303 |
| 1.99 GHz | 1.302 | -2.910 | -5.082 | -7.147 | 0.183 | -4.964 |

## Gain Summary for : Theta Cut, Phi=0

| Frequency | Pwr Gn Peak (dBi) | Pwr Gn Ave (dBi) | Pol 1 Peak (dBi) | Pol 1 Ave (dBi) | Pol 2 Peak (dBi) | Pol 2 Ave(dBi) |
|---|---|---|---|---|---|---|
| 1.85 GHz | 1.906 | -2.151 | -3.798 | -8.531 | 0.963 | -3.287 |
| 1.91 GHz | 1.949 | -2.574 | -2.543 | -7.862 | 0.441 | -4.098 |
| 1.93 GHz | 1.999 | -2.719 | -2.153 | -7.817 | 0.198 | -4.326 |
| 1.99 GHz | 2.594 | -2.568 | -0.878 | -6.951 | 0.200 | -4.536 |

## Gain Summary for : Theta Cut, Phi=90

| Frequency | Pwr Gn Peak (dBi) | Pwr Gn Ave (dBi) | Pol 1 Peak (dBi) | Pol 1 Ave (dBi) | Pol 2 Peak (dBi) | Pol 2 Ave(dBi) |
|---|---|---|---|---|---|---|
| 1.85 GHz | -0.215 | -4.904 | -0.271 | -5.249 | -10.968 | -16.078 |
| 1.91 GHz | -0.062 | -4.966 | -0.112 | -5.324 | -9.632 | -15.986 |
| 1.93 GHz | -0.023 | -5.006 | -0.074 | -5.357 | -9.227 | -16.107 |
| 1.99 GHz | 0.775 | -4.390 | 0.739 | -4.743 | -8.129 | -15.462 |

Pwr Gn Peak: Power Gain Peak
Pwr Gn Ave: Power Gain Average
Pol 1 Peak: Polarity 1 Peak
Pol 1 Ave: Polarity 1 Average
Pol 2 Peak: Polarity 2 Peak
Pol 2 Ave: Polarity 2 Average