General Technical Description

Model: CA8a

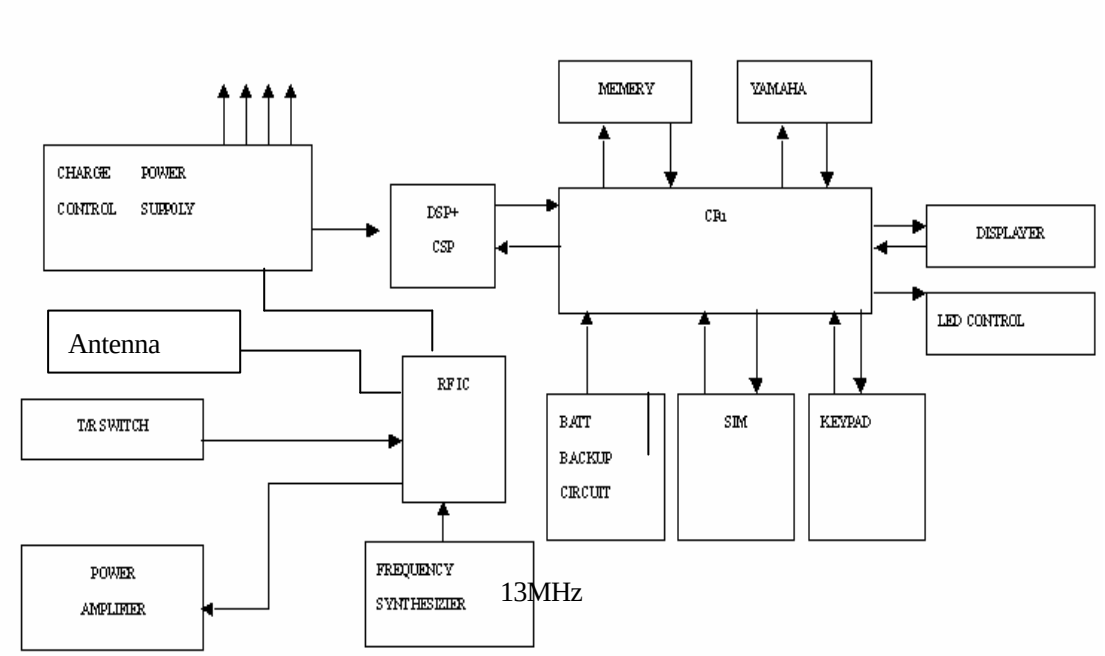
Date: 2005-3-1

Band: EGSM850, DCS1800, PCS 1900

1. Scope

This document is shown and provided the more detail information about the platform used in. The basic description for the Baseband and RF section are also included.

2. Detail Block Diagram



3. RF Front End

RF Front architecture is based on Florence's Carbon highly integrated solution and comprise mainly chips:

3.1 SI4206BM *Transceiver with Direct Conversion*

The SI4206BM supports EGSM850, DCS1800, and PCS 1900 application.

In the transmit path, the device consists of an In-phase and Quadrature(I/Q) modulator within a frequency translation loop designed to perform frequency up-conversion with high output spectral purity. This loop also contains a phase-frequency detector, charge pump, mixer, programmable dividers, and high power transmit Voltage Controlled Oscillators (VCOs) with no external tank required.

The receive path implements a direct down-conversion architecture that eliminates the need for Intermediate Frequency (IF) components. The SI4206BM receiver consists of three integrated Low Noise Amplifiers (LNAs), a quadrature demodulator, tunable receiver baseband filters, and a DC-offset correction sequencer.

3.2 **RF3133** ***Power Amplifier***

The PAM consists of an EGSM850 PA block, a DCS 1800/ PCS 1900 PA block, impedance matching circuitry for 50ohm input and output impedance, and interface circuitry. Two separate Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated on a single Gallium Arsenide (GaAS) die. One PA bock operates in the EGSM900 band and the other PA block supports both the DCS 1800 and the PCS 1900 bands. The assembly is encapsulated with plastic overmold.

4. Baseband

Baseband architecture is based on Florence's Carbon highly integrated solution and comprise mainly three chips:

4.1 **TR09WQTFC15IN2B-DB** ***Digital Baseband Processor***

The baseband processing tasks are divided between the DSP and AVR microprocessor cores. The DSP core executes the physical layer, layer 1, processing functions, and the AVR microprocessor core executes Layer 2 and Layer 3 protocol software and the Man-Machine Interface (MMI) functions.

4.2 **TR09WQTFC15IN2B-DB** ***Integrated Analog Processor***

TR09WQTFC15IN2B-DB implements all the voice-band, mixed signal, and radio control function in a GSM/GPRS handset.

In the transmit path, bursts of digital data are input to the device over the control port. The device Gaussian Minimum-Shift Keying (GMSK) modulator generates modulated I and Q waveforms from the input data. The I and Q waveforms are converted into analog waveforms and output from the device.

In the receive path, the device digitizes the baseband In-Phase / Quadrature (I/Q) input, and outputs the digital samples on the device receive port. The receive path features a programmable gain amplifier (PGA) for Automatic Gain Control (AGC) of the receive signal.

4.3 **M-G-CSP2200B1-YV10-DB** ***Power Management IC***

Power Management Integrated circuit (PMIC) integrates all the power supply and battery charging functions of a low power wireless system into one package. The device is designed for Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) cellular handset applications.

The device contains the following functions:

- Voltage switching, conversion, and regulation
- Power management control logic
- Charging and monitoring of system battery
- SIM interface