# Technical Description

The Equipment Under Test (EUT) is a Stereo Turntable with Bluetooth Receiver and Record Storage Compartment. It can accept input sources such as analog Aux-in (3.5mm phone jack), Phono (Long-Play Record), USB flash memory playback and wireless Bluetooth device. The Bluetooth module in the EUT is operating in the frequency range from 2402MHz to 2480MHz (79 channels with 1MHz channel spacing). The audio signal is amplified and fed to the built-in stereo loudspeakers. The EUT has an analog line-out. It is powered by 120VAC only.

**2.4GHz Bluetooth Module:**
**Modulation Type: GFSK**
**Antenna Type: Integral, Internal (PCB Trace)**
**Frequency Range: 2402MHz - 2480MHz, 1MHz channel spacing, 79 channels**

**Nominal field strength is 90BµV/m @ 3m**
**Production Tolerance of field strength is +/- 3dB**
**Antenna gain is 0dBi**

**The functions of main ICs are mentioned below.**

**1. Bluetooth module (IC4):**
 1) MT6622 acts as the 2.4GHz radio core of Bluetooth module IC4.
 2) 26MHz crystal provides clock for Bluetooth RF IC MT6622.
 3) BM5064 acts as DSP core and CODEC.
 4) 32.768kHz crystal provides clock for BM5064.

**2. Audio portion:**
 1) IC1 (KA8227) is stereo power amplifier for loudspeakers and Line-Out.
 2) IC7 (D4558) is RIAA equalizer of the stereo phono pick-up.

# Channel Frequency Table of Bluetooth Module

| CH. NO. | FRE. | Hex Value | | CH. NO. | FRE. | Hex Value | | CH. NO | FRE. | Hex Value | | CH. NO | FRE. | Hex Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CH0 | 2402MHz | 0 | | CH26 | 2428MHz | 1A | | CH52 | 2454MHz | 34 | | CH78 | 2480MHz | 4E |
| CH1 | 2403MHz | 1 | | CH27 | 2429MHz | 1B | | CH53 | 2455MHz | 35 | | | | |
| CH2 | 2404MHz | 2 | | CH28 | 2430MHz | 1C | | CH54 | 2456MHz | 36 | | | | |
| CH3 | 2405MHz | 3 | | CH29 | 2431MHz | 1D | | CH55 | 2457MHz | 37 | | | | |
| CH4 | 2406MHz | 4 | | CH30 | 2432MHz | 1E | | CH56 | 2458MHz | 38 | | | | |
| CH5 | 2407MHz | 5 | | CH31 | 2433MHz | 1F | | CH57 | 2459MHz | 39 | | | | |
| CH6 | 2408MHz | 6 | | CH32 | 2434MHz | 20 | | CH58 | 2460MHz | 3A | | | | |
| CH7 | 2409MHz | 7 | | CH33 | 2435MHz | 21 | | CH59 | 2461MHz | 3B | | | | |
| CH8 | 2410MHz | 8 | | CH34 | 2436MHz | 22 | | CH60 | 2462MHz | 3C | | | | |
| CH9 | 2411MHz | 9 | | CH35 | 2437MHz | 23 | | CH61 | 2463MHz | 3D | | | | |
| CH10 | 2412MHz | A | | CH36 | 2438MHz | 24 | | CH62 | 2464MHz | 3E | | | | |
| CH11 | 2413MHz | B | | CH37 | 2439MHz | 25 | | CH63 | 2465MHz | 3F | | | | |
| CH12 | 2414MHz | C | | CH38 | 2440MHz | 26 | | CH64 | 2466MHz | 40 | | | | |
| CH13 | 2415MHz | D | | CH39 | 2441MHz | 27 | | CH65 | 2467MHz | 41 | | | | |
| CH14 | 2416MHz | E | | CH40 | 2442MHz | 28 | | CH66 | 2468MHz | 42 | | | | |
| CH15 | 2417MHz | F | | CH41 | 2443MHz | 29 | | CH67 | 2469MHz | 43 | | | | |
| CH16 | 2418MHz | 10 | | CH42 | 2444MHz | 2A | | CH68 | 2470MHz | 44 | | | | |
| CH17 | 2419MHz | 11 | | CH43 | 2445MHz | 2B | | CH69 | 2471MHz | 45 | | | | |
| CH18 | 2420MHz | 12 | | CH44 | 2446MHz | 2C | | CH70 | 2472MHz | 46 | | | | |
| CH19 | 2421MHz | 13 | | CH45 | 2447MHz | 2D | | CH71 | 2473MHz | 47 | | | | |
| CH20 | 2422MHz | 14 | | CH46 | 2448MHz | 2E | | CH72 | 2474MHz | 48 | | | | |
| CH21 | 2423MHz | 15 | | CH47 | 2449MHz | 2F | | CH73 | 2475MHz | 49 | | | | |
| CH22 | 2424MHz | 16 | | CH48 | 2450MHz | 30 | | CH74 | 2476MHz | 4A | | | | |
| CH23 | 2425MHz | 17 | | CH49 | 2451MHz | 31 | | CH75 | 2477MHz | 4B | | | | |
| CH24 | 2426MHz | 18 | | CH50 | 2452MHz | 32 | | CH76 | 2478MHz | 4C | | | | |
| CH25 | 2427MHz | 19 | | CH51 | 2453MHz | 33 | | CH77 | 2479MHz | 4D | | | | |

# MEDIATEK

# MT6622

# Bluetooth V2.1+EDR/V3.0 single chip

Version:          1.5

Release date:     2013-11-25

Specifications are subject to change without notice.

# Document Revision History

| Revision | Date | Author | Description |
|----------|------|--------|-------------|
| 0.1 | 2011-03-09 | PC Lin | Initial Draft |
| 1.0 | 2011-05-30 | Jason Hung | Fix BT Sleep mode power description and update order information |
| 1.1 | 2011-06-15 | Jason Hung | Add new part number of WLCSP package |
| 1.2 | 2011-09-19 | Jason Hung | Add interface signal specification |
| 1.3 | 2011-11-04 | Jason Hung | Add interface signal specification, WLCSP POD |
| 1.4 | 2012-03-28 | Jason Hung | Add support Bluetooth spec. V3.0 |
| 1.5 | 2012-05-29 | Jason Hung | Fix some typo |

# TABLE OF CONTENTS

# 1    System overview

## 1.1    General description

MT6622 is a monolithic single chip that integrates Bluetooth V2.1+EDR/V3.0. It can be incorporated in varieties of mobile platforms to provide Bluetooth connectivity.

MT6622 is available in QFN40 and WLCSP package. With a very small package size and require few external BOM components, a compact footprint can be designed for today's slim mobile device.

Unparalleled performance of sensitivity and interference rejection featured, MT6622 also provides uncompromising low power performance. It also supports 10dBm transmit power with efficient power control, which provide the user with excellent link quality.

## 1.2    Features

■ **BT Radio features**

- Fully compliant with Bluetooth specification V2.1+EDR / V3.0

- Low out-of-band spurious emissions supports simultaneous operation with GPS, GSM/GPRS worldwide radio systems

- Integrated balun

- Supports low power scan mode support

- Fully integrated power amplifier provides 10dBm (class 1) output power

- -95dBm sensitivity with excellent interference rejection performance

- AGC dynamically adjusts receiver performance in changing environments

■ **BT Baseband features**

- Up to 4 simultaneous active ACL links

- Support SCO and eSCO link with re-transmission

- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan

- Sniff mode support

- AFH and PTA collaborative support for WLAN/BT coexistence

- PCM interface and built-in transcoders for A-law, μ-law and linear voice with re-transmission support.

- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening, and encryption

- Channel quality driven data rate adaptation

- Channel assessment for AFH

■ **Platform features**

- 32-bit RISC microprocessor

- Integrated LDO enables direct connection to battery.

- Wide range of frequency of crystal and external reference clock support.

- High speed UART supports up to 4Mbps baud rate

- Built-in RAM and ROM with patch system.

- External LPO clock support for sleep mode.

- Supports standard HCI interface.

- Idle mode and sleep mode design enables ultra low power performance

## 1.3    Applications

A typical example with connection to a baseband chip of a cellular phone is illustrated in **Figure 1**. The UART interface supports hardware flow control as well as high-speed baud rate connection. Both master and slave operating mode are provided on PCM interface with programmable data frequency to connect to the voice channel on the host chip. The PTA interface accommodates different arbitration scheme in which channel utilization can be efficiently performed in a co-existence environment. The external reference clock interface supports wide ranges of frequency common to mobile phone applications.
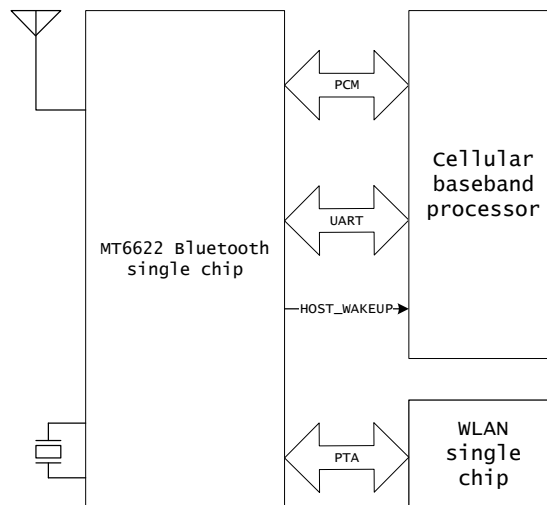
*Figure 1 Mobile phone application.*

## 1.4    Block diagram

The connections between internal modules, as well as, external interfaces can be found in **Figure 2**. The Bluetooth transceiver section of MT6622 incorporates the complete receiving and transmitting paths, including PLL, VCO, LNA, PA, modulator, and demodulator. The Bluetooth baseband signal processor incorporates hardware engines to perform frequency hopping, error correcting, whitening, encrypting, data packet assembling.



*Figure 2 MT6622 functional block diagram*

# 2 Product description

## 2.1 Pin description

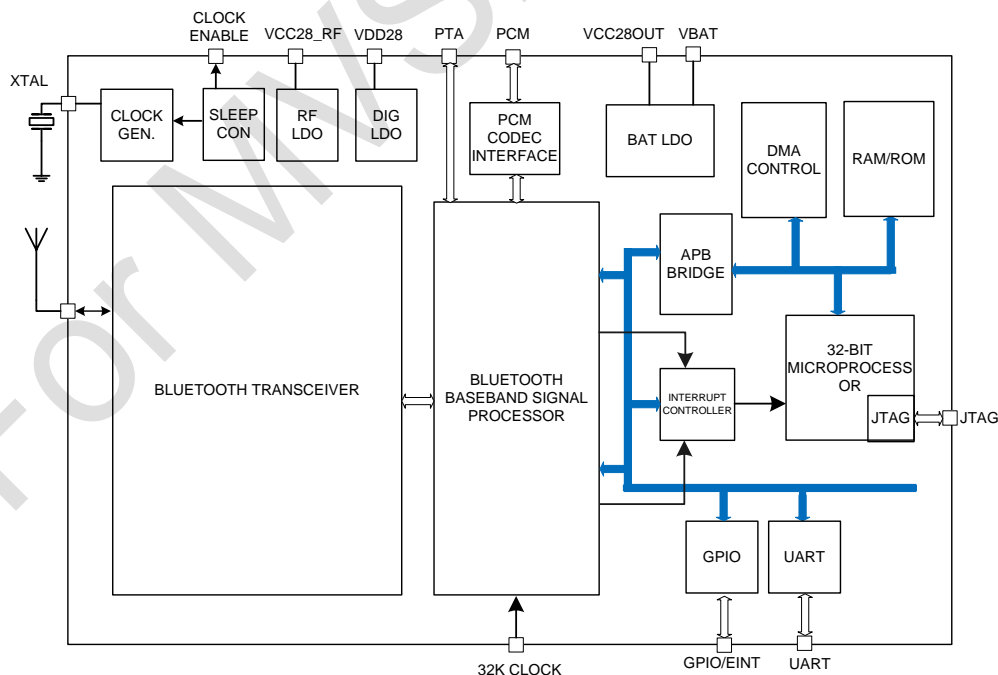| QFN40 lead | WLCSP Ball | Pin Name | Pin description | Default PU/PD | I/O | Supply domain |
|---|---|---|---|---|---|---|
| **Test, reset, and clocks** | | | | | | |
| 38 | B5 | TESTMODE | Test mode enable<br>1: test mode.<br>0: normal mode. | PD | Input | VDD28 |
| 2 | C4 | SYSRST_B | External system reset active low<br>1: normal mode.<br>0: reset. | PU | Input | VDD28 |
| 13 | D1 | OSC_IN | Crystal input or external clock input | N/A | Input | AVDD28_SX |
| 37 | D6 | SRCLKENA | Source clock enable to the host or the oscillator.<br>1: ask host to give MT6622 reference clock. (BT Active or Idle mode)<br>0: inform host that MT6622 doesn't need reference clock. (BT Sleep or power off mode) | N/A | Output | VDD28 |
| 39 | E6 | EXT32K | External 32KHz or 32.768KHz low power clock input. Its worst case accuracy is +-250ppm (same as BT spec). | PD | Input | VDD28 |
| 26 | | ECLK_SEL | External clock select<br>0: enable crystal oscillator in MT6622.<br>1: disable crystal oscillator in MT6622 but enable external clock path. | N/A | Input | VDD28 |
| **UART interface** | | | | | | |
| 40 | C5 | UTXD1 | UART data output active high | PU | Input | VDD28 |
| 1 | D5 | URXD1 | UART data input active high | PU | Input | VDD28 |
| **PCM interface** | | | | | | |
| 4 | D4 | PCMCLK | PCM interface clock. Default in slave mode. | PD | Input | VDD28 |
| 3 | E5 | PCMSYNC | PCM interface sync. Default in slave mode. | PD | Input | VDD28 |
| 7 | E3 | PCMOUT | PCM synchronous data out | PU | Output | VDD28 |
| 6 | E4 | PCMIN | PCM synchronous data in | PU | Input | VDD28 |
| **PTA interface and programmable I/O** | | | | | | |
| 27 | A6 | GPIO4/BT2WIFI | Programmable input/output/WiFi coexistence | PD | Input | VDD28 |

| 24 | A5 | WIFI2BT | WiFi coexistence | PD | Input | VDD28 |
|---|---|---|---|---|---|---|
| 36 | B6 | GPIO0 | Programmable input/output | PU | Input | VDD28 |
| 28 | | GPIO1 | Programmable input/output | PU | Input | VDD28 |
| 25 | | GPIO2 | Programmable input/output | PD | Input | VDD28 |
| 29 | | GPIO3 | Programmable input/output | PU | Input | VDD28 |
| 30 | | GPIO6 | Programmable input/output | PD | Input | VDD28 |
| 31 | | GPIO7 | Programmable input/output | PU | Input | VDD28 |
| 32 | | GPIO8 | Programmable input/output | PD | Input | VDD28 |
| 33 | | GPIO9 | Programmable input/output | PD | Input | VDD28 |
| **Bluetooth radio interface** | | | | | | |
| 22 | A2 | RF2G_N | RF input | N/A | Input | AVDD28_TRX |
| 21 | A1 | AVSS_BALUN | RF BALUN ground | N/A | | |
| 20 | B1 | REXT (RES_IN) | 15K ohm biasing resistor | N/A | | |
| **LDOs** | | | | | | |
| 12 | C3 | LDO28EN | VBAT linear regulator enable control<br>1: power on MT6622.   (voltage spec: VIH>1.5V)<br>0: power down MT6622. (voltage spec: VIL<0.8V) | N/A | Input | |
| 11 | E1 | VBAT | VBAT linear regulator input | N/A | Input | |
| 10 | E2 | VCC28OUT | VBAT linear regulator output for Bluetooth and digital circuit. | N/A | Output | |
| 8 | | VCC28_BBLDO | Digital linear regulator input | N/A | Input | |
| 9 | D3 | LDODVOUT12 | Digital linear regulator output | N/A | Output | |
| **Power supplies** | | | | | | |
| 35 | C6 | VDD28 | Digital I/O power supply | N/A | Input | |
| 5, 34 | D3 | VDD12 | Digital core power supply | N/A | | |
| 14, 15 | C1 | AVDD28_SX | Bluetooth RF 2.8V power supply | N/A | Input | |
| 23 | A3 | AVDD28_TRX | Bluetooth RF 2.8V power supply | N/A | Input | |
| E-PAD | A4 | DVSS | Digital ground | N/A | | |
| E-PAD | B2,B4,C2,D2 | AVSS28_RF | RF/PMU ground | N/A | | |
| **Debug and unconnected pins** | | | | | | |
| 18 | | T1N | RF test pin | N/A | Output | |

| 17 | B3 | T1P | RF test pin | N/A | Output | |
|----|----|-----|-------------|-----|--------|--|
| 16 | | VCO_MONITOR | RF test pin | N/A | N/A | |
| 19 | | N/C | Reserved | N/A | | |

**Table 1** Pin description

## 2.2 Package information

### 2.2.1 QFN40 pin map

| | | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | UTXD1 | EXT32K | TESTMODE | SRCLKENA | GPIO0 | VDD28 | VDD12 | GPIO9 | GPIO8 | GPIO7 | | |
| 1 | URXD1 | | | | | | | | | | | GPIO6 | 30 |
| 2 | SYSRST_B | | | | | | | | | | | GPIO3 | 29 |
| 3 | PCMSYNC | | | | | | | | | | | GPIO1 | 28 |
| 4 | PCMCLK | | | | | | | | | | | GPIO4/BT2WIFI | 27 |
| 5 | VDD12 | | | | | Exposed pad | | | | | | ECLK_SEL | 26 |
| 6 | PCMIM | | | | | | | | | | | GPIO2 | 25 |
| 7 | PCMOUT | | | | | | | | | | | WIFI2BT | 24 |
| 8 | VCC28_BBLDO | | | | | | | | | | | AVDD28_TRX | 23 |
| 9 | LDODVOUT12 | | | | | | | | | | | RF2G_N | 22 |
| 10 | VCC28OUT | | | | | | | | | | | AVSS_BALUN | 21 |
| | | VBAT | LDO28EN | OSC_IN | AVDD28_SX | AVDD28_SX | VCO_MONITOR | T1P | T1N | Not connected | REXT | | |
| | | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | | |

***Figure 3*** Top view of MT6622 QFN pin-out.

## 2.2.2    QFN40 Package dimensions



LASER MARK FOR PIN 1
IDENTIFICATION IN THIS AREA

TOP VIEW

SIDE VIEW

BOTTOM VIEW

\* CONTROLLING DIMENSION : MM

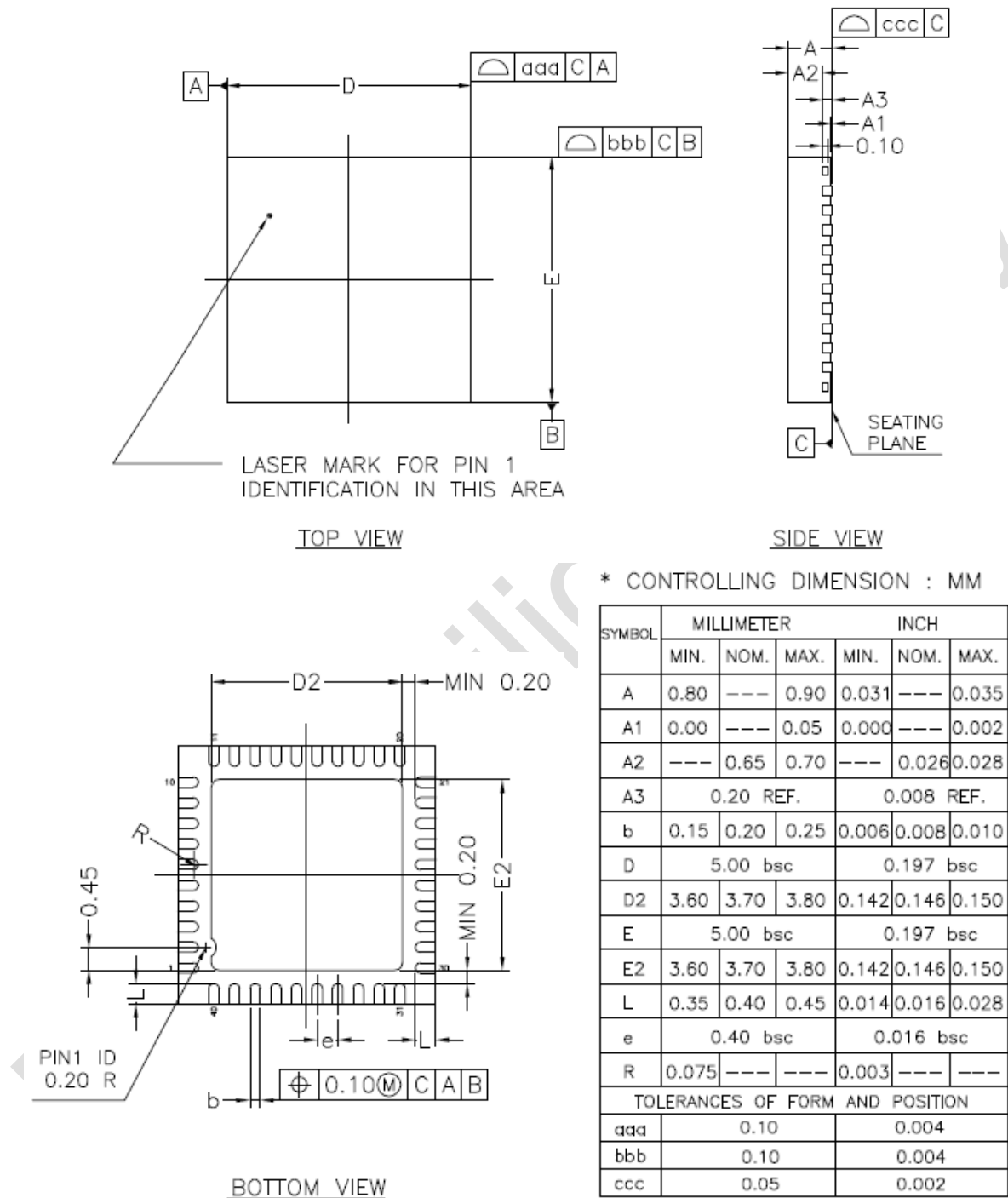| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | --- | 0.90 | 0.031 | --- | 0.035 |
| A1 | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |
| A2 | --- | 0.65 | 0.70 | --- | 0.026 | 0.028 |
| A3 | 0.20 REF. | | | 0.008 REF. | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 5.00 bsc | | | 0.197 bsc | | |
| D2 | 3.60 | 3.70 | 3.80 | 0.142 | 0.146 | 0.150 |
| E | 5.00 bsc | | | 0.197 bsc | | |
| E2 | 3.60 | 3.70 | 3.80 | 0.142 | 0.146 | 0.150 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.028 |
| e | 0.40 bsc | | | 0.016 bsc | | |
| R | 0.075 | --- | --- | 0.003 | --- | --- |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

*Figure 4* **Package outline and dimensions of QFN40 5mm x 5mm, 0.4mm pitch Package**

## 2.2.3 WLCSP ball map

MT6622 WLCSP is a compact 30-pin chip-scale package. The ball coordinate is listed in Table 2.
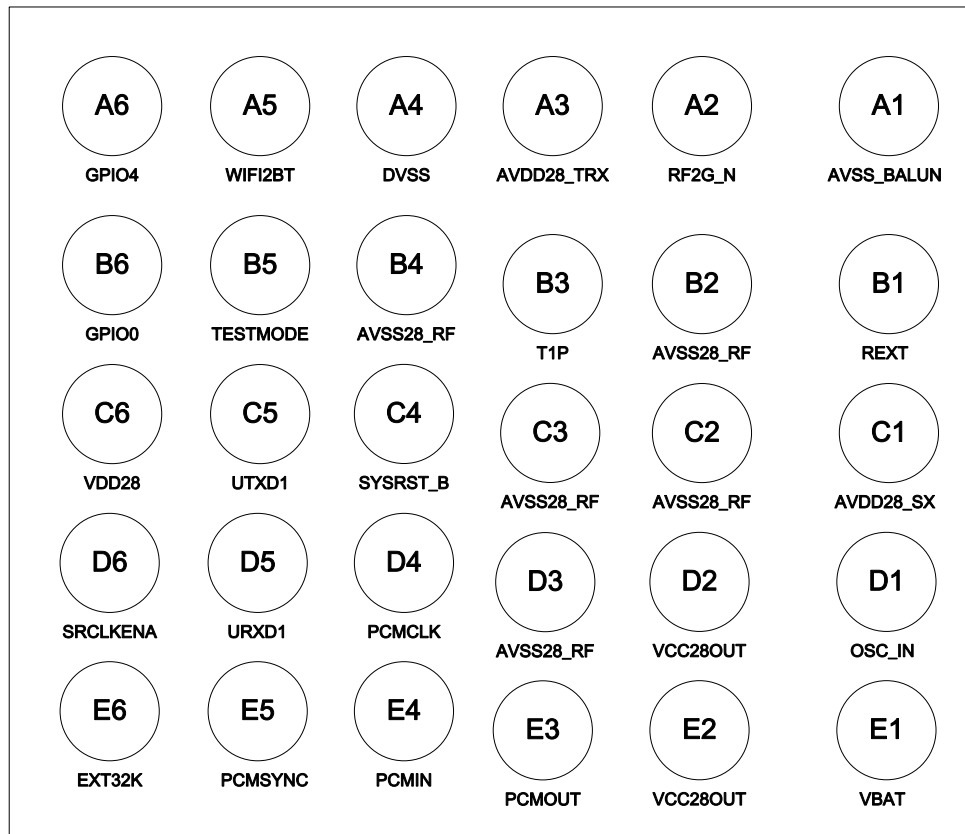


*Figure 5 Bottom view of MT6622 WLCSP ball map*
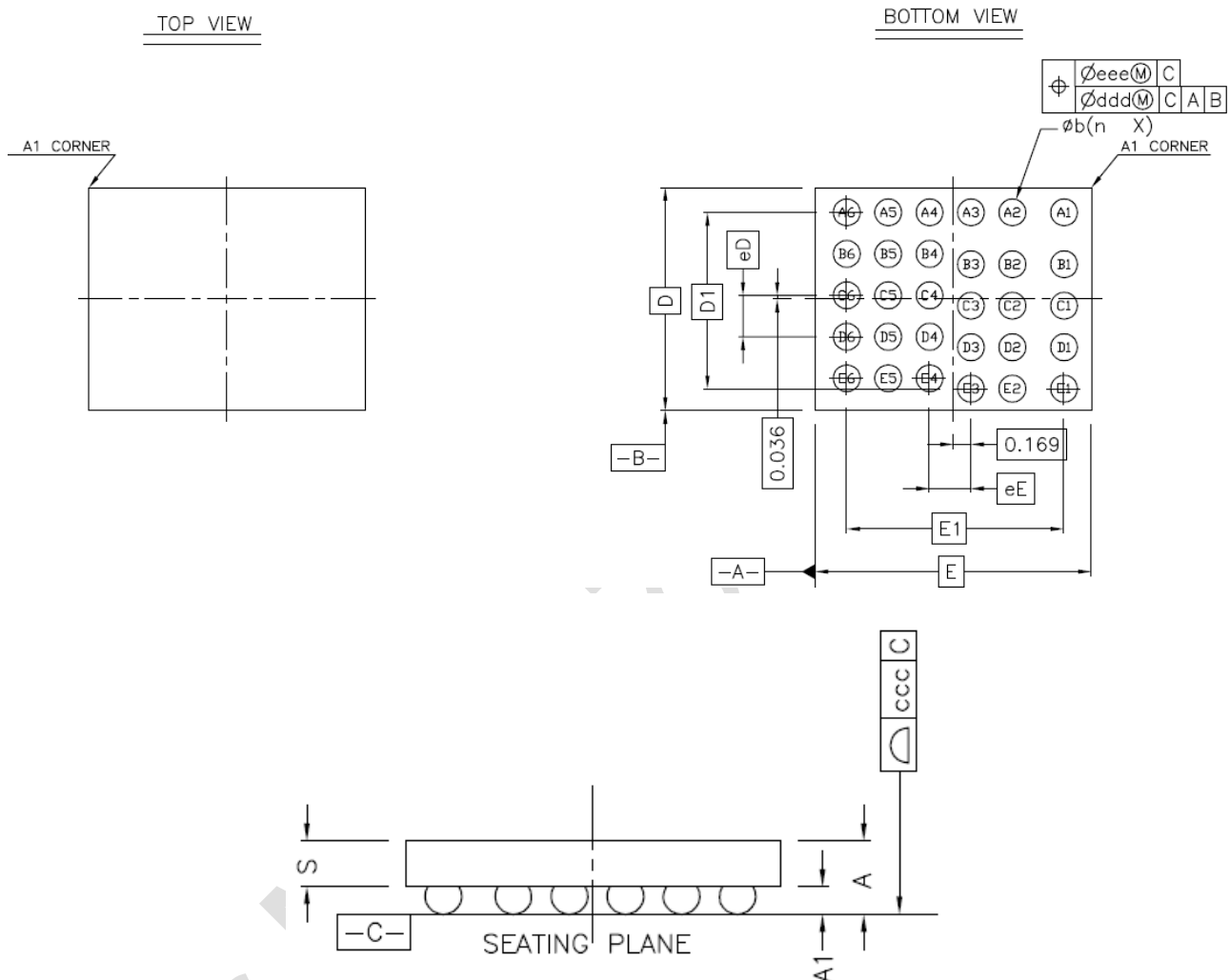
### 2.2.4 WLCSP Package dimensions



*Figure 6 Package outline and dimensions of WLCSP 3.047mm x 2.552mm Package*

The detailed ball coordinates is shown below for accurate reference:

| Ball | Location X (um) | Location Y (um) | Ball | Location X (um) | Location Y (um) |
|------|-----------------|-----------------|------|-----------------|-----------------|
| A1 | 1068.97 | 836.07 | D1 | 1068.97 | -436.07 |
| A2 | 568.97 | 836.07 | D2 | 568.97 | -436.07 |
| A3 | 168.97 | 836.07 | D3 | 168.97 | -436.07 |
| A4 | -231.03 | 836.07 | D4 | -231.03 | -336.07 |
| A5 | -631.03 | 836.07 | D5 | -631.03 | -336.07 |
| A6 | -1031.03 | 836.07 | D6 | -1031.03 | -336.07 |
| B1 | 1068.97 | 336.07 | E1 | 1068.97 | -836.07 |
| B2 | 568.97 | 336.07 | E2 | 568.97 | -836.07 |
| B3 | 168.97 | 336.07 | E3 | 168.97 | -836.07 |

| B4 | -231.03 | 436.07 | E4 | -231.03 | -736.07 |
|----|---------|--------|----|---------|---------|
| B5 | -631.03 | 436.07 | E5 | -631.03 | -736.07 |
| B6 | -1031.03 | 436.07 | E6 | -1031.03 | -736.07 |
| C1 | 1068.97 | -63.93 | | | |
| C2 | 568.97 | -63.93 | | | |
| C3 | 168.97 | -63.93 | | | |
| C4 | -231.03 | 36.07 | | | |
| C5 | -631.03 | 36.07 | | | |
| C6 | -1031.03 | 36.07 | | | |

*Table 2 WLCSP Ball Coordinates*

### 2.2.5    Top marking

```
MTK
MT6622N
DDDD-AF&L
BBBBBBB
```

```
MT6622N  : Part number
DDDD     : Date code
&        : Subcontractor code
BBBBBBB  : Lot number
```

*Figure 7 MT6622N product marking (QFN Package)*

```
MTK
MT6622P
DDDD-AF&H
BBBBBBB
```
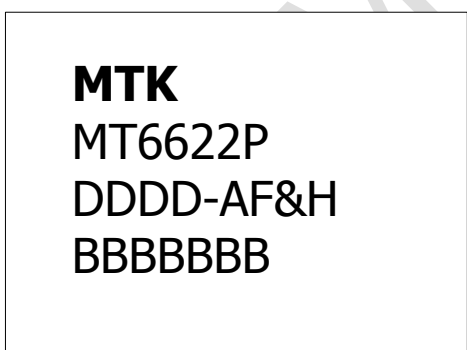
```
MT6622P  : Part number
DDDD     : Date code
&        : Subcontractor code
BBBBBBB  : Lot number
```

*Figure 8 MT6622P product marking (WLCSP Package)*

**MEDIATEK**

```
MTK
MT6622BP
DDDD-AF&H
BBBBBBB
```

```
MT6622BP : Part number
DDDD     : Date code
&        : Subcontractor code
BBBBBBB  : Lot number
```

*Figure 9 MT6622BP product marking (WLCSP Package)*

## 2.3    Ordering information

| Part number | Package | Operational temperature range |
|---|---|---|
| MT6622N/B-L | 5x5x0.9 mm 40-QFN | -25~85°C |
| MT6622P/B-L | 3.047x2.552x0.55mm WLCSP with crystal mode | -25~85°C |
| MT6622BP/B-L | 3.047x2.552x0.55mm WLCSP with co-clock mode | -25~85°C |

*Table 3 MT6622 ordering information*

# 3 Electrical characteristics

## 3.1 Absolute maximum ratings

| Parameter | Description | Min | Max | Unit |
|-----------|-------------|-----|-----|------|
| VBATT | Battery regulator supply voltage | -0.3 | 4.73 | V |
| VDDP | I/O supply voltage | -0.3 | 3.63 | V |
| VDIG | Digital regulator supply voltage | -0.3 | 3.63 | V |
| VCC | Analog supply voltage | -0.3 | 3.63 | V |
| VDD | Regulated digital circuit supply voltage | -0.3 | 1.32 | V |
| TST | Storage temperature | -55 | +125 | °C |
| RFMAX | Maximum RF input level | - | +5 | dBm |

*Table 4 Absolution maximum ratings*

## 3.2 Recommended operating range

| Parameter | Description | Min | Max | Unit |
|-----------|-------------|-----|-----|------|
| VBATT | Battery regulator supply voltage | 3.2 | 4.3 | V |
| VDDP | I/O supply voltage | 1.62 | 3.08 | V |
| VDIG | Digital regulator supply voltage | 2.52 | 3.08 | V |
| VCC | Analog supply voltage | 2.52 | 3.08 | V |
| VDD | Regulated digital circuit supply voltage | 1.08 | 1.32 | V |
| TOP | Operating temperature | -25 | +85 | °C |

*Table 5 Recommended operating range*

## 3.3 DC characteristics of digital IO

| Parameter | Description | Min | Max | Unit |
|-----------|-------------|-----|-----|------|
| $V_{IL}$ (VDD28 = 2.8v) | Input logic low voltage | -0.3 | 0.25*VDD28 | V |
| $V_{IH}$ (VDD28 = 2.8v) | Input logic high voltage | 0.75*VDD28 | VDD28+0.3 | V |
| $V_{OL}$ (VDD28 = 2.8v) | Output logic low voltage | | 0.15*VDD28 | V |
| $V_{IH}$ (VDD28 = 2.8v) | Output logic high voltage | 0.85*VDD28 | | V |
| $V_{IL}$ (VDD28 = 1.8v) | Input logic low voltage | -0.3 | 0.25*VDD28 | V |
| $V_{IH}$ (VDD28 = 1.8v) | Input logic high voltage | 0.75*VDD28 | VDD28+0.3 | V |
| $V_{OL}$ (VDD28 = 1.8v) | Output logic low voltage | | 0.15*VDD28 | V |
| $V_{IH}$ (VDD28 = 1.8v) | Output logic high voltage | 0.85*VDD28 | | V |

*Table 6 DC characteristics of digital IO*

## 3.4    Typical current consumption

| Operating mode | Current consumption | Unit |
|---|---|---|
| Deep sleep mode | 50 | µA |
| Bluetooth continuous transmit (TX output power: 10dBm) | 49 | mA |
| Bluetooth continuous receive (TX power: -90dBm) | 34 | mA |
| Bluetooth SCO connection, HV3 packets | - | mA |
| Bluetooth sniff mode + page scan<br>(Page scan interval = 1.28 sec, sniff interval = 500ms.) | - | mA |
| Bluetooth page scan + inquiry scan<br>(Page scan interval = 1.28s, inquiry scan interval = 2.56s) | 0.5 | mA |
| Bluetooth page scan<br>(Page scan interval = 1.28s) | 0.34 | mA |

*Table 7 Current consumption specifications*

## 3.5    Regulator specifications

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input voltage | 3.2 | - | 4.3 | V |
| Output voltage | 2.52 | 2.8 | 3.08 | V |
| Maximum load current | - | - | 100 | mA |
| Quiescent current | - | 30 | - | µA |
| Load capacitance (VCC28_BT) | 1 | - | 10 | µF |
| Load capacitor ESR | - | - | 500 | mΩ |
| Line regulation | - | 1.5 | - | mV/V |
| Load regulation (Iload < 70mA) | - | - | 50 | mV |
| PSRR@1KHz | - | -60 | - | dB |
| Turn on time (Cload = 2uF) | - | - | 400 | µs |

*Table 8 Battery linear regulator electrical specifications*

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input voltage | 2.52 | 2.8 | 3.08 | V |
| Output voltage | 1.08 | 1.2 | 1.32 | V |
| Maximum load current | - | - | 40 | mA |
| Quiescent current | - | 25 | - | µA |
| Quiescent current (sleep mode) | - | 9 | - | µA |
| Load capacitance | - | 1 | - | µF |

| Load capacitor ESR | - | - | 500 | mΩ |
|---|---|---|---|---|
| Line regulation | - | 1.5 | - | mV/V |
| Load regulation (Iload < 40mA) | - | 55mV | - | mV |
| Turn on time | - | - | 400 | µs |

*Table 9 Digital linear regulator electrical specifications*

# 4    Functional description

## 4.1    Power subsystem

MT6622 contains several LV (low voltage, 2.8V to 1.5V) linear regulators to provide power supply for every power domain, including RF circuitry and digital core circuitry. Furthermore, it has built-in BAT linear regulator which allows the chip to connect directly to Li-Ion battery power supply. The supported battery voltage ranges from 3.2V to 4.3V.

The input pin LDO28EN is used by the host controller to turn on and off the BAT regulator. The host can control this pin to enable the whole MT6622 system. The enable voltage ($V_{IH}$) of pin LDO28EN is 1.5V. Please be sure that the control signal meets this requirement in order for the system to operate correctly.

The built-in LV linear regulators for RF circuitry are cap-less regulators. It provides high PSRR for achieving excellent RF performance. The power controls for these RF LDOs are maintained internally by digital controller for optimized power consumption.

The DIG (digital) LV regulator requires an external capacitor. When the 1.2V power is supplied from the regulator on VDD12 pins, an internal POR (Power-On Reset) will be generated to start the system. An external system reset to start the system is optional according to the application requirement.
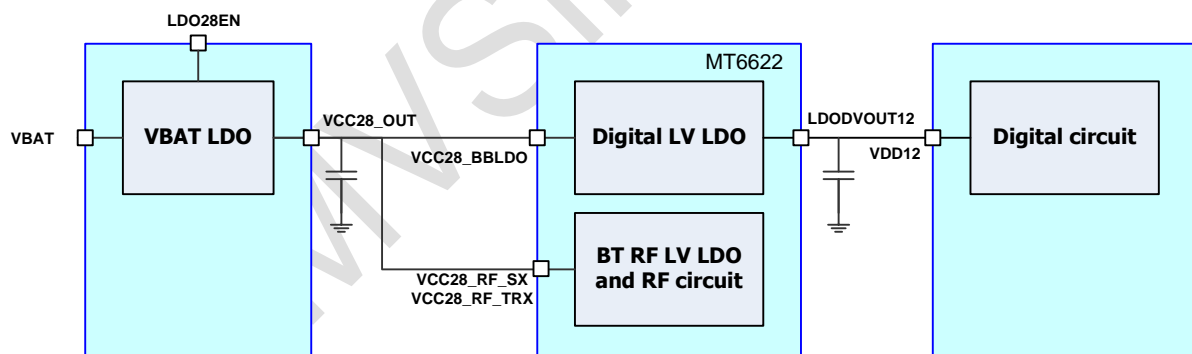
The power subsystem is illustrated in Figure 10.



*Figure 10 Power subsystem diagram*

## 4.2    Clock generation

There are two clock domains inside MT6622. One is the SYSTEM reference clock which is used for the Bluetooth and MCU system operations. The second is the LPO clock, which is a low-power 32.768KHz reference clock used to maintain Bluetooth link during sleep mode operations.

MT6622 has two options for the SYSTEM clock source input. It can either be a one-pin crystal input, or it can come from external clock source.

MT6622 supports most widely used clock frequencies in the mobile handset platform. They include 13, 16, 19.2, 26, and 32MHz.

To save system BOM cost, the SYSTEM clock can be shared with the clocks available on the mobile handset platform. For example, the reference clock used for mobile base-band chipset can also be used as the MT6622 source clock. In this configuration, an output pin SRCLKENA from MT6622 is used as the enable signal for the external clock source. The generation of the signal is coupled to the internal sleep mode control function.

The input frequencies can be selected by GPIO trapping or detected automatically based on the availability of externally supplied 32.768KHz clock.

The LPO clock can come from the host chip in both QFN40 and WLCSP package.

## 4.3 Chip operating mode and power management

MT6622 is optimized for low power operation of Bluetooth. With sophisticated built-in state control and advanced power management, the operating mode can be changed seamlessly while achieving minimum power consumption.

MT6622's operating modes can be categorized into 4 major modes:

- Chip power off mode

- Power-on Init mode

- Bluetooth standalone operation mode

- System deep sleep mode

For each of these major operating modes, the individual subsystems may be under different power states as the table below shows:

| Operating Modes | Platform Subsystem State | Bluetooth Subsystem State |
|---|---|---|
| Chip Power Off | Power off | Power off |
| Power-on Init | Active | Power-down |
| System Deep Sleep | Sleep | Power-down |
| BT Standalone | Active/Idle | Active |
| | Sleep | Sleep |

*Table 10 Operating Modes*

The power states for each subsystem are further described below:

Chip-level Power States

**Power-off mode**: Power supply is not enabled or LDO28EN is low. The entire chip is powered off.

**Power-on Init mode**: When MT6622 is powered on, it first enters the init mode. In this mode, an internal digital PLL is turned on to supply the clock for baseband circuit.

**Deep Sleep mode**: No link needs to be maintained, the baseband controller can enter sleep mode in order to turn off most of the Bluetooth related circuit in MT6622. In deep sleep mode, the system could be awakened by a external wake up signal from the host controller. During always sleep mode, only the LPO clock reference is active and the Bluetooth baseband controller doesn't maintain any link at all.

Platform Subsystem Power States

**Platform Active mode**: It is defined as the state where the platform system is in operation.

**Platform Idle mode**: When firmware no longer has tasks pending to be completed, then the MCU and the relevant buses can be put under power down mode to save current consumption. Under this mode, the platform peripheral system are still in operation and can therefore still receive traffic from the host.

Bluetooth Subsystem Power States

**BT Power-down mode**: It is defined as the state where BT related RF circuitries and LDO are turned off, and Bluetooth digital circuitries have no clock supply.

**BT Active mode**: It is defined as the state that RF circuit is enabled to transmit or receive data. Since Bluetooth is a TDD (Time-Division Duplex) system, only TX or RX circuit will be turned on at the same time.

**BT Idle mode**: When the firmware finishes its task and starts to wait for next hardware trigger, it forces the hardware to enter this mode. In this mode. Part of the logic, like MCU, will enter a low power mode. RF circuit might still be operating in the mode.

**BT Sleep mode**: For some Bluetooth scenarios, where all links are in low power mode, the baseband controller can enter sleep mode in order to turn off most of the Bluetooth related circuit in MT6622. In sleep mode, the system could be awakened after sleep time expired or by a external wake up signal from the host controller. During sleep mode, only the LPO clock reference is active and the Bluetooth baseband controller maintains the correct link timing based on this reference signal.

| | Chip power off | Chip power on Init | Deep Sleep | Platform Active | Platform Idle | BT Power down | BT Active | BT Sleep |
|---|---|---|---|---|---|---|---|---|
| VBAT linear regulator | OFF | ON | ON | ON | ON | ON | ON | ON |
| Digital LV linear regulator | OFF | ON | ON | ON | ON | ON | ON | ON |

| Bluetooth Digital circuitry | OFF | System clock domain is ON. LPO clock domain is OFF. | Bluetooth Baseband is powered-down with clock supply turned off | | | Bluetooth Baseband clock is turned off | System clock domain is ON. LPO clock domain is OFF. Bluetooth low power controller is active with LPO clock. | System clock domain is ON. Part of System clock based circuitry might be turned off by the firmware. LPO clock domain is ON. |
|---|---|---|---|---|---|---|---|---|
| Bluetooth RF LV linear regulator and BT RF circuitry | OFF | Crystal oscillator is ON. Other RF circuitry is OFF. | OFF | Crystal oscillator and PLL are ON. Other RF circuitry is OFF. | Crystal oscillator and PLL are ON. Other RF circuitry is OFF. | Crystal oscillator and PLL are ON. Other RF circuitry is OFF. | Crystal oscillator and PLL are ON. The other RF circuitry might be in RX or TX modes. | Crystal oscillator and PLL are ON. The other RF circuitry might be in RX or TX modes. |

*Table 11 Power state description for power management*

## 4.4    MCU subsystem

The MCU (Micro-Controller Unit) subsystem contains the 32-bit RISC microprocessor, internal memory and the ROM patch function. It also contains the UART interface controller and the power/clock management function.

## 4.5    Bluetooth subsystem

The Bluetooth subsystem contains the Bluetooth baseband subsystem and the Bluetooth RF subsystem.

The Bluetooth baseband subsystem contains a baseband processor which supports timing control, bit-stream processing, encryption, frequency hopping, and modulation/demodulation. It also contains the audio codec, Wi-Fi coexistence interface controller, and a sleep mode controller.

The Bluetooth RF subsystem contains a fully integrated transceiver.

For TX path, the baseband transmit data is digitally modulated in the baseband processor, then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter, and the power amplifier. The power amplifier is capable of transmitting 10dBm power for class-1.5 operation.

For RX path, MT6622 is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which could support different clock frequencies as the reference clock

as described in section 4.2. The mixer output is then converted to digital signal, down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.

MT6622 features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

# 5 Interface Descriptions

## 5.1 UART Interface

MT6622 utilizes the Universal Asynchronous Receiver Transmitter (UART) interface as its host control interface. This UART interface supports flexible configurations, as listed in the table below.

| Interface Configuration Parameters | Supported values |
|---|---|
| Data length | 8 bits |
| Flow control | Hardware RTS/CTS<br>Software RTS/CTS<br>NONE |
| Parity | Even/Odd/None<br>(Note: parity is only supported when Software flow control is disabled) |
| Stop bit length | 1 or 2 |

*Table 12 UART Interface Configurations*

The electrical timing characteristic for the UART interface is illustrated below.
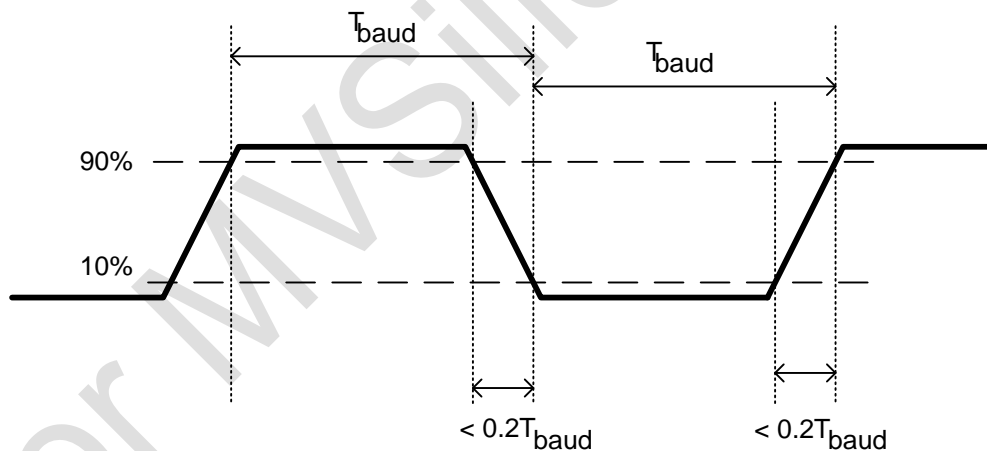


*Figure 11 Electrical Timing Characteristics*

In addition to the standard baud rates, high speed baud rates are also supported in order to meet the higher bandwidth requirements for EDR data transfers.  The default supported baud rates by MT6622 are listed in the table below.

| Baud Rate (bps) | Error |
|---|---|
| 110 | 0.00% |
| 300 | 0.00% |

| 1200 | 0.00% |
|------|-------|
| 2400 | 0.00% |
| 4800 | 0.00% |
| 9600 | 0.01% |
| 19200 | -0.02% |
| 38400 | 0.04% |
| 57600 | -0.08% |
| 115200 | -0.08% |
| 230400 | -0.08% |
| 460800 | 0.64% |
| 921600 | -0.79% |
| 3200000 | 0.00% |

*Table 13 Default UART Baud Rate Support*

Other baud rates that are not shown in the default baud rate table above may also be supported through UART register configuration. However, system designers must take care in making sure that the total baud rate frequency mismatch between the 2 sides, along with the electrical signal timings, can still meet the 2% error margin required in order to sustain the rate of operation.

## 5.2  PCM Interface

### 5.2.1  Data format

MT6622 incorporates the Pulse Coded Modulation (PCM) interface, which can be used for Bluetooth voice data transfers between the MT6622 system and the host system. Using this interface, the voice signals can be transferred between the 2 devices continuously without mcu intervention for maximum power savings.

The MT6622 PCM interface supports most commonly used interface formats through user configuration. The supported formats are listed below.

| Interface Configuration Parameters | Supported values |
|------------------------------------|------------------|
| Line Interface Format | Linear/A-law/U-law |
| Data length | Linear: 13/14/15/16 bits<br>A-law/U-law: 8 bits |
| Voice Sampling Rate | 8KHz samples |
| PCM Clock/Sync Source | PCM Master Mode: clock and sync are internally generated<br>PCM Slave Mode: clock and sync are from external |
| PCM Sync Rate | 8KHz |
| PCM Clock Rate | PCM Master Mode:<br>64KHz/128KHz/256KHz/512KHz/1024KHz /2048KHz (A-law/U-law) |

| | 128KHz/256KHz/512KHz/1024KHz/2048KHz (Linear)<br>PCM Slave Mode:<br>64KHz ~ 2400KHz (A-law/U-aw)<br>128KHz ~ 2400KHz (Linear) |
|---|---|
| PCM Sync Format | Short sync or long sync |
| Data Ordering | MSB or LSB first (see configuration matrix for limitation) |
| Zero Padding | Yes (see configuration matrix for limitation) |
| Sign extension | Yes (see configuration matrix for limitation) |

*Table 14 PCM Interface Configurations*

Based on the wide range of interface options, the supported configuration matrix is summarized as follows.

(Note that sign extension and zero padding are only relevant when the linear input bits are less than 16bits.)

| Configurations | Sign Extension | Zero Padding | MSB First | LSB First | PCM Long Sync | PCM Short Sync |
|---|---|---|---|---|---|---|
| 1 | | ● | ● | | ● | |
| 2 | | ● | ● | | | ● |
| 3 | | ● | | ● | ● | |
| 4 | | ● | | ● | | ● |
| 5 | ● | | ● | | ● | |
| 6 | ● | | ● | | | ● |

*Table 15 PCM Configuration Matrix Summary*

For best quality, the recommended settings are:

**16b linear CVSD + MSB First + short sync + 256 KHz PCM clock**

The illustrations below give 2 common interface timing configuration examples.

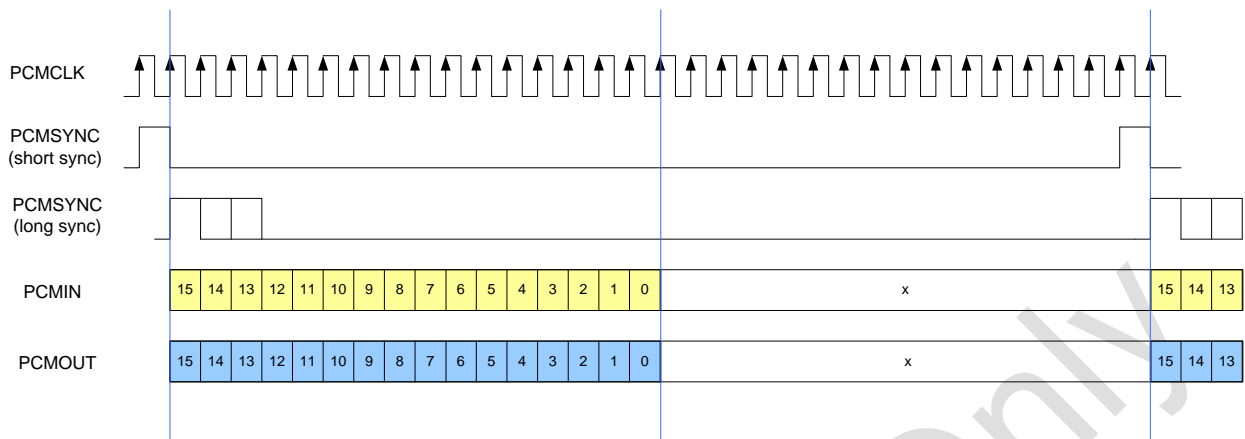Example: 16b linear PCM, 256KHz PCM clock, 8k sync

*Figure 12 PCM format: 16b Example*

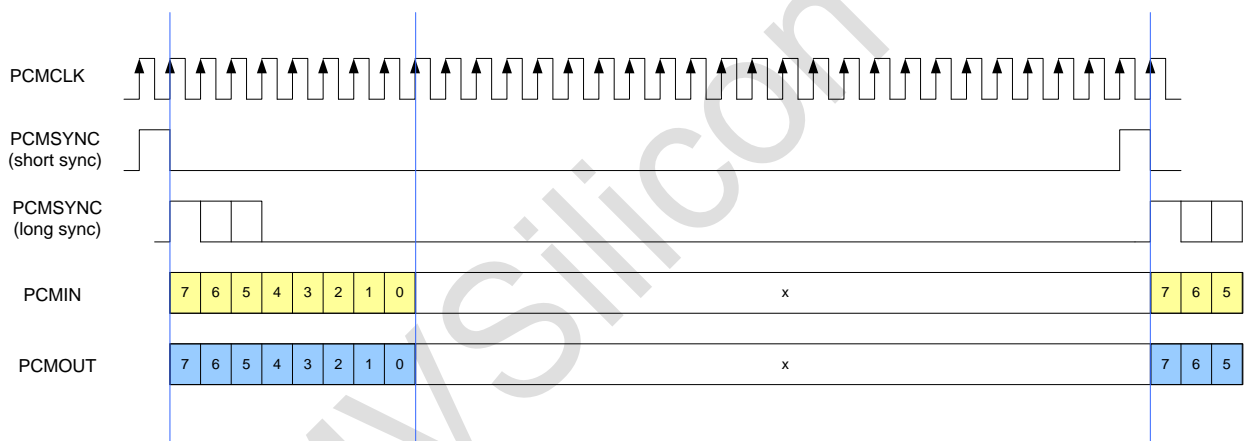Example: 8b a-law/u-law, 256KHz PCM clock, 8k sync



*Figure 13 PCM format: 8b Example*

## 5.2.2    Detailed Interface Descriptions

### 5.2.2.1    PCM Master/Slave Mode

When acting as a PCM Slave, both PCM and PCM clock signals are generated by the external PCM master. When acting as a PCM Master, both PCM sync and PCM clock are generated by MT6622.
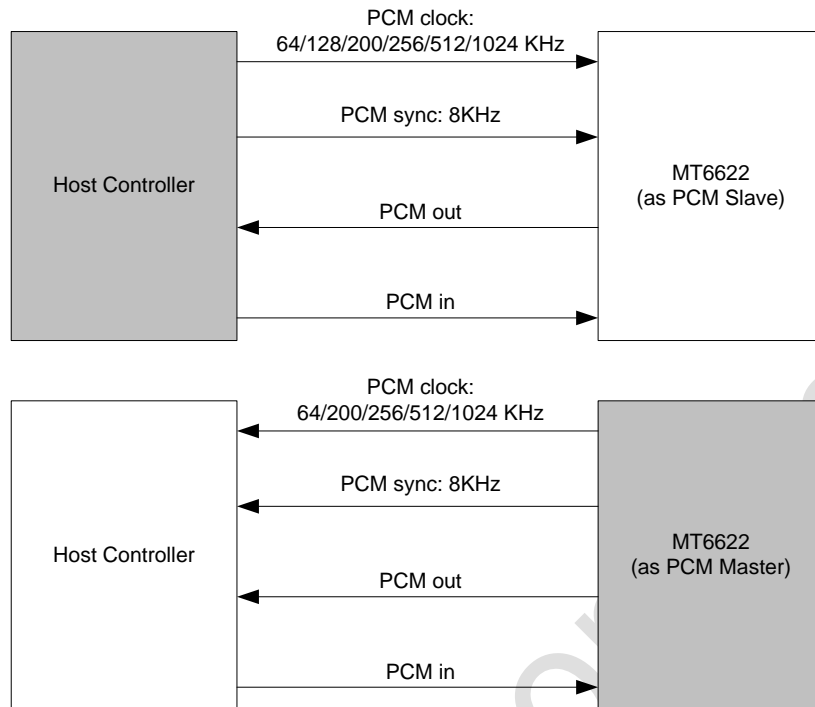
*Figure 14 PCM Master/Slave Modes*

## 5.2.2.2    Sign Extension

Sign extension is only meaningful when the linear PCM length is less than 16bits, and it only applies to MSB first data formats.
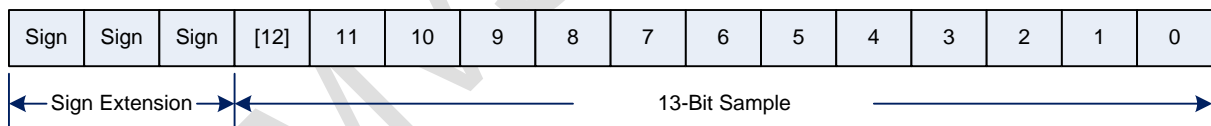
| Sign | Sign | Sign | [12] | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|----|----|---|---|---|---|---|---|---|---|---|---|

←—— Sign Extension ——→ ←——————————————— 13-Bit Sample ———————————————→

*Figure 15 PCM format: Sign Extension*

## 5.2.2.3    Zero Padding

Zero padding is only meaningful when the linear PCM length is less than 16bits, and it only applies to LSB first data formats.

| [12] | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 1'b0 | 1'b0 | 1'b0 |
|------|----|----|---|---|---|---|---|---|---|---|---|---|------|------|------|

←——————————————— 13-Bit Sample ———————————————→ ←— Zero padding —→
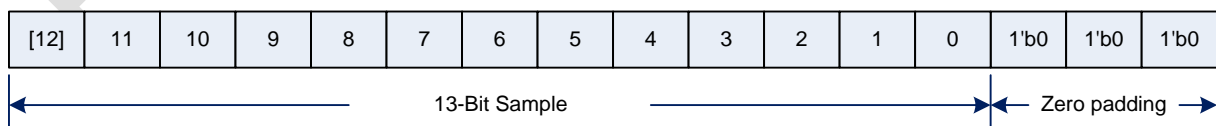
*Figure 16 PCM format: Zero Padding*
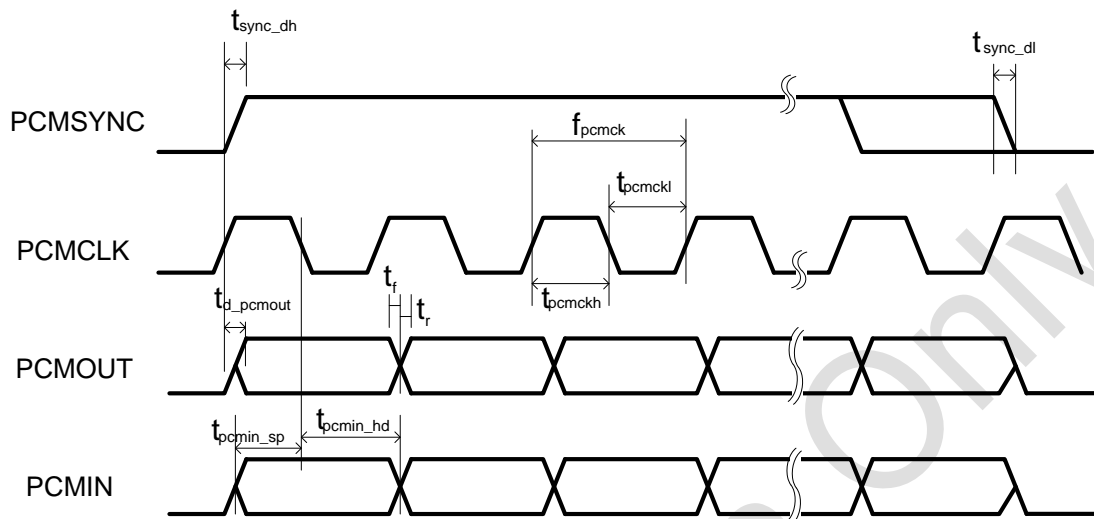
### 5.2.3    PCM timing information



*Figure 17 PCM timing: master mode with long sync*
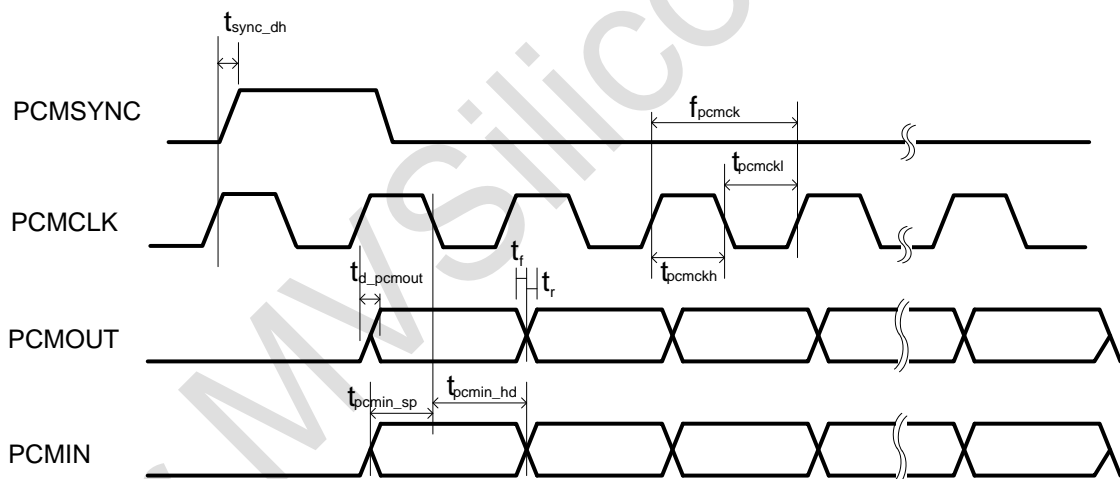


*Figure 18 PCM timing: master mode with short sync*

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| fpcmck | PCM clock frequency | | -[1] | | KHz |
| tpcmckh | PCM clock high duration | - | 500/ fpcmck | - | ns |
| tpcmckl | PCM clock low duration | - | 500/ fpcmck | - | ns |
| tsync_dh | Delay time from PCM_CLK high to PCM_SYNC high | 50 | - | 150 | ns |
| tsync_dl | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | 50 | - | 150 | ns |

| td_pcmout | PCM_OUT delay time from PCM_CLK low | - | - | 20 | ns |
|-----------|-------------------------------------|---|---|----|-----|
| tf | PCM _OUT falling time from high to low | - | - | 5 | ns |
| tr | PCM _OUT rising time from low to high | - | - | 5 | ns |
| tpcmin_sp | Setup time for PCM_IN valid to PCM_CLK low | 50 | - | - | ns |
| tpcmin_hp | Hold time for PCM_CLK low to PCM_IN invalid | 50 | - | - | ns |

*Note 1: Refer to Table 14 for a detail list of clock rate.*

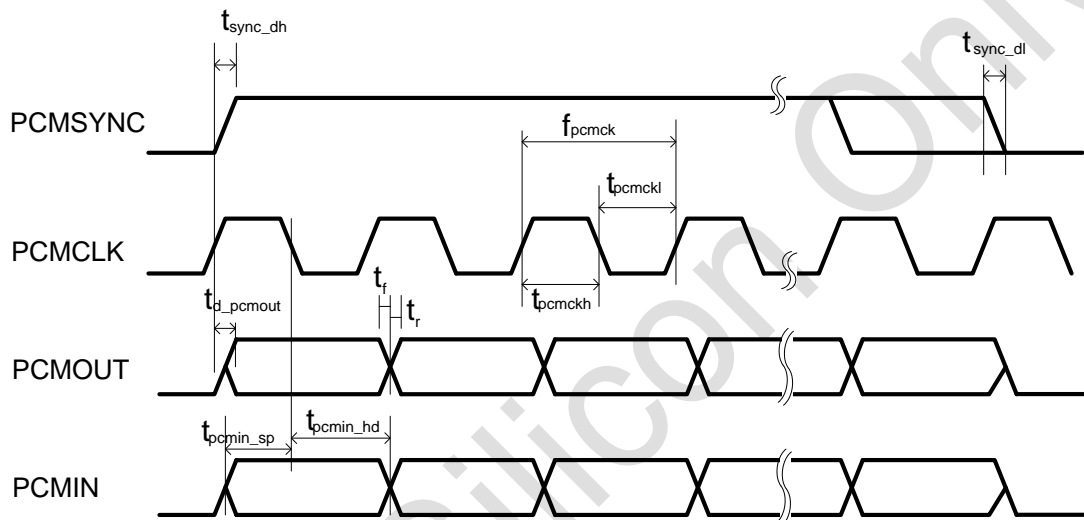**Table 16 PCM timing: master mode**



**Figure 19 PCM timing: slave mode with long sync**
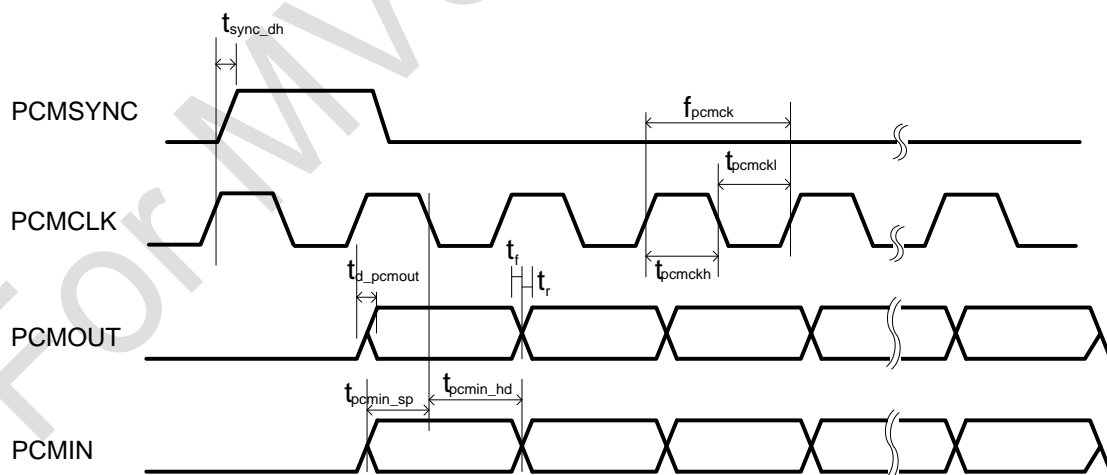


**Figure 20 PCM timing: slave mode with short sync**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| fpcmck | PCM clock frequency (slave: input) | 64 | - | 2400 | kHz |

| tpcmckh | PCM clock high duration | 200 | - | - | us |
|---------|--------------------------|-----|---|-----|-----|
| tpcmckl | PCM clock low duration | 200 | - | - | us |
| tsync_dh | Delay time from PCM_CLK high to PCM_SYNC high | 0 | - | - | ns |
| tsync_dl | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | - | - | 50 | ns |
| td_pcmout | PCM_OUT delay time from PCM_CLK low | 50 | - | 150 | ns |
| tf | PCM _OUT falling time from high to low with 10pf output load. | - | - | 5 | ns |
| tr | PCM _OUT rising time from low to high with 10pf output load. | - | - | 5 | ns |
| tpcmin_sp | Setup time for PCM_IN valid to PCM_CLK low | 50 | - | - | ns |
| tpcmin_hp | Hold time for PCM_CLK low to PCM_IN invalid | 50 | - | - | ns |

*Table 17 PCM timing: slave mode*

## 5.3    Wireless LAN Co-existence Interface

MT6622 supports the Packet Traffic Arbitration (PTA) interface that allows the Bluetooth system to coexist with another Wireless LAN system on the same PCB. This interface is defined by IEEE 802.15.2 as one of the methods for Wireless LAN co-existence. With the PTA features enabled, arbitration is performed in order to prevent collision of the Bluetooth and WLAN signals. The diagram below illustrates this interface connection.
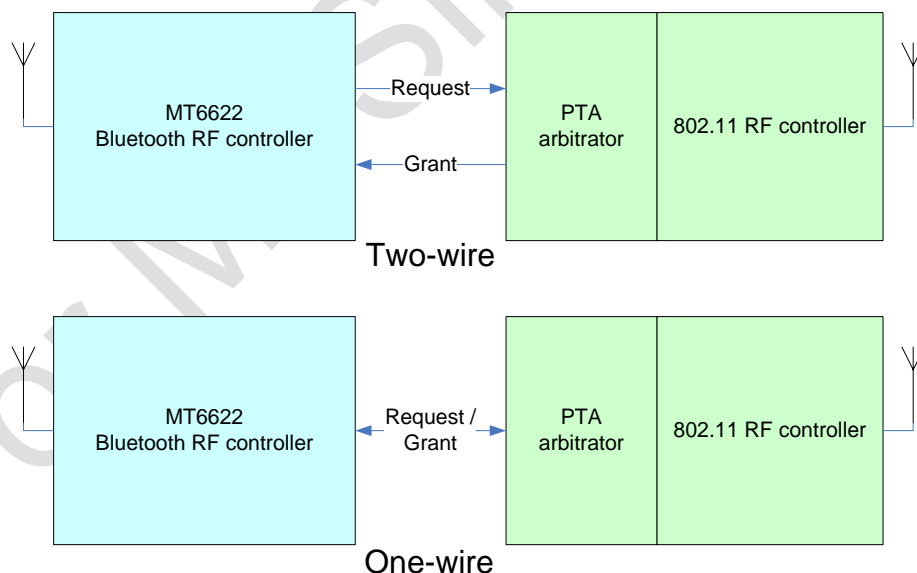


*Figure 21 PTA Interface*

The interface signal in the diagram above maps to the pad names as follows:

| Signal | GPIO | Direction | Description |
|--------|------|-----------|-------------|
|        |      |           |             |

| BT2WIFI | GPIO4 | Two wire: Output<br>One wire: Inout | Request from Bluetooth to other 2.4GHz radio |
|---------|-------|--------------------------------------|-----------------------------------------------|
| WIFI2BT | GPIO5 | Input | Grant from other 2.4GHz radio to Bluetooth |

*Table 18 PTA Interface Pad Name*

For the widest range of compatibility, MT6622's PTA interface supports 5 types of operating modes. Mode 1/2/3/4 selections are governed by the request pin configuration behavior. In addition, a proprietary 1-wire interface mode is also supported for minimum pin requirement.

## 5.4    Specification of External Reference Clock

If MT6622 clock input path is from external clock, the specification of external reference clock should be as below.

| Chip part number | MT6612 | MT6616 | MT6622 | MT6626 |
|------------------|--------|--------|--------|--------|
| Loading (on) | 75k//9.8pF | 75k//9.8pF | 75k//3.5pF | 75k//3.5pF |
| Loading (off) | 75k//8.1pF | 75k//8.1pF | 75k//3.5pF | 75k//3.5pF |
| Swing | 1.5V~300mV | 1.5V~300mV | 1.5V~300mV | 1.5V~300mV |
| Waveform | Analog Signal/Square Wave | Analog Signal/Square Wave | Analog Signal/Square Wave | Analog Signal/Square Wave |
| PN requirement 1Hz | -- | -- | -- | -- |
| PN requirement 10Hz | -- | -- | -- | -- |
| PN requirement 100Hz | -- | -- | -- | -- |
| PN requirement 1kHz | -128dBc/Hz | -128dBc/Hz | -128dBc/Hz | -128dBc/Hz |
| PN requirement 10kHz | -140dBc/Hz | -140dBc/Hz | -140dBc/Hz | -140dBc/Hz |
| PN requirement 100kHz | -147dBc/Hz | -147dBc/Hz | -147dBc/Hz | -147dBc/Hz |
| Internal AC couple?<br> (to check if external cap needed) | No<br>(need ext AC couple cap) | No | No | No |

*Table 19 Specification of External Reference Clock*

## 5.5　LDO28EN/SYSRST__B/SRCLKENA Timing Information
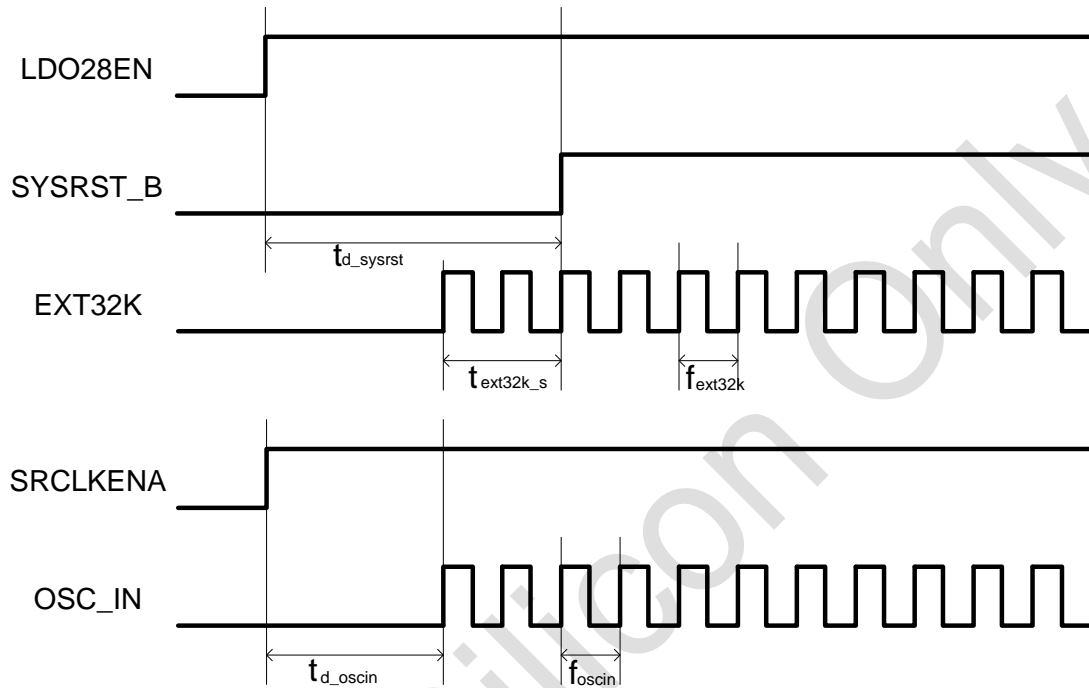


*Figure 22 LDO28EN/SYSRST_B/SRCLKENA timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| fext32k | EXT32K frequency | 31 | 32.768 | 34 | KHz |
| td_sysrst | Delay time form LDO28EN high to SYSRST_B high | 10 | - | - | ms |
| text32k_s | Setup time for EXT32K | 1 | - | - | ms |
| foscin | OSC_IN frequency |  | *1 |  | MHz |
| td_oscin | OSC_IN delay time from SRCLKENA high | *2 |  |  | ms |

*Table 20 Specification of LDO28EN/SYSRST_B/SRCLKENA signals*

*1 : Typical frequency can be 13, 16, 19.2, 26 or 32MHz. Please refer to section 4.2 clock generation.

*2 : This value depends on the clock stable time of OSC_IN. For example, MT6252 OSC clock stable time is 2ms. AD6548 OSC clock stable is 5ms.

# 6 Bluetooth radio characteristics

Tests are performed under the normal conditions defined in Bluetooth test specification with external band pass filter. Typical specifications are with default register settings and under recommended operating conditions. Min/Max specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

## 6.1 Basic rate

### 6.1.1 Receiver specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency range | | 2402 | - | 2480 | MHz |
| Receiver sensitivity[1] | BER<0.1% | - | -95 | - | dBm |
| Maximum usable signal | BER<0.1% | - | 0 | - | dBm |
| C/I co-channel (BER<0.1%) | Co channel selectivity | - | 6 | 11 | dB |
| C/I 1MHz (BER<0.1%) | Adjacent channel selectivity | - | -9 | 0 | dB |
| C/I 2MHz (BER<0.1%) | 2nd adjacent channel selectivity | - | -40 | -30 | dB |
| C/I≥3MHz (BER<0.1%) | 3rd adjacent channel selectivity | - | -45 | -40 | dB |
| C/I Image channel (BER<0.1%) | Image channel selectivity | - | -20 | -9 | dB |
| C/I Image 1MHz (BER<0.1%) | 1MHz adjacent to image channel selectivity | - | -43 | -20 | dB |
| Out-of-band blocking | 30MHz to 2000MHz | -10 | -3 | | dBm |
| | 2000MHz to 2399MHz | -27 | -9 | - | dBm |
| | 2498MHz to 3000MHz | -27 | -8 | - | dBm |
| | 3000MHz to 12.75GHz | -10 | -1 | - | dBm |
| Intermodulation | Max interference level to maintain 0.1% BER, interference signals at 3MHz and 6MHz offset. | -39 | -33 | - | dBm |

*Note 1: The receiver sensitivity is measured on the chip input interface.*

*Table 21 Basic rate receiver specifications*

### 6.1.2 Transmitter specifications

| Parameter | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Frequency range | | 2402 | - | 2480 | MHz |

| Output power[1] | At maximum power output level | 6 | 10 | 12 | dBm |
|---|---|---|---|---|---|
| Gain step | | 2 | 4 | 8 | dB |
| Modulation characteristics | Δf1avg | 140 | 157 | 175 | KHz |
| | Δf2max (For at least 99.9% of all Δf2max) | 115 | 130 | - | KHz |
| | Δf1avg /Δf2avg | 0.8 | 0.98 | - | KHz |
| ICFT | Initial carrier frequency tolerance | -75 | +5 | +75 | KHz |
| Carrier frequency drift | One slot packet (DH1) | -25 | +13 | +25 | KHz |
| | Two slot packet (DH3) | -40 | +15 | +40 | KHz |
| | Five slot packet (DH5) | -40 | +15 | +40 | KHz |
| | Max drift rate | - | 7 | 20 | KHz/50µs |
| TX output spectrum | 20dB bandwidth | - | 920 | 1000 | KHz |
| In-Band spurious emission | ±2MHz offset | - | -40 | -20 | dBm |
| | ±3MHz offset | - | -48 | -40 | dBm |
| | >±3MHz offset | - | -48 | -40 | dBm |
| Output-of-Band spurious emission | 30MHz to 1GHz, operating mode | - | -76 | - | dBm |
| | 1GHz to 12.75GHz, operating mode | - | -52 | - | dBm |
| | 1.8GHz to 1.9GHz | - | -80 | - | dBm |
| | 5.15GHz to 5.3GHz | - | -78 | - | dBm |

*Note 1: The output power is measured on the chip output interface.*

*Table 22 Basic rate transmitter specifications*

## 6.2     Enhanced data rate

### 6.2.1     Receiver specifications

| Parameter | Modulation | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Receiver sensitivity (BER<0.01%)[1] | π/4 DQPSK | - | -96 | - | dBm |
| | 8PSK | - | -89 | - | dBm |
| Maximum usable signal (BER<0.1%) | π/4 DQPSK | - | 0 | - | dBm |
| | 8PSK | - | 0 | - | dBm |
| C/I co-channel (BER<0.1%) | π/4 DQPSK | - | 9 | 13 | dB |
| | 8PSK | - | 16 | 21 | dB |
| C/I 1MHz (BER<0.1%) | π/4 DQPSK | - | -12 | 0 | dB |
| | 8PSK | - | -5 | 5 | dB |
| C/I 2MHz (BER<0.1%) | π/4 DQPSK | - | -48 | -30 | dB |
| | 8PSK | - | -42 | -33 | dB |
| C/I≥3MHz (BER<0.1%) | π/4 DQPSK | - | -51 | -40 | dB |

| | 8PSK | - | -44 | -33 | dB |
|---|---|---|---|---|---|
| C/I Image channel (BER<0.1%) | π/4 DQPSK | - | -24 | -7 | dB |
| | 8PSK | - | -18 | 0 | dB |
| C/I Image 1MHz (BER<0.1%) | π/4 DQPSK | - | -51 | -20 | dB |
| | 8PSK | - | -44 | -13 | dB |

*Note 1: The receiver sensitivity is measured on the chip input interface.*

*Table 23 Enhanced data rate receiver specifications*

## 6.2.2 Transmitter specifications

| Parameter | Description and modulation | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency range | | | 2402 | - | 2480 | MHz |
| Maximum transmit power[1] | π/4 DQPSK | | 4 | 7.5 | 9 | dBm |
| | 8PSK | | 4 | 7.5 | 9 | dBm |
| Relative transmit power | π/4 DQPSK | | - | -1.7 | - | dB |
| | 8PSK | | - | -1.7 | - | dB |
| Frequency stability | maximum carrier frequency stability, $\omega_o$ | π/4 DQPSK | -10 | 4 | 10 | KHz |
| | | 8PSK | -10 | 4 | 10 | KHz |
| | maximum carrier frequency stability, $\omega_i$ | π/4 DQPSK | -75 | 10 | 75 | KHz |
| | | 8PSK | -75 | 10 | 75 | KHz |
| | maximum carrier frequency stability, $|\omega_o + \omega_i|$ | π/4 DQPSK | -75 | 10 | 75 | KHz |
| | | 8PSK | -75 | 10 | 75 | KHz |
| Modulation accuracy | RMS DEVM | π/4 DQPSK | - | 5 | 30 | % |
| | | 8PSK | - | 5 | 20 | % |
| | 99% DEVM | π/4 DQPSK | - | 9 | - | % |
| | | 8PSK | - | 9 | - | % |
| | Peak DEVM | π/4 DQPSK | - | 15 | 35 | % |
| | | 8PSK | - | 15 | 25 | % |
| In-Band spurious emission | ±1MHz offset | π/4 DQPSK | - | -33 | -26 | dB |
| | ±1MHz offset | 8PSK | - | -33 | -26 | dB |
| | ±2MHz offset | π/4 DQPSK | - | -30 | -20 | dBm |
| | ±2MHz offset | 8PSK | - | -30 | -20 | dBm |
| | ±3MHz offset | π/4 DQPSK | - | -42 | -40 | dBm |
| | ±3MHz offset | 8PSK | - | -42 | -40 | dBm |

*Note 1: The output power is measured on the chip output interface.*

*Table 24 Enhanced data rate transmitter specifications*

# 7    Terminology

| | |
|---|---|
| π/4 DQPSK | π/4 Differential Quadrature Phase Shift keying |
| 8PSK | 8 Phase Shift Keying |
| AFH | Adaptive Frequency Hopping |
| AGC | Automatic Gain Control |
| LDO | Low Drop-Out |
| LNA | Low Noise Amplifier |
| LO | Local Oscillator |
| LPO | Low Power Oscillator |
| LSB | Least Significant Bit |
| MCU | Micro-Controller Unit |
| MSB | Most Significant Bit |
| PCM | Pulse Code Modulation |
| PLL | Phase Locked Loop |
| PTA | Packet Traffic Arbitration |
| RAM | Random Access Memory |
| ROM | Read Only Memory |
| VCO | Voltage Control Oscillator |
| WLCSP | Wafer-Level Chip-Scale Packaging |