Technical Description

The Equipment Under Test (EUT) is a Bluetooth 3-Speed Stereo Turntable with Metal Tone Arm. It can accept input sources such as analog Aux-in (3.5mm phone jack), Phono (Long-Play Record) and wireless Bluetooth device. The Bluetooth module in the EUT is operating in the frequency range from 2402MHz to 2480MHz (79 channels with 1MHz channel spacing). The audio signal is amplified and fed to the built-in stereo loudspeakers. The EUT has an analog line-out (RCA) and headphone output (3.5mm phone jack). The EUT also equipped audio recording feature via USB port. The EUT is powered by 120VAC only.

2.4GHz Bluetooth Module:
Modulation Type: GFSK
Antenna Type: Integral, Internal (PCB Trace)
Frequency Range: 2402MHz - 2480MHz, 1MHz channel spacing, 79 channels

Nominal field strength is 90.8BµV/m @ 3m
Production Tolerance of field strength is +/- 3dB
Antenna gain is 0dBi

The functions of main ICs are mentioned below.

1. BlueTooth module BM84 (IC201):

1) U1 (IS1684S) acts as the 2.4GHz radio core of Bluetooth module IC201 (BM84), which is integrating with audio CODEC.
2) 16MHz crystal (X1) provides clock for Bluetooth RF IC IS1684S (U1).
3) U2 (24C32) is serial EEPROM for parameter backup of U1 (IS1684S).
4) IC202 (UTC4558) acts as analog audio output buffer amplifier.

2. USB Audio Recording Portion:

1) U500 (LW829A) acts as USB audio recorder.

3. Phono Small Signal Analog audio Portion:

1) IC502 (UTC4580) acts as RIAA equalizer of the stereo phono pick-up.

4. Audio Output portion:

1) IC504 (KA8227) is stereo power amplifier for loudspeakers and headphone.
2) IC503 (UTC4558) is Line-Out buffering amplifier.

Channel Frequency Table of Bluetooth Module

CH. NO.	FRE.	Hex Value		CH. NO.	FRE.	Hex Value		CH. NO	FRE.	Hex Value		CH. NO	FRE.	Hex Value
CH0	2402MHz	0		CH26	2428MHz	1A		CH52	2454MHz	34		CH78	2480MHz	4E
CH1	2403MHz	1		CH27	2429MHz	1B		CH53	2455MHz	35				
CH2	2404MHz	2		CH28	2430MHz	1C		CH54	2456MHz	36				
CH3	2405MHz	3		CH29	2431MHz	1D		CH55	2457MHz	37				
CH4	2406MHz	4		CH30	2432MHz	1E		CH56	2458MHz	38				
CH5	2407MHz	5		CH31	2433MHz	1F		CH57	2459MHz	39				
CH6	2408MHz	6		CH32	2434MHz	20		CH58	2460MHz	3A				
CH7	2409MHz	7		CH33	2435MHz	21		CH59	2461MHz	3B				
CH8	2410MHz	8		CH34	2436MHz	22		CH60	2462MHz	3C				
CH9	2411MHz	9		CH35	2437MHz	23		CH61	2463MHz	3D				
CH10	2412MHz	A		CH36	2438MHz	24		CH62	2464MHz	3E				
CH11	2413MHz	B		CH37	2439MHz	25		CH63	2465MHz	3F				
CH12	2414MHz	C		CH38	2440MHz	26		CH64	2466MHz	40				
CH13	2415MHz	D		CH39	2441MHz	27		CH65	2467MHz	41				
CH14	2416MHz	E		CH40	2442MHz	28		CH66	2468MHz	42				
CH15	2417MHz	F		CH41	2443MHz	29		CH67	2469MHz	43				
CH16	2418MHz	10		CH42	2444MHz	2A		CH68	2470MHz	44				
CH17	2419MHz	11		CH43	2445MHz	2B		CH69	2471MHz	45				
CH18	2420MHz	12		CH44	2446MHz	2C		CH70	2472MHz	46				
CH19	2421MHz	13		CH45	2447MHz	2D		CH71	2473MHz	47				
CH20	2422MHz	14		CH46	2448MHz	2E		CH72	2474MHz	48				
CH21	2423MHz	15		CH47	2449MHz	2F		CH73	2475MHz	49				
CH22	2424MHz	16		CH48	2450MHz	30		CH74	2476MHz	4A				
CH23	2425MHz	17		CH49	2451MHz	31		CH75	2477MHz	4B				
CH24	2426MHz	18		CH50	2452MHz	32		CH76	2478MHz	4C				
CH25	2427MHz	19		CH51	2453MHz	33		CH77	2479MHz	4D				

BM84

Bluetooth 3.0+EDR Wireless Speaker Module

Version:0.92
2012.08.15

Product Description

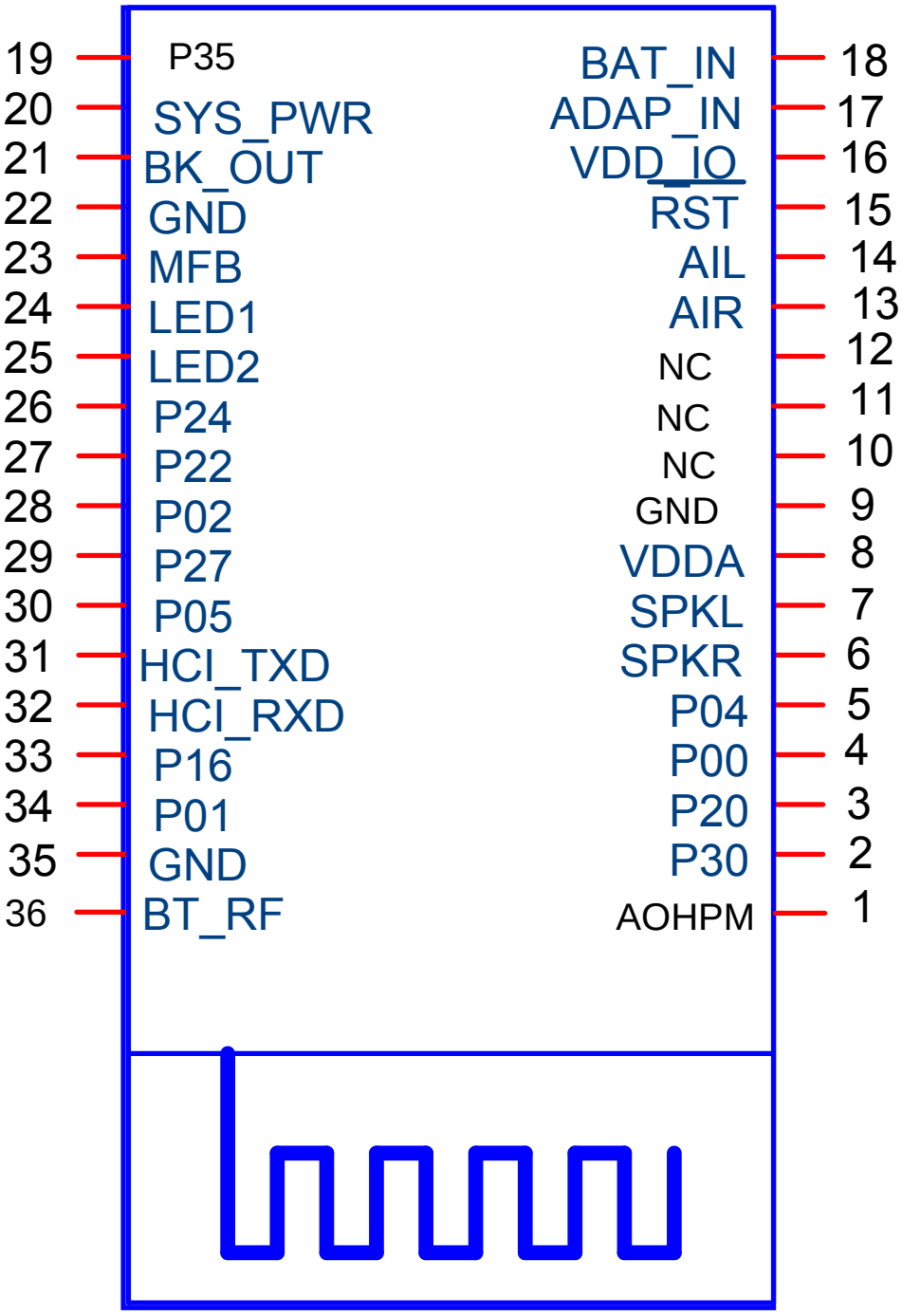
The ISSC BM84 is a highly integrated Bluetooth 3.0+EDR stereo module, designed for high data rate, short-range wireless communication in the 2.4 GHz ISM band. With ISSC Bluetooth stack and profile, the ISSC BM84 provides a low power and ultra-low cost Bluetooth 3.0+EDR solution for wireless voice/audio applications.

Features

- Main Chip: ISSC IS1684S
- Bluetooth 3.0+EDR compliant
- Typical +2dBm Class 2 output power
- Receiver Sensitivity: GFSK typical -91dBm, π/4 PSK typical -92dBm, 8DPSK typical -84dBm
- Piconet and Scatter net support
- HCI UART interface

- SBC decode for Bluetooth audio streaming
- Build-in High performance stereo audio codec
- Cap-less/single end headphone driver
- Audio DAC: 94dB SNR
- Build in Max. 350mAH Li-ion battery charger
- A2DP,AVRCP Profile support
- 3V operating voltage
- ROM version: 32Kb EEPROM
- 36 pins for SMT module(with additional 35th pin antenna port for external antenna option)
- Size: 15mm x29mm
- Build-in PCB Antenna
- RoHS compliant

Device Pinout Diagram



Pin Definition

Pin No.	I/O	Name	Description
1	AO	AOHPM	SPK-(Onle for Capless out put)
2	P	P30	GPIO, default pull-high input Line-in detection, 1: no line-in detected; 0: line-in detected
3	I/O	P20	GPIO, default pull-high input System Configuration, H: Application L: Baseband(IBDK Mode)
4	I/O	P00	GPIO, default pull-low input. Slide Switch Detector
5	I/O	P04	GPIO, default pull-high input Audio AMP Enable
6	AO	SPKR	R-channel analog headphone output, single-ended application only
7	AO	SPKL	L-channel analog headphone output, single-ended application only
8	AP	VDDA	Reserve for external cap to fine tune audio frequency response
9	AP	AGND	Audio ground
10		NC	
11		NC	
12		NC	
13	AI	AIR	Stereo analog line in, R-channel
14	AI	AIL	Stereo analog line in, L-channel
15	I/O	RST_N	System Reset Pin
16	P	VDDIO	VDDIO pin, for calibration only Do not add external power to this pin
17	P	adap_in	Power adaptor input
18	P	bat_in	battery input
19	I/O	P35	GPIO P35
20	P	SYS_PW	System power output
21	P	bk_out	buck feedback sense pin
22	P	GND	Ground

23	P	MFB	Multi-Function Push Button key Combined Play/Pause key when A2DP enabled.
24	P	LED1	LED Driver 1
25	P	LED2	LED Driver 2
26	I/O	P24	GPIO, default pull-high input System Configuration, H: Boot Mode
27	I/O	P22	GPIO, default pull-low input. External LDO enable
28	I/O	P02	GPIO, default pull-high input PLAY/PAUSE button
29	I/O	P27	GPIO, default pull-high input Foward button
30	I/O	P05	GPIO, default pull-high input REW button
31	O	HCI_TXD	HCI TX data
32	I	HCI_RXD	HCI RX DATA
33	I/O	P16	GPIO, default pull-high input Volumn down button
34	I/O	P01	GPIO, default pull-high input Volumn up button
35	P	GND	Ground
36	AIO	BT_RF	NC for on board PCB antenna Antenna matching if an external antenna is used

Bluetooth 3.0(EDR) Multimedia SOC

1. General Description

ISSC IS1684S is a compact, high integration, ultra-low cost, CMOS single-chip RF + baseband IC for Bluetooth v3.0(EDR) (Enhanced Data Rate) 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 1.1, 1.2, 2.0 or 2.1 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle 8051, TX/RX modem, memory controller, task/hopping controller, UART interface, and ISSC Bluetooth software stack to achieve the required Bluetooth v3.0(EDR) functions.

The IS1684S is designed to support high quality audio applications, an audio engine and a high performance stereo DAC are integrated for this purpose.

The audio engine supports the SBC audio decoding and equlizer to offer the best audio quality.

In addition, to minimize the external components required for portable devices, a voltage sensor for battery, Li-ion battery charger, a switching regulator and LDOs are integrated to reduce BOM cost for various Bluetooth applications.

The device incorporates built-in self-test (BIST) and auto-calibration functions to simplify production test.

2. Features

System Specification

- Compliant with Bluetooth Specification v.3.0 (EDR) in 2.4 GHz ISM band

Baseband Hardware

- 16MHz main clock input
- Built-in internal ROM for program memory
- Built-in 32 KB RAM for data storage and baseband data transfer buffering
- Enhanced Power Control
- Bluetooth 2.1 features
  - Encryption Pause and Resume
  - Erroneous Data Reporting
  - Extended Inquiry Response
  - Link Supervision Timeout Changed Event
  - Non-Flushable Packet Boundary Flag
  - Secure Simple Pairing
  - Sniff Subtracting
- Support both Pico-net and Scatter-net applications
- Hard-wired logic for modulation, demodulation, access code correlation, whitening, forward error correction (FEC), header error check (HEC), shorten hamming code, CRC generation/checking, frame check sequence (FCS), encryption bit stream generation, and transmit pulse shaping
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels

- Fast Connection supported

RF Hardware

- Fully Bluetooth 3.0 (EDR) system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Build-in T/R switch for Class 2/3 application
- Build-in channel filter.
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.

Audio processor

- SBC decoding
- Packet error concealment

Audio Codec

- 16 bit stereo codec
- 94dB SNR DAC playback
- Integrate headphone amplifier for 16Ω speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in 10-bit Aux-ADC for battery monitor and voltage sense.
- LED driver

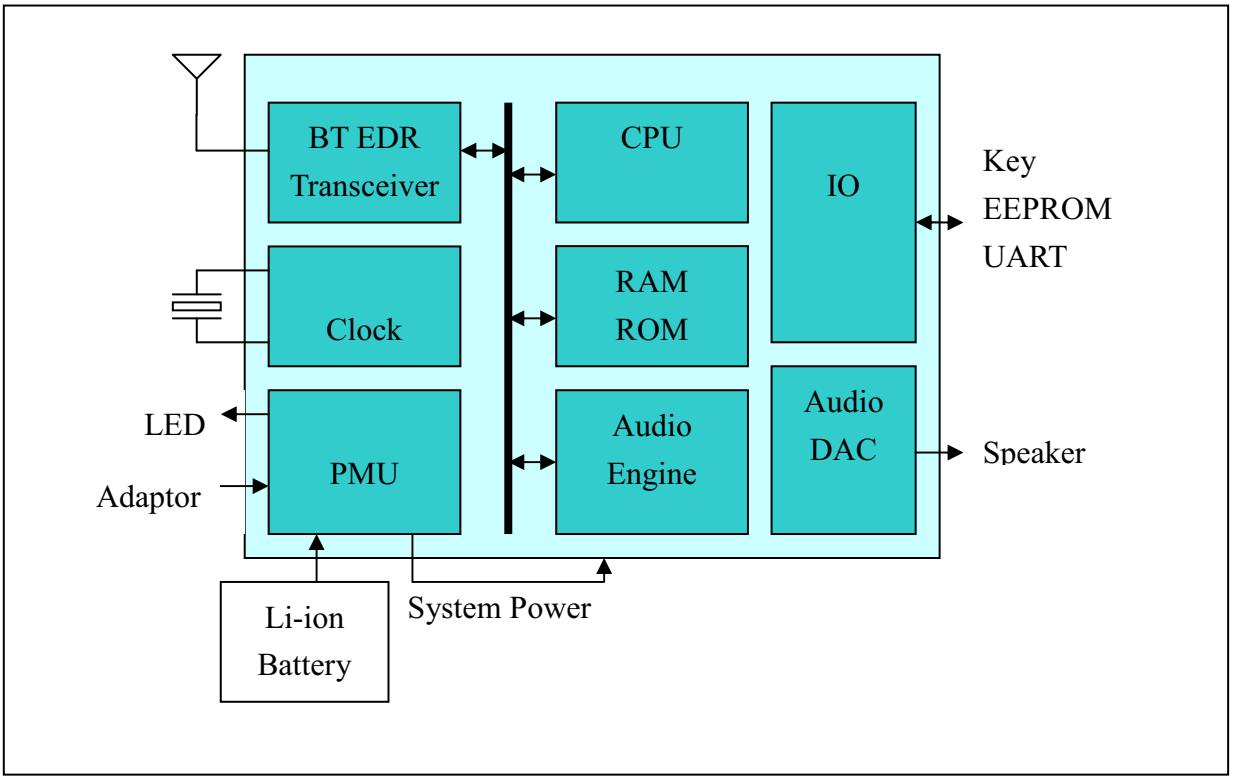
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

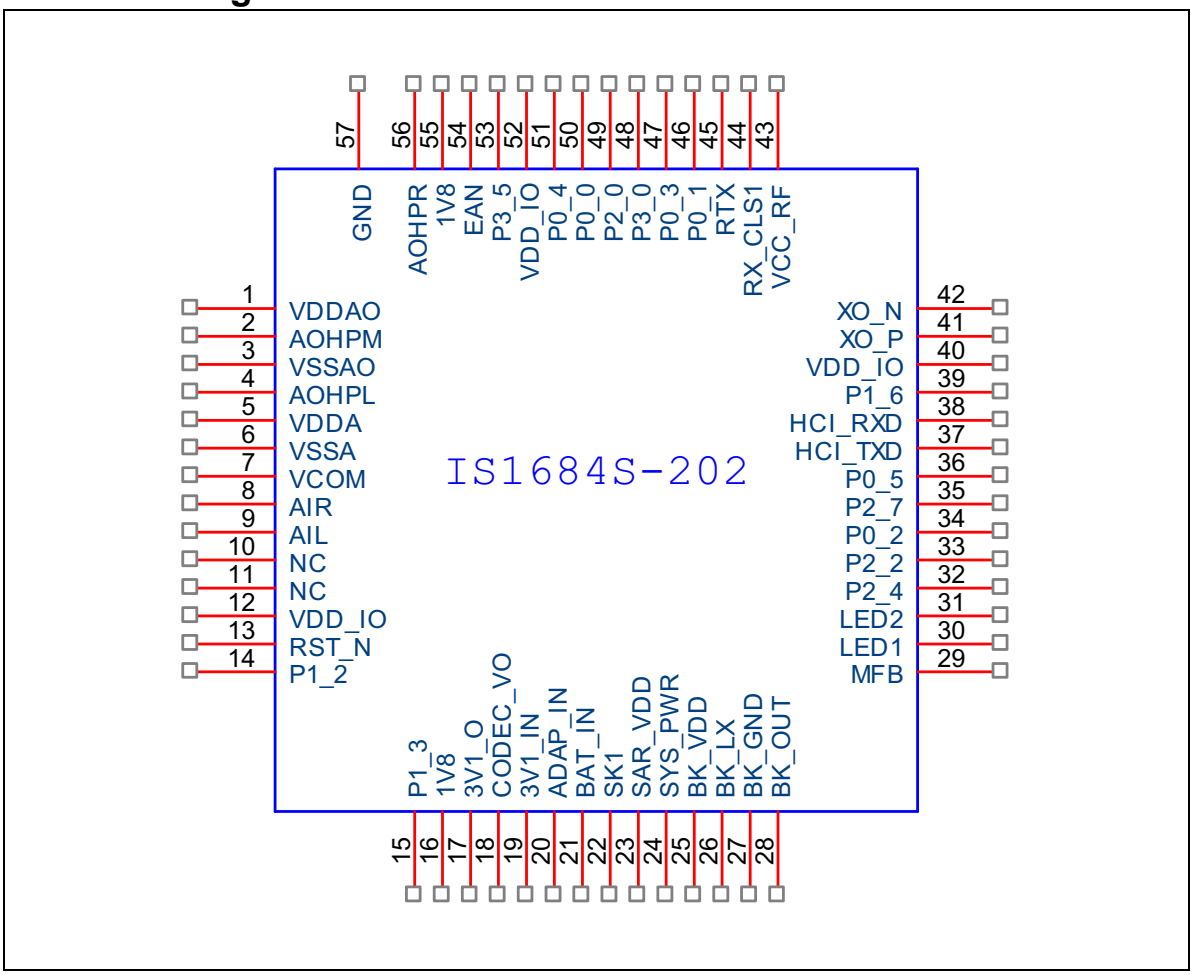
Package

- 7x7mm^2 56 pins, 0.4mm pitch SAW QFN standard package

3. Functional Diagram



4. Pin Assignment



5 Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers.
2	AO	AOHPM	Headphone common mode output/sense input
3	P	VSSAO	Negative power supply dedicated to CODEC output amplifiers
4	AO	AOHPL	L-channel analog headphone output
5	P	VDDA	Positive power supply/reference voltage for CODEC
6	P	VSSA	Negative reference/power supply for CODEC
7	AO	VCOM	Internal biasing voltage for CODEC
8	AI	AIR	R-channel single-ended analog inputs
9	AI	AIL	L-channel single-ended analog inputs
10	NC		
11	NC		
12	P	VDD_IO	I/O power supply input
13	AI	RST_N	KEY PIN for FT Test System Reset Pin
14	I/O	P1_2	GPIO, default pull-high input KEY PIN for FT Test EEPROM clock SCL Clock signal for OLED
15	I/O	P1_3	GPIO, default pull-high input KEY PIN for FT Test EEPROM data SDA Data signal for OLED
16	P	1V8	Core 1.8V power input
17	P	3V1_O	3.1V LDO output
18	P	CODEC_VO	3.1V LDO output for CODEC power
19	P	3V1_VIN	3.1V LDO input
20	P	ADAP_IN	Power adaptor input
21	P	BAT_IN	Battery input
22	AI	SK1	ADC analog input 1

Pin No.	I/O	Pin Name	Pin Descriptions
23	P	SAR_AVDD	SAR 1.8V input
24	P	SYS_PWR	System Power Output
25	P	BK_VDD	Buck VDD Power Input
26	P	BK_LX	Buck feedback input
27	P	BK_GND	Buck Ground
28	P	BK_OUT	Buck output
29	P	MFB	Multi-Function Push Button key, push high
30	AI	LED1	LED Driver 1
31	AI	LED2	LED Driver 2
32	I/O	P2_4	GPIO, default pull-high input KEY PIN for FT Test System Configuration, H: Boot Mode
33	I/O	P2_2	GPIO, default pull-low input. Keep alive for external LDO power enable application.
34	I/O	P0_2	GPIO, default pull-high input Play/Pause key as the default setting
35	I/O	P2_7	GPIO, default pull-high input FWD key when class 2 RF FWD key(short press) when class 1 RF
36	I/O	P0_5	GPIO, default pull-high input KEY PIN for FT Test REV key when class 2 RF REV key(short press) when class 1 RF
37	O	HCI_TXD	KEY PIN for FT Test HCI TX data
38	I	HCI_RXD	KEY PIN for FT Test HCI RX data
39	I/O	P1_6	GPIO P1_6, default pull-high input Volume down key when class 2 RF Audio AMP Enable when class 1 RF
40	P	VDD_IO	I/O power supply input
41	I	XO_P	16MHz Crystal input positive

Pin No.	I/O	Pin Name	Pin Descriptions
42	I	XO_N	16MHz Crystal input negative
43	RP	VCC_RF	RF power input for both synthesizer and TX/RX block
44	I	RX_CLASS1	Class1 RF RX path
45	I/O	RTX	Class2 RTX path; Class1/Class2 TX path
46	I/O	P0_1	GPIO, default pull-high input Volume up key when class 2 RF. Class1 Control signal of external TR switch when class 1 RF
47	I/O	P0_3	GPIO, default pull-high input KEY PIN for FT Test UART RX_IND when class 2 RF Class1 Control signal of external TR switch when class 1 RF
48	I/O	P3_0	GPIO, default pull-high input Line-in Detector (Low Active)
49	I/O	P2_0	GPIO, default pull-high input KEY PIN for FT Test System Configuration, H: Application L: Baseband(IBDK Mode)
50	I/O	P0_0	GPIO, default pull-low input. KEY PIN for FT Test Slide Switch Detector/TX_IND when class 2 RF
51	I/O	P0_4	GPIO, default pull-high input Audio AMP Enable when class 2 RF
52	P	VDD_IO	I/O power supply input
53	I/O	P3_5	GPIO 3_5, default pull-high input. Buzzer Signal Output
54	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
55	P	1V8	Core 1.8V power input
56	AO	AOHPR	R-channel single ended analog headphone output
57	P	GND	Exposed pad as ground

Application Note for GPIO Setting:

1) KEY PIN for FT Test
HCI_RXD, HCI_TXD, RST_N, P2_0, P2_4, P1_3, P1_2, P0_3, P0_5, P0_0

2) For Class2 RF application: VOL+:P0_1, VOL-: P1_6, FWD:P2_7, REV:P0_5, AUDIO AMP ENABLE: P0_4

3) For Class1 RF application: VOL+:P2_7(Long Press), VOL-: P0_5(Long Press), FWD:P2_7(Short Press) , REV: P0_5(Short Press) , AUDIO AMP ENABLE: P1_6

4) Play/Pause: P0_2

5) P1_2:EEPROM Clock/Clock Signal for OLED(5028-202 not support)
P1_3:EEPROM Data/Data Signal for OLED(5028-202 not support)

6) SLIDE SWITCH DETECT: P0_0

7) Buzzer Signal Output: P3_5

8) CLASS 1 RF TX: P0_1, CLASS 1 RF RX: P0_3

9) External LDO power enable keep alive: P2_2

10) System Configuration: P2_0, P2_4

11) P0_0/P0_3 are used as TX_IND/RX_IND of UART control in MCU application

6 Functional Description

6.1 Overall Architecture

The ISSC IS1684S integrates an enhanced EDR Bluetooth RF & BB core, HCI controller, audio engine and an ENHANCED 8051 processor with an internal mask ROM for program memory and SRAM for data memory. An innovative interconnection structure called the Common-Memory Architecture (CMA) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware.

For audio application and power management, IS1684S has build-in an audio processor, mono codec and power management unit to reduce the external components.

6.2 Radio Frequency (RF)

6.2.1 Transmitter

The internal PA has a maximum output power of +4dBm with level control 20dB from amplitude control. This is applied into Class 2/3 radios without external RF PA. For Class1 application, the build-in level control can be used with external PA for power control requirement.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

6.2.2 Receiver

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for external PA/LNA application.

An ADC is used to sample input analogue wave for digital demodulation. Before the ADC, a channel filter has been integrated into receiver channel to increase the anti-interference capacity and also reduce the external component count.

For avoiding temperature variation issues, a temperature sensor with temperature calibration is utilized into bias current and gain control of LNA, Mixers, and RF AMP.

6.2.3 Synthesizer

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.

6.3 MODEM

There are three different modulations for Bluetooth v3.0 (EDR). Table 6.3 summarizes these modulations and data rate.

Figure 6.3 Modulation type for Bluetooth v3.0 (EDR)

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8DPSK	3

6.3.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v3.0(EDR) specification.

Figure 6.3.1 Data format for BDR

Access Code	Header	Payload

6.3.2 Enhanced Data Rate MODEM (EDR)

On the Bluetooth v3.0(EDR) specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v3.0(EDR) specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

Figure 6.3.2.A Data format for EDR

Access Code	Header	Guard	Sync	Payload	Trailer

For π/4 DQPSK modulation, each symbol carries 2 bits of information. For its constellation diagram, although there are 8 possible phase states, the encoding scheme guarantees the trajectory of the modulation between symbols is restricted to 4 states. For a given starting

point, every phase change between symbols is restricted to +45°, +135°, -45°, and -135°.

Figure 6.3.2.B Phase shift & bit pattern for 2 MHz data rate

Phase Shift	Bit Pattern
+45° (+π/4)	00
+135° (+3π/4)	01
-135°(-3π/4)	11
-45°(-π/4)	10

For 8DPSK modulation, each symbol carries 3 bits of information. For its constellation diagram, it is similar toπ/4 DQPSK but the trajectory of the modulation between symbols has 8 possible phase states. For a given starting point, every phase change between symbols is restricted to 0°, +45°, +90°, +135°, +180°, -135°, -90°, and -45°.

Figure 6.3.2.C Phase shift & bit pattern for 3 MHz data rate

Phase Shift	Bit Pattern
0° (+0)	000
+45° (+π/4)	001
+90° (+π/2)	011
+135° (+3π/4)	010
+180° (+π)	110
-135° (-3π/4)	111
-90° (-π/2)	101

-45° (-π/4)	100

6.4 Baseband

The following modules implemented in hardware constitute the Bluetooth Baseband Core.

The frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address. The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

Bluetooth uses two types of FEC: 1/3 repetition code and (15, 10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.

6.5 MCU

The embedded processor for IS1684S is a single-cycle 8051 CPU. The embedded processor will be referred to as simply the processor, 8051, or MCU throughout the remainder of this document. There are a few minor differences between a standard 8051 and this CPU. These include:

1. Alteration of memory timings to match internal and external memory configurations.
2. Modification of idle mode to disable internal CPU clocking. Only externally-clocked interrupt sources can allow the CPU to recover from idle mode.

A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 7 interfaces spread amongst 5 physical busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus
- DMA bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a

status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.

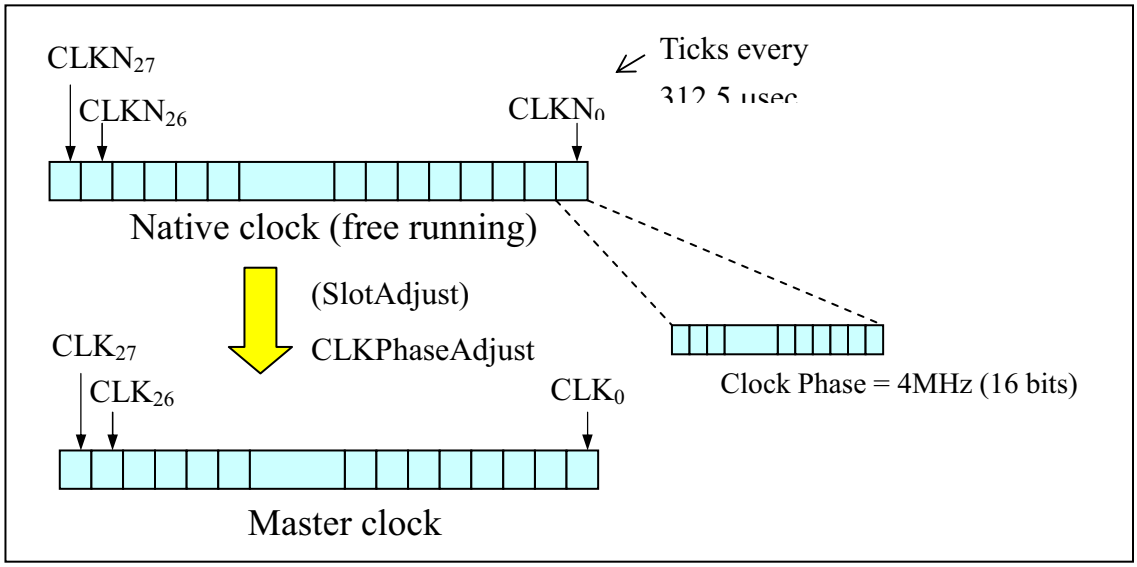
6.6 Bluetooth Clock and Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification. This clock provides the transmission and receiving timing of a half time slot (312.5 μs). Another finer counter implemented in 16 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. The counter is pre-scalable for the purpose of power saving operations. The diagram below describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt.

There are several timers provided by the system, two timers for TX/RX and the others for general purpose.

The powerful pre-scheduling functions for the transceiver are realized different sets of programmable timers. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time. Sub-tasks and timing for a TX task remain to be defined.

Figure 6.6 Bluetooth clock



6.7 HCI Control Logic for USB/UART

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

6.7.1 HCI UART Interface

An embedded HCI UART (Universal Asynchronous Receiver Transmitter) with programmable data rate up to 3Mbps is included in this design. The HCI UART supports the following functions:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 or x24 or x13 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

6.8 General Purpose I/O

The IS1684S provides 15 general purpose I/O ports. These general I/Os can be defined as input or output port individually by setting specific register bit. While setting as an input port, a build-in 50KΩ pull high or pull low resistor can be enabled for different application purpose.

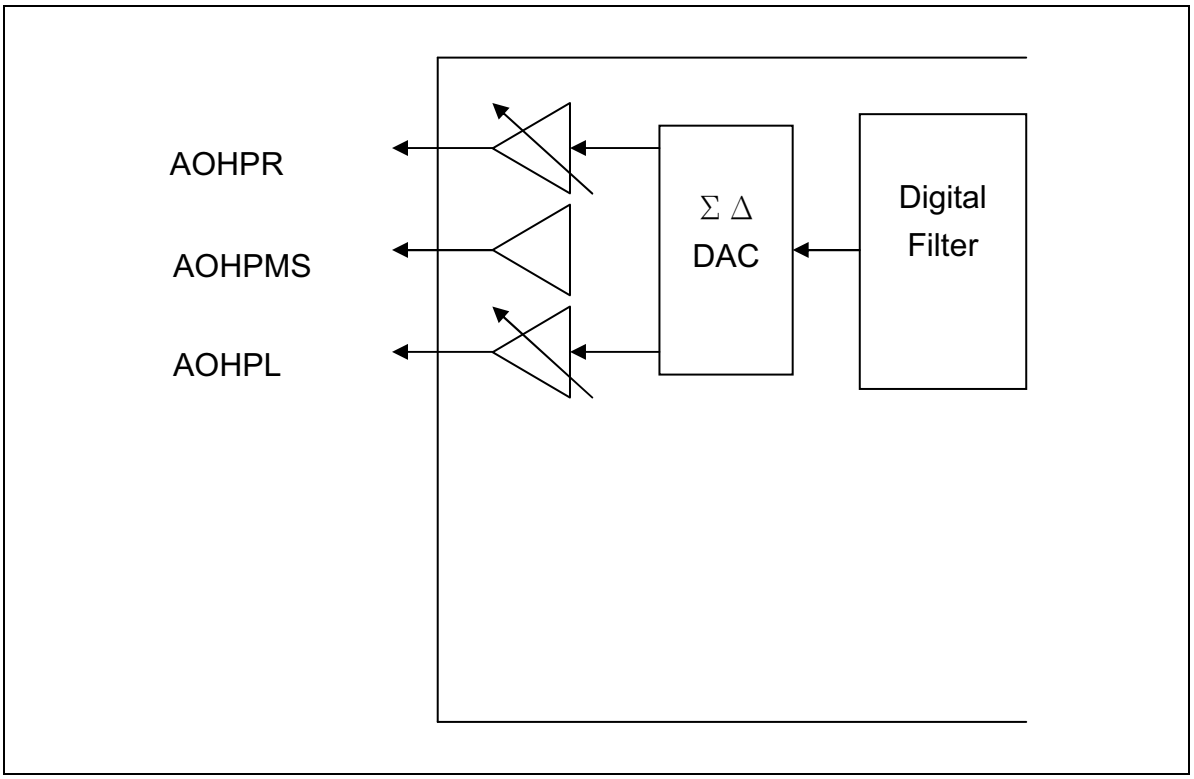
6.9 Audio Processor

The IS1684S builds in an enhanced audio engine to offer high quality of audio for audio application. The standard SBC A2DP audio function is implemented in the audio engine.

6.10 Audio DAC

The build in audio circuits contain a digital to analog converter (DAC) and a headphone driver. The DAC output is available for both line level and through the headphone amplifier to drive a low impedance headphone. The headphone output volume is adjustable by the combination of the digital/analog gain control.

Figure 6.10 Audio DAC



6.11 Auxiliary ADC

The 10-bit auxiliary analog to digital converter (SAR ADC) provides one dedicated channel for battery power detection and one other channel for external peripheral sensing. This ADC has 10 bits resolution that provides an accurate monitoring for battery voltage. The operating current is very low and almost consumes no power when disabled.

6.12 Power Management (PMU)

The power management unit of IS1684S includes several power control blocks, linear regulators, switch-mode regulator, Aux-ADC, LED driver and Lithium-ion/Polymer battery charger.

6.12.1 3V1_LDO

The IS1684S has build-in the programmable output voltage LDOs (1.8~3.2V) for codec and digital IO power supply. The programmable LDO is used to regulate the high input voltage from battery or adapter. This LDO needs 1uF bypass capacitor.

6.12.2 Buck regulator

The built-in programmable output voltage buck (1.8~2.4V) converts battery voltage for RF and baseband core power supply. This converter has high conversion efficiency and fast transient response.

6.12.3 Voltage Dectector

The 10-bit Successive-Approximation analog to digital converter (SAR ADC) monitors the battery power and adapter power for charging and power management control.

6.12.4 Li-ion Battery Charger

IS1684S includes a built-in battery charger optimized for use with lithium polymer batteries. The charger features a current sensor for charging control, user programmable current regulation and high accuracy voltage regulation. It charges the battery in four phases:

- reviving mode : 2mA charging current to charge BAT to 2.5V
- pre-charge mode : 0.1C charging current to charge BAT to 3.0V
- constant current mode : 0.xC (default 0.7C) charging current to charge BAT to 4.2V (programmable)
- constant voltage mode : charging is terminated while the charging current drops below 0.YC (default 0.13C)

Charging current in the constant current mode can be configured to provide a wide range of charging current up to 180mA (1mA per step). Charger will re-start charging if the battery voltage falls below an internal threshold.

System operation is allowed when the battery is charging.

6.13 Miscellaneous (Watchdog Timer, and Clock Divider)

System related functions such as watchdog timer, Endian control, and interrupt vectors are also provided. The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period.

7 Electrical Characteristics

Absolute Maximum Ratings

Rating		Min	Max	Max
Operation Temperature		-20ºC	+70ºC	ºC
Core supply voltage	VDD_CORE, VCC_RF, AVDD_SAR, AVDD_PLL	1.7V	1.98V	V
Codec supply voltage	VDD_AUDIO		3.3	V
I/O voltage	VDD_IO		3.3	V
Supply voltage	BK_VDD		4.7	V
	3V1_VIN		5	V
	BAT_IN		4.3	V
	ADAP_IN		6	V
	LED[1:0]		5	V
	Power switch		6	V

Recommended Operate Condition

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD18}	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage	1.62	1.8	1.92	V
V_{DDIO}	I/O supply voltage RF supply voltage	2.5	2.7	3.3	V
$T_{OPERATION}$	Operating temperature range	-20	+25	+70	ºC
T_{stg}	Storage temperature	-40		+125	ºC
V_{LDO}	LDO supply voltage	1.8		3.3	V
V_{BAT_IN}	Input voltage for SAR ADC	0.9		3.3	V

Radio Characteristics:

Transmitter section for BDR

VCC_RF = 2.7V Temperature = 25ºC		Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power			3	4.0	-6 to 4	dBm
RF power variation over temperature range with compensation enabled			±2			dB
RF power control range			20		≥16	dB
RF power range control resolution			0.5			dB
20dB bandwidth for modulated carrier			900		≤1000	KHz
ACP	F = F_0±2MHz		-28		≤-20	dBm
	F = F_0±3MHz		-46		≤-40	dBm
Note: F_0=2441MHz	F = F_0±>3MHz		-54		≤-40	dBm
Δf_{1avg} maximum modulation		150		165	$140<\Delta f_{1avg}<175$	KHz
Δf_{2max} maximum modulation		140		150	≥115	KHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.95	1		≥0.80	
ICFT (abs)		0	5	10	75	KHz
Drift rate (abs)		2		7	≤20	KHz/50us
Drift (single slot packet, abs)			12		≤25	KHz
2nd harmonic content @ Tx= 4dBm			-53		≤-47	dBm
3rd harmonic content @ Tx= 4dBm			-55		≤-47	dBm

Receiver section for BDR

Temperature = 25ºC	Frequency (GHz)	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER for all basic rate packet types	2.402		-91		≤-70	dBm
	2.441		-91			
	2.480		-91			
Maximum received signal at 0.1% BER			-10		≥-20	dBm
C/I co-channel			5		≤11	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	F = F_0+1MHz		-7		≤0	dB
	F = F_0-1MHz		-7		≤0	dB
	F = F_0+2MHz		-36		≤-30	dB
	F = F_0-2MHz		-22		≤-9	dB
	F = F_0-3MHz		-24		≤-20	dB
	F = F_0+5MHz		-50		≤-40	dB
	F = F_{image}		-22		≤-9	dB
Maximum level of intermodulation interferers			-38		≥-39	dB

Transmitter Section for EDR

Temperature = 25ºC		Min	Typ	Max	Bluetooth specification	Unit
Relative transmit power			-1.6		-4 to 1	dB
π/4 DQPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		5		≤10 for all blocks	KHz
	$\|\omega_i\|$ initial freq. error		10		≤75 for all blocks	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		10		≤75 for all blocks	KHz
8DPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		5		≤10 for all blocks	KHz
	$\|\omega_i\|$ initial freq. error		10		≤75 for all blocks	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		10		≤75 for all blocks	KHz
π/4 DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤20	%
	99% DEVM		Pass		≤30	%
	Peak DEVM			25	≤35	%
8DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤13	%
	99% DEVM		Pass		≤20	%
	Peak DEVM			20	≤25	%

In-band spurious emissions Note: F_0=2441MHz	F > F_0+3MHz		<-54		≤-40	dBm
	F = F_0-3MHz		-46		≤-40	dBm
	F = F_0-2MHz		-28		≤-20	dBm
	F = F_0-1MHz		-30		≤-26	dBm
	F = F_0+1MHz		-30		≤-26	dBm
	F = F_0+2MHz		-28		≤-20	dBm
	F = F_0+3MHz		-46		≤-40	dBm
EDR differential phase encoding			100		≥99	%

Receiver Section for EDR

Temperature = 25ºC		Frequency (GHz)	Modulation	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.01% BER		2.402	π/4 DQPSK		-92		≤-70	dBm
		2.441	π/4 DQPSK		-92			
		2.480	π/4 DQPSK		-92			
		2.402	8DPSK		-84		≤-70	dBm
		2.441	8DPSK		-84			
		2.480	8DPSK		-84			
Maximum received signal at 0.1% BER			π/4 DQPSK		-10		≥-20	dBm
			8DPSK		-10		≥-20	
C/I co-channel at 0.1% BER			π/4 DQPSK		4		≤13	dB
			8DPSK		5		≤21	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	$F = F_0$+1MHz		π/4 DQPSK		-14		≤0	dB
			8DPSK		-8		≤5	dB
	$F = F_0$-1MHz		π/4 DQPSK		-13		≤0	dB
			8DPSK		-8		≤5	dB
	$F = F_0$+2MHz		π/4 DQPSK		-38		≤-30	dB
			8DPSK		-34		≤-25	dB
	$F = F_0$-2MHz		π/4 DQPSK		-21		≤-7	dB

		8DPSK		-21		≤0	dB
	F = F_0-3MHz	π/4 DQPSK		-27		≤-20	dB
		8DPSK		-20		≤-13	dB
	F = F_0+5MHz	π/4 DQPSK		-52		≤-40	dB
		8DPSK		-45		≤-33	dB
	F = F_{image}	π/4 DQPSK		-21		≤-7	dB
		8DPSK		-21		≤0	dB

Audio DAC

Test Condition: T= 25°C, Vdd=2.8V, 1KHz sine wave input, Bandwidth= 20~20KHz						
Parameter	**Condition**		**Min.**	**Typ.**	**Max.**	**Unit**
Output Level	Full scale			2.1		Vpp
Resolution			16			bits
Output Sampling Rate			8		48	KHz
SNR	f_{in}=1KHz B/W=20~20KHz A-weighted THD+N < 0.01% 0dBFS signal Load=100KΩ	8KHz		94		dB
		16KHz		94		dB
		32KHz		94		dB
		44.1KHz		94		dB
		48KHz		94		dB
Max Output Power	R_L=16Ohm			35		mW
	R_L=32Ohm			17		mW
THD+N	16Ohm load				0.05	%
	100KΩ load				0.01	%
Digital Gain			-54		4.85	dB
Digital Gain Resolution				6		dB
Analog Gain			-28		3	dB
Analog Gain step				1		dB
Output resistance	R_L		8	16		Ohm
Output capacitance	Cp				500	pF
Crosstalk between channels	L vs. R, measured at -10dBFS@1KHz input			-90	-80	dB
Analog supply voltage (AVDD)			1.8	2.8	3.0	V

Battery Charger

Charging Mode (BAT_IN rising to 4.2V)		Min	Typ	Max	Unit
Operation Temperature		-20		70	℃
Input Voltage (Vin) Note: It needs more time to get battery fully charged when Vin=4.5V		4.5		6	V
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)			0.1C		mA
Trickle charge voltage threshold			3		V
Maximum battery charge current	Headroom > 0.7V		350		mA
	Headroom = 0.3V		150		mA
Minimum battery charge current	Headroom > 0.7V		1		mA
	Headroom = 0.3V		1		mA
Battery charge termination current, % of fast charge current			10		%
Battery recharge hysteresis (Note1)			100		mV
Battery recharge current (Note2) Note: C → Battery capacity			0.25C		mA

Note1：When charging complete and the adapter is still in, the battery voltage will slowly drop down. When the voltage drop is larger than 100mV from the full voltage, the re-charging cycle will start.

Note2：If the battery voltage during plug in is larger than 4V, the charging current will be limited to 0.25C to avoid the battery voltage overshoot.

Switching Regulator

Normal Operation		Min	Typ	Max	Unit
Operation Temperature		-20		70	℃
Input Voltage (Vin)		3	3.7	4.5	V
Output Voltage (Vout)		1.6	1.85	2.4	mA
Output Ripple				20	mVrms
Max. Average Load Current(I_{load})		120			mA
Max. Output Current (peak)		200			mA
Conversion Efficiency (Bat.@3.7V)	I_{load} =50mA		88		%
	I_{load} ≥ 10mA		80		
	I_{load} ≥ 250uA		65		
Switching Frequency			800		KHz
Start-up current Limit		0	50	210	mA
Start-up Settling Time			1.2	2	ms
Shutdown Current				<1	uA

LDO

Normal Operation		Min	Typ	Max	Unit
Input Voltage (Vin)		3.0		4.5	V
Output Voltage (V_{OUT}) (1) V_{OUT_CODEC} (2) V_{OUT_IO}	V_{OUT} = 2.9V (2.4~3.4V)		2.9		V
	V_{OUT} = 1.8V (1.3~2.3V)		1.8		
Accuracy (V_{IN}=3.7V, I_{LOAD}=100mA, 27'C)			±5		%
Output Voltage adjustable step			100		mV/Step
Output adjustment range			±0.5		V
Start-up inrush current			200	400	mA
Start-up Settling Time			250	500	μs
Output current(average)				100	mA
Output Current(peak)				150	mA
Drop-out voltage (I_{load} = maximum output current)				300	mV
Quiescent Current (excluding load, I_{load} < 1mA)			45		μA
Load Regulation (I_{load} = 0mA to 100mA), ΔVout				80	mV
Shutdown Current				<1	μA

Note: Two 100mA LDOs, one for IO and one for audio CODEC.

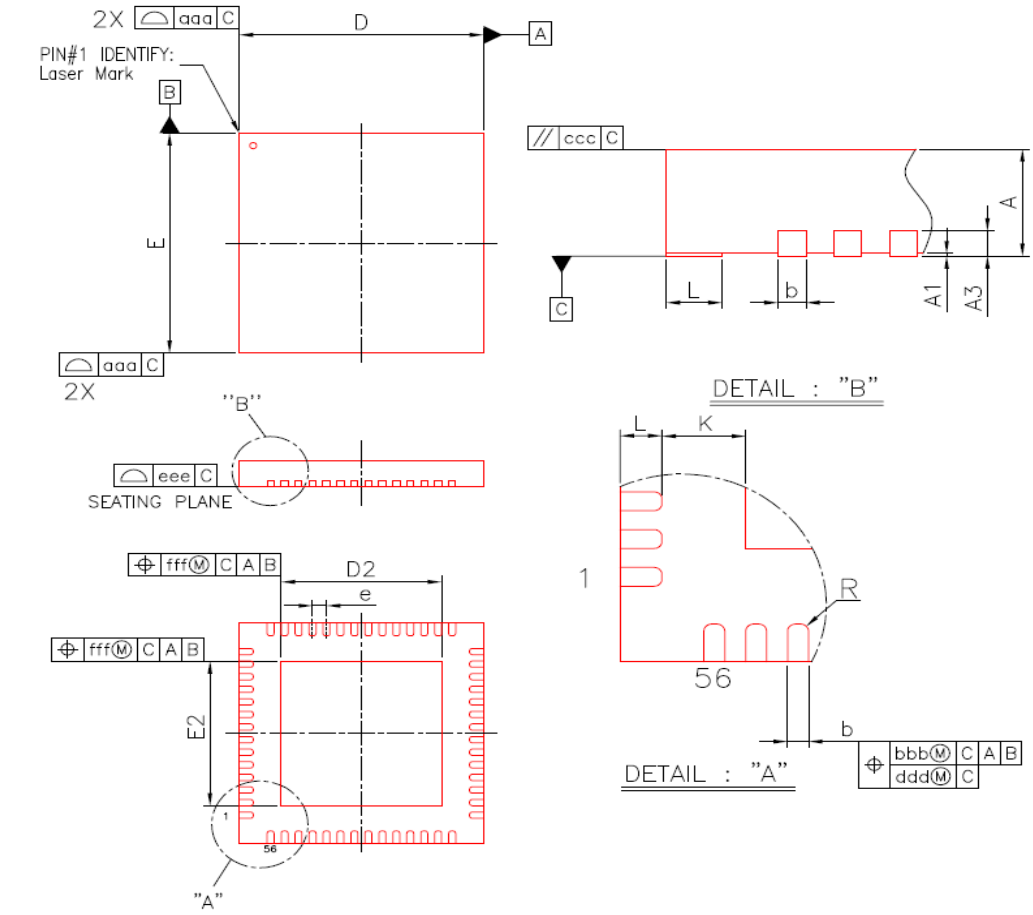
Clock

Parameters	MIN	TYP	MAX	Unit
Crystal Frequency		16		MHz
Frequency Tolerence		±20		ppm
Operating Temperature	-20		70	^{O}C
Trimming Capacitance		6.4		pF
Trimming Step Size		0.2		pF

Digital GPIO (2.8V)

Parameters	MIN	TYP	MAX	Unit
Input Voltage	2.7	3	3.6	V
V_{IH} (Input High Voltage)	2.0		Vdd	V
V_{IL} (Input Low Voltage)	0		0.8	V
Input Reference Resistor				
R_{PU} (Pull-Up Resistor)		50K		Ohm
R_{PD} (Pull-Down Resistor)		50K		Ohm
Output Voltage				
V_{OH} (Output High Voltage)	2.4		Vdd	V
V_{OL} (Output Low Voltage)	0		0.4	V

8 Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D2	4.45	4.60	4.75	0.175	0.181	0.187
E2	4.45	4.60	4.75	0.175	0.181	0.187
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

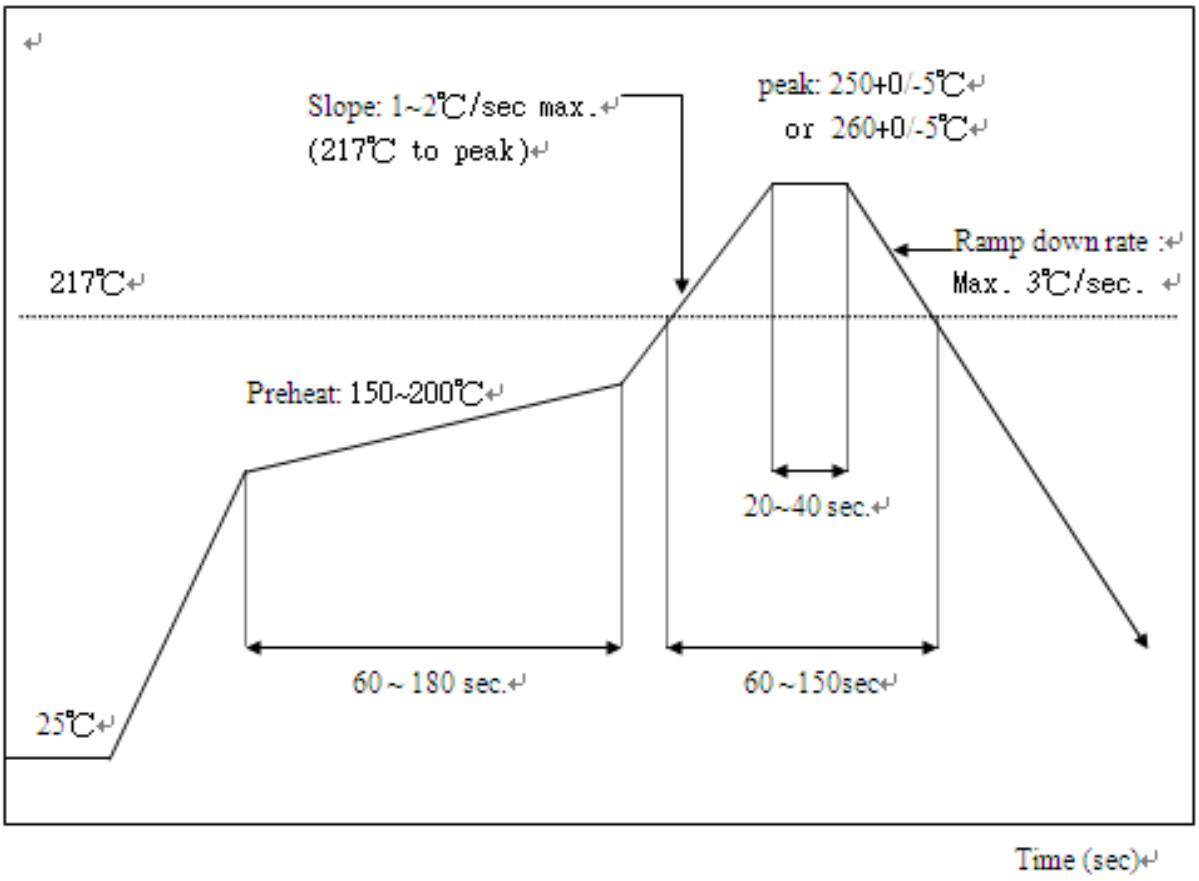
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Appendix A. Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.
Preheat：150~200C、60~180 seconds
Temperature maintained above 217℃ : 60~150 seconds
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.
Peak temperature：250+0/-5℃ or 260+0/-5℃
Ramp-down rate : 3℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minus



Appendix B. BQB certification

TPG Project	ISSC Bluetooth 3.0(EDR) Single Chip (Component (Tested))
Qualified Design ID (QD ID)	B016749 | Export PICS
PRD 1.0 ID (QP ID)	
Design Name	ISSC Bluetooth 3.0(EDR) Single Chip
Wi-Fi® Certification ID	
Subsetted Designs	**Date Created** / **Type** / **PICS**: Jun 28, 2010 / Main / PICS
Member Company	ISSC Technologies Corp.
Specification Name	3.0
Core Spec Addenda	N/A
Design Model Number	IS1XYZ, where X, Y and Z means 1~9
Hardware Version Number	ISBT_BB_v30
Software Version Number	ISBT_BB_v30
Qualification Assessment Date	July/21/2010
Listing Date	July/21/2010
Design Description	ISSC Bluetooth 3.0(EDR) Single Chip
Product Type	Component (Tested)
Technical Data Sheet (RIN)	** Open Reference Integration Notes (RIN) **
Listed By	Charlie Lee
BQE	Jan-Willem Vonk
Profile / Protocol	**Role / Version (If Any)**
Baseband	
Radio	
Link Manager	