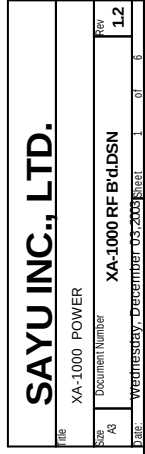
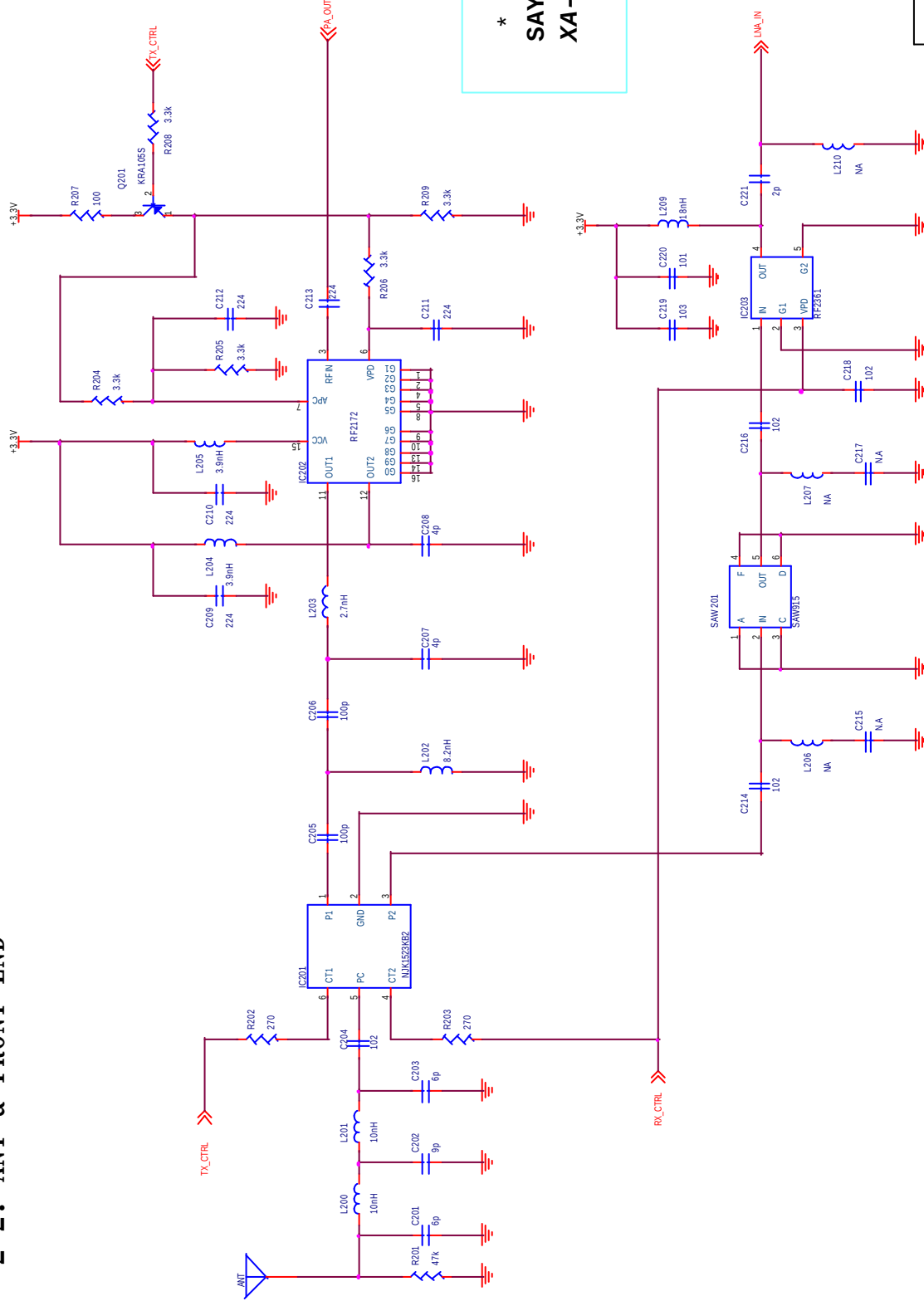


2-1. REGULATOR



2-2. ANT & FRONT END



* PCB Marking "
SAYU INC., LTD.
XA-1000 B'd Rev 1.2

SAYU INC., LTD.

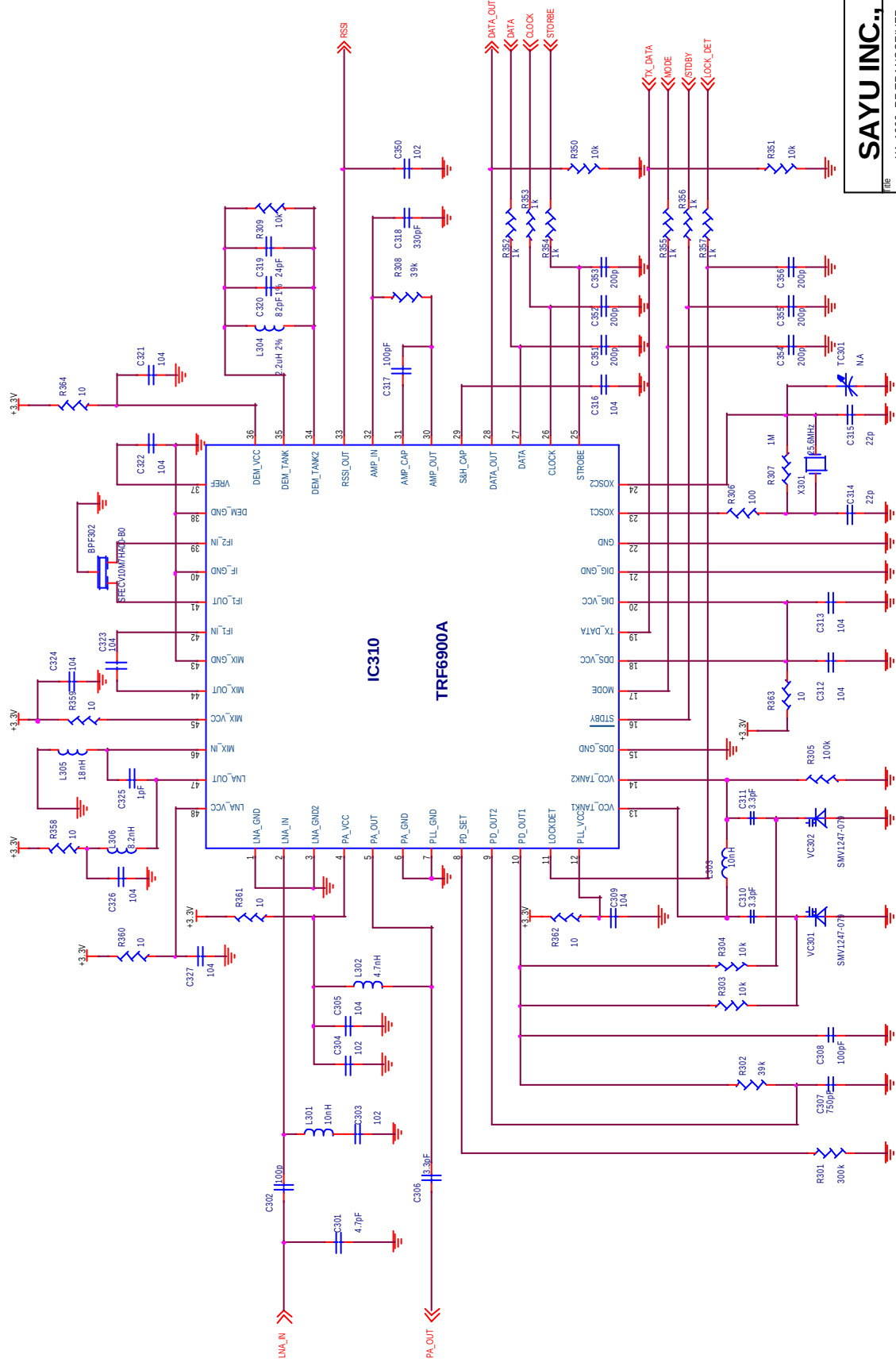
XA-1000 ANT & FRONT END

Document Number XA-1000 RF B'd.DSN

Rev 1.2

Wednesday, December 03, 2009 5:08 PM

2-3. RF TRANSCEIVER



SAYU INC., LTD.

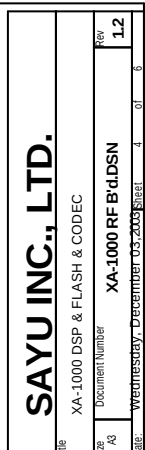
XA-1000 RF TRANSCEIVER

Document Number
XA-1000 RF B'd.DSN

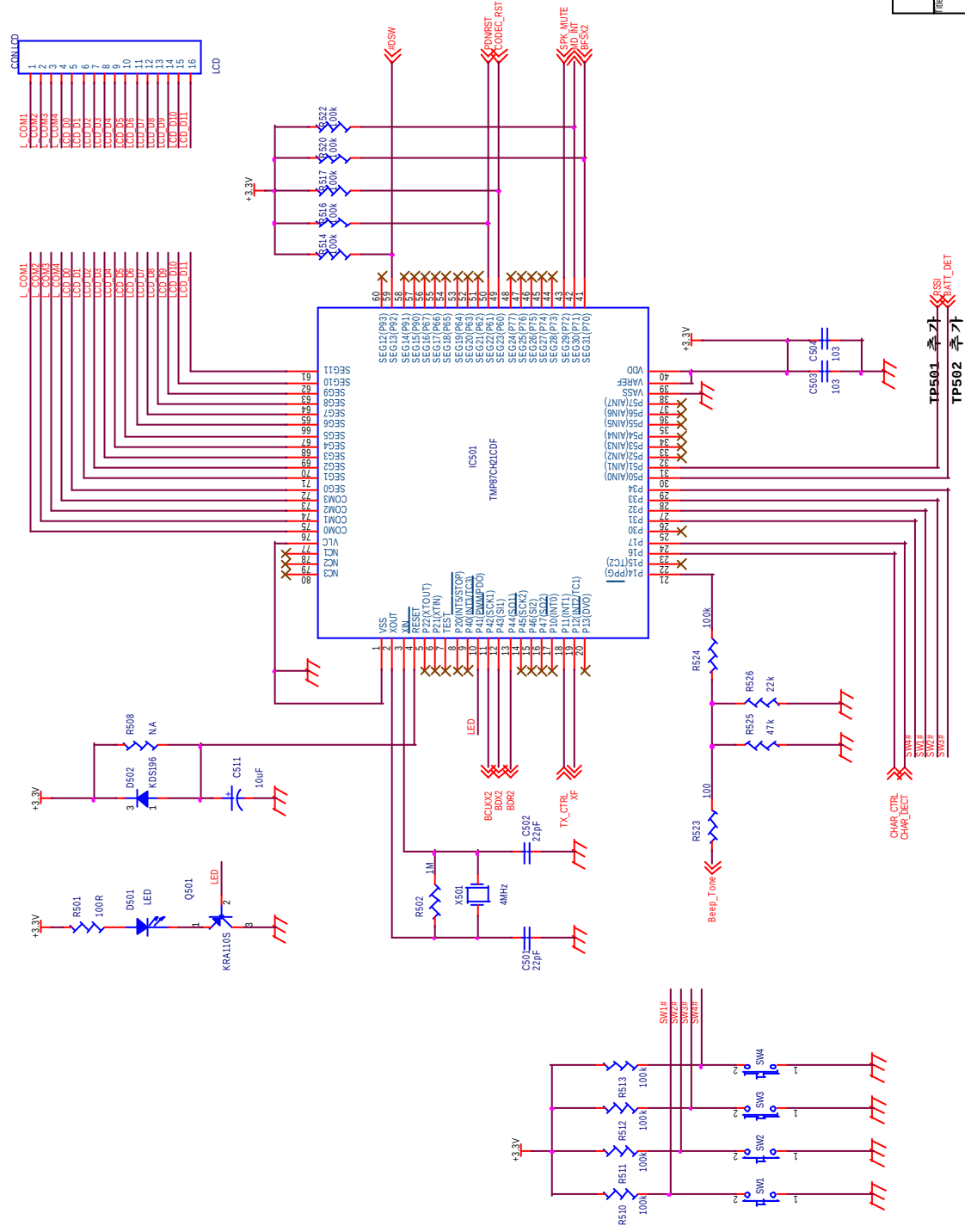
Rev
1.2

Wednesday, December 03, 2008 5:08 PM

Timing diagram for the 74VHC04-100. The diagram shows the relationship between the LOCK DET MODE pin, the ENVILOFF pin, and the READY pin. The LOCK DET MODE pin is shown with a pulse from 0 to 1. The ENVILOFF pin is shown with a pulse from 0 to 1. The READY pin is shown with a pulse from 0 to 1. The diagram is divided into three sections: LOCK DET MODE, ENVILOFF, and READY. The LOCK DET MODE section shows the pulse from 0 to 1. The ENVILOFF section shows the pulse from 0 to 1. The READY section shows the pulse from 0 to 1. The diagram is labeled with 'LOCK DET MODE', 'ENVILOFF', and 'READY'.



2-5. MCU & LCD



SAYU INC., LTD.

XA-1000 MCU & LCD

Document Number

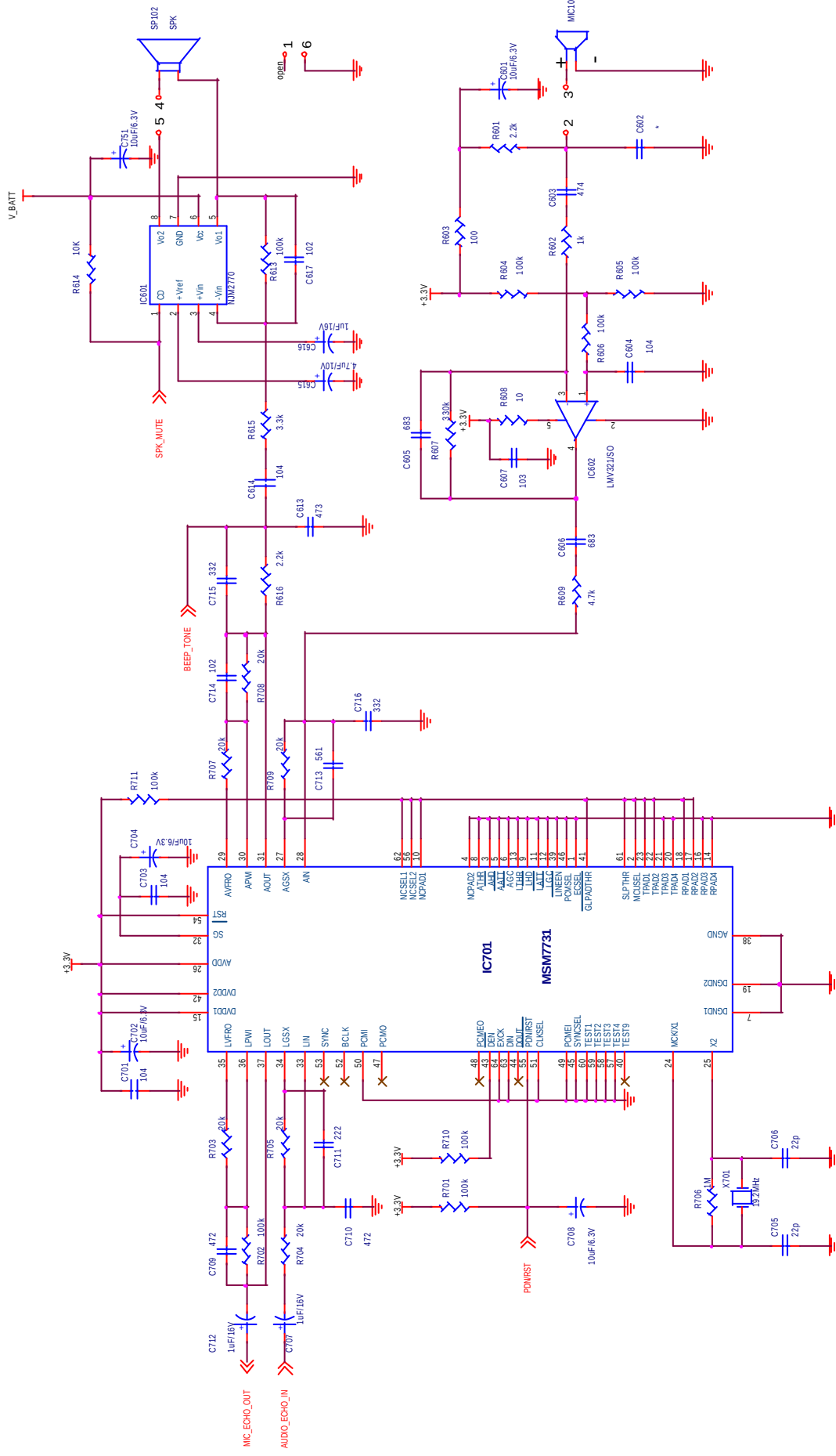
XA-1000 RF B'd.DSN

Rev

1.2

Wednesday, December 05, 2008 5:01 PM

2-6. AUDIO _ ECHO



SAYU INC., LTD.

XA-1000 AUDIO _ ECHO

Document Number

XA-1000 RF B'd.DSN

Wednesday, December 03, 2003 11:01 AM

Rev 1.2