FCC Part 15 Certification
Test Report

910.5MHz – 918.5MHz Multi-Channel Transmitter

FCC ID: RPE1000-7315

FCC Rule Part: 15.249

ACS Report Number: 04-0038-15C249

Manufacturer: VeriFiber, LLC.
Model: VT31XX

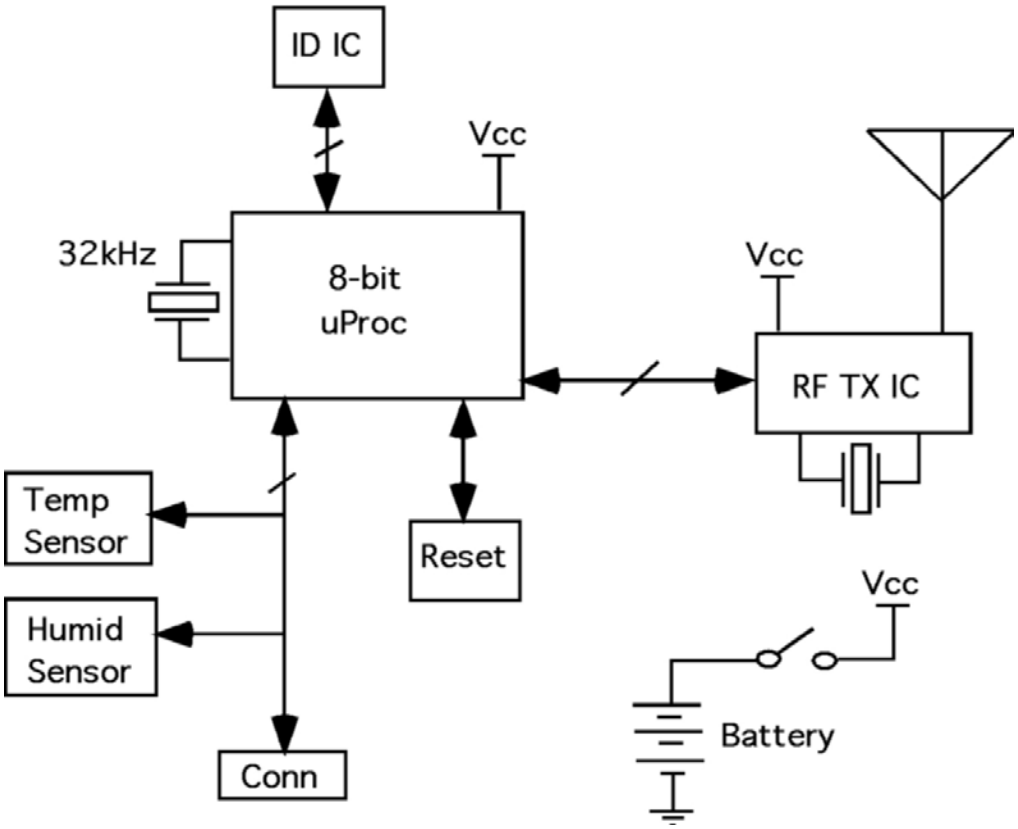
Theory of Operation

Theory of Operation for the VT31XX

MicroController Section

The VT31xx is controlled by a TI MPS 430 series microprocessor. It is running at 32kHz and performs all the sensor activation, sensor measurements, data packetization, data whitening, and control of the transmitter IC. The unique task the microprocessor does is that it takes sensor measurements and intelligently conserves battery usage and RF frequency usage. The measurements evolve from a timed event function when initially powered up to an event driven function. Initially, the sensor measurements are at a predetermined timed event. This is programmable in the microprocessor from 30 sec to 300sec. As the unit measurements' evolve, the microprocessor tracks changes in the sensor measurement. If no change is recorded over a pre-specified limit (30 sec), the unit will only transmit data at a 5-minute (300Sec) interval as a heartbeat operation. This is done for battery conservation and spectrum efficiency. If the sensor measurement surpasses the pre-specified limit change, at the measurement interval, the transmitter will immediately send the data and revert to a 30 sec interval. The transmission interval is dithered using a pseudorandom algorithm to reduce collision with multiple transmitters. The burst duration is approximately 20 msec.

VT31XX Wireless Remote Block Diagram



TRANSMITTER Section

The transmitter section is based on the MC33493, a PLL tuned low power UHF transmitter. Four digital input pins (ENABLE, DATA, BAND and MODE) enable the circuit to be controlled by a microprocessor. The BAND and MODE are permanently configured. The power supply voltage ranges from 2.7V to 3.6V allowing operation with a single lithium cell. The Phase Frequency Detector (PFD) and the loop filter are fully integrated. The exact output frequency is equal to: $f_{RFOUT} = f_{XTAL} \times$ [PLL Divider Ratio]. The FSK modulation is achieved by crystal pulling. An internal switch connected to CFSK pin enables to switch the external crystal load capacitors. The output stage is a single ended square wave switched current source. Harmonics are present in the output current drive. Their radiated absolute level depends on the antenna characteristics and output power. A resistor (R4) connected to the REXT pin controls the output power allowing a trade-off between radiated power and current consumption

When the battery voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off. This is a secondary failsafe protection feature. The circuit is latched until a low level is applied on pin ENABLE.