Preliminary

FOCUS AMR Board

Design Document

Version 1.0 (Preliminary)

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Revision History

Date	Revision done by	Revision	Comments
October 9, 2003	Ashok Mahadevan	1.0	Initial version based on the S4 document

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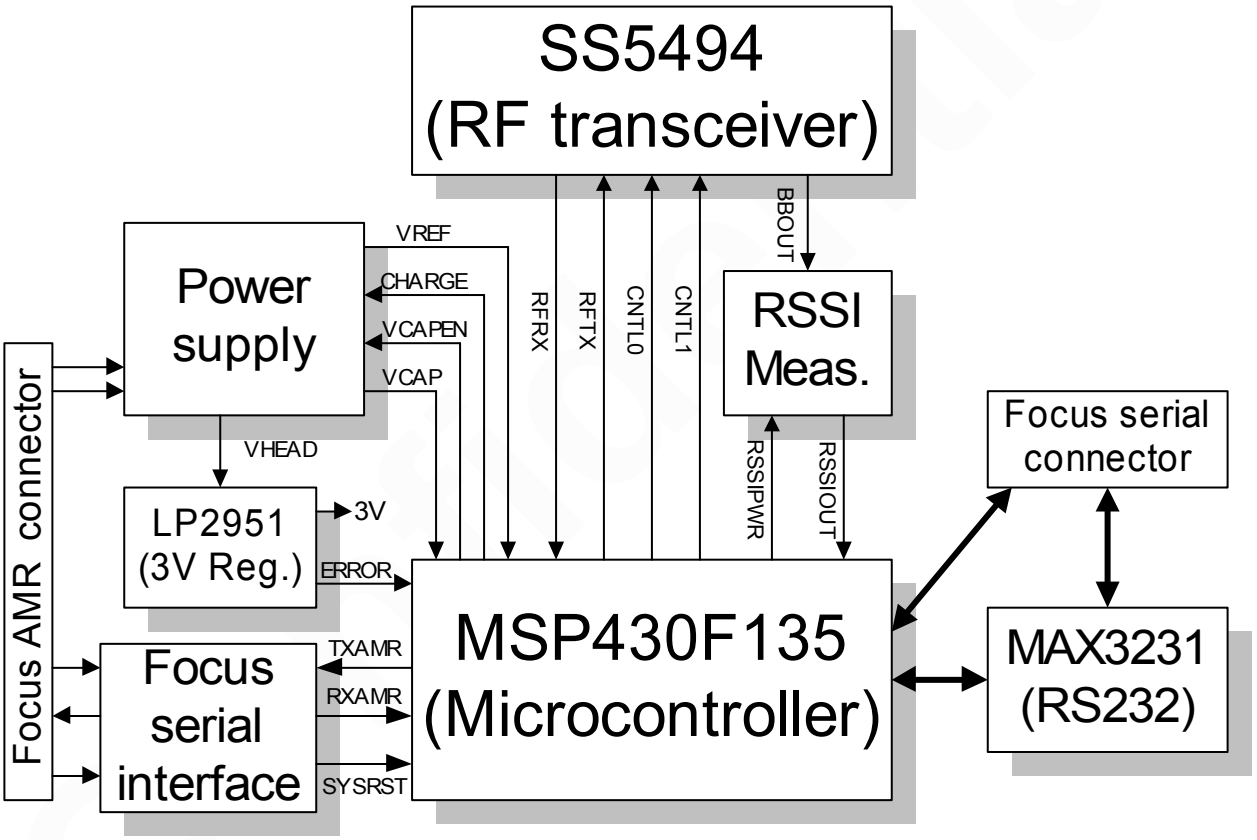
1. Introduction

This note attempts to document the design of the hardware for the Statsignal FOCUS AMR section. The AMR section is intended to be integrated in a Landis+GYR FOCUS electric meter, in all of its meter forms. The FOCUS AMR section will allow remote data acquisition from the FOCUS meter and enable the FOCUS meter to be a part of the Statsignal RF network. The FOCUS AMR board uses the RFM radio transceiver part with OOK mode of operation. The FOCUS AMR section is qualified for operation between a temperature range of –40C to +85C at all humidities, from 0 to 100% relative humidity and condensing.

A block diagram of the FOCUS AMR board is shown along with the major signal paths.



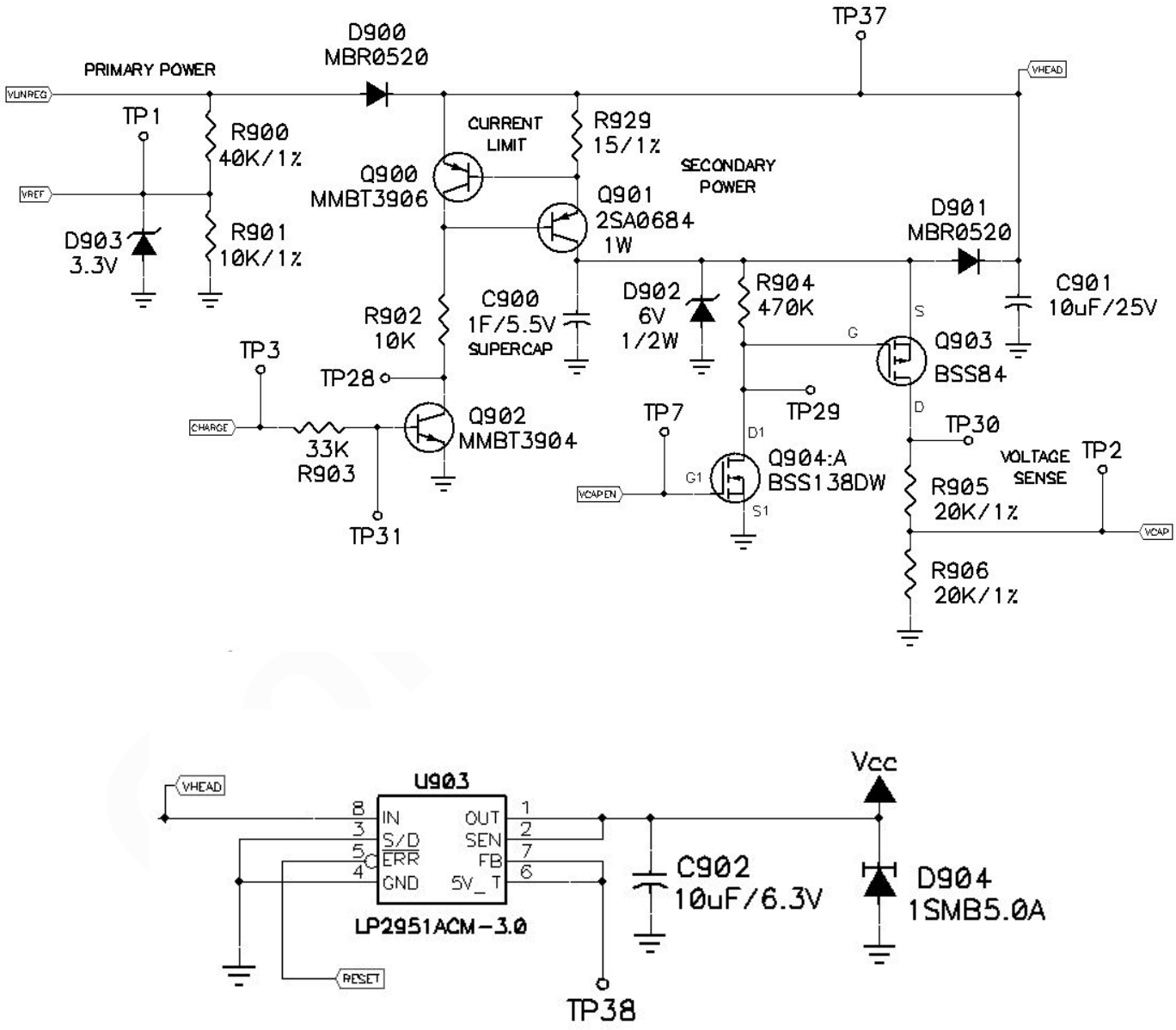
The FOCUS AMR board consists of the following major functional blocks:

1) *Power supply*
2) *Microcontroller*
3) *RF Transceiver*
4) *RSSI measurement*
5) *Serial I/O and interfacing*

In addition to the major blocks mentioned, there are some smaller connections used as test/debug points, for tilt detection and JTAG programming of the microcontroller.

2. Power supply

The power supply circuit provides the regulated 3VDC (Vcc) required to power the different sections of the FOCUS AMR board. The power supply circuit performs three major functions: voltage monitoring and sensing, supplying backup power using a Supercapacitor, and voltage regulation.



The primary source of power is the unregulated DC voltage (VUNREG) coming from the FOCUS metrology section. During normal operation, the raw DC voltage is fed through Schottky diode D900 to the LP2951ACM-3.0 regulator U903. The 3VDC output of this regulator (Vcc) is used to power the FOCUS AMR section. The raw DC voltage is also used to charge the Supercapacitor C900 through a current limiting circuit comprised of Q900, Q901 and R929, with resistor R929 setting the charging current. R903, Q902 and R902 allow the microcontroller to turn ON/OFF the charging of the Supercapacitor by controlling the state of the CHARGE pin. The zener diode D902 is used to protect the Supercapacitor from being overcharged in case there is a firmware malfunction that leaves the charging circuit on permanently.

R904, Q904A and Q903 form an analog switch that is controlled by the state of the VCAPEN pin from the microcontroller. When VCAPEN is asserted, Q904A and Q903 turn on and the voltage present on the Supercapacitor is available on the drain pin of Q903. Resistors R905 and R906 form a voltage divider that scales this voltage down and allows the microcontroller to read the Supercapacitor voltage on the VCAP pin. Note that the analog switch will not turn on until the voltage across the Supercapacitor reaches the minimum turn-on threshold (Vgs) of P-Channel MOSFET Q903. Thus, the Supercapacitor voltage cannot be monitored below about 2 VDC.

The microcontroller can periodically monitor the voltage on the Supercapacitor, and if it falls below a preset firmware threshold, it can turn on the charging circuit. Once the voltage on the Supercapacitor rises above another preset firmware threshold, the microcontroller can then turn off the charging circuit. In this way, the voltage on the Supercapacitor can be continuously topped off by the microcontroller.

Resistors R901 and R902 form a voltage divider that scales down the raw input VUNREG voltage. This scaled down voltage, available on the VREF pin, allows the microcontroller to monitor the VUNREG voltage and detect AC mains power outage condition. The zener diode D903 is used as protection if VUNREG should rise too high. When there is an AC mains voltage failure, the unregulated DC voltage (VUNREG) drops as a consequence. The charge stored in the Supercapacitor is used to provide backup power to the FOCUS AMR section through Schottky diode D901. Diode D900 prevents the Supercapacitor voltage from discharging through the primary VUNREG path during a power failure condition.

A power-on reset circuit is needed to hold the system in a reset condition on initial power-up and during a brownout condition until the power supply voltage has stabilized. The ERROR output of the LP2951ACM regulator U903, which is connected to the RESET input of the microcontroller, is used to provide this functionality. This open-collector ERROR signal is asserted by U903 whenever the regulator output voltage is out of spec by more than 5%. RESET will be asserted until Vcc rises above 2.85V on power-up, and if Vcc drops below 2.85V during a brownout condition.

3. RF Transceiver

All RF communications on the FOCUS AMR section is performed by the RF Monolithics TR-1000 Hybrid Transceiver (U902), under direct control of the microcontroller firmware. The TR-1000 is a low-power, single-channel radio that operates at a fixed frequency of 916.5 MHz. Data rates of up to 115.2 Kbps are supported, and the hybrid design requires very few external components for operation.

The RF transceiver supports four different modes of operation: receive mode, OOK transmit mode, ASK transmit mode, and power-down (sleep) mode. The mode of operation is controlled in the firmware by asserting the appropriate logic levels on the CNTL0 and CNTL1 signals.

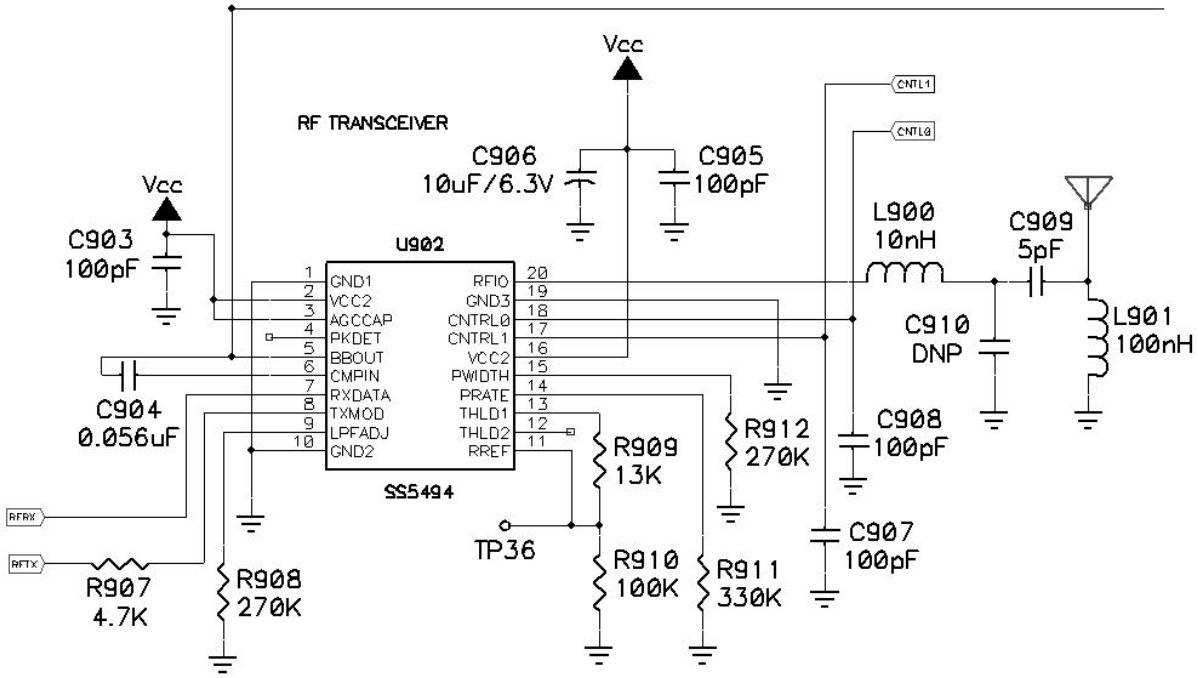
In receive mode, the demodulated receive signal is output on the RXDATA pin, which is connected directly to the microcontroller (RFRX) for continuous monitoring by the firmware. A 1M pull-down resistor (R924) is provided to maintain a valid logic level on the receive signal when the RF transceiver is placed in transmit or power-down modes.

In transmit mode, the encoded data stream is driven by the microcontroller on the RFTX signal. The logic high voltage at RFTX determines the peak RF transmit power by setting the current through resistor R907 into the TXMOD pin (U902). The following equation can be used to determine the peak RF output power:

$$Po = 4.8 * (Itx)^2$$ where Po is in mW, and peak modulation current Itx is in mA.

With a series resistance of 6800 ohms and a logic high voltage of 3 volts DC, a peak transmit power of just under 1mW is achieved. The RF transceiver can also be placed in power-down or "sleep" mode. In this mode, all transceiver operation is disabled and a power supply current of less than 5uA can be achieved.

Refer to the RF Monolithics *TR-1000 Data Sheet*, and *ASH Transceiver Designer's Guide* for more information. Also refer to section 7 for special PCB layout considerations.

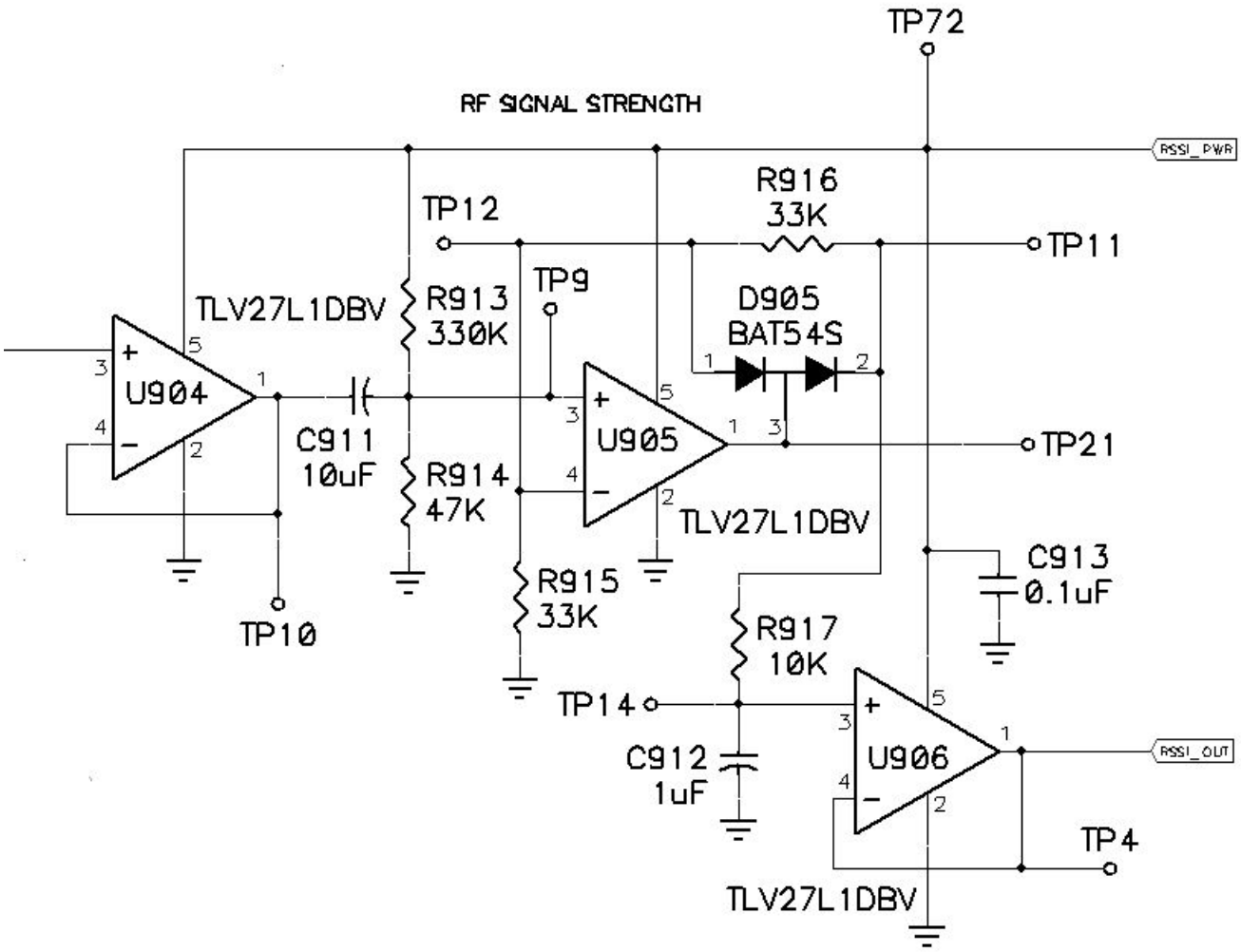


4. RSSI monitoring

The Received Signal Strength Indicator (RSSI) signal from the RF transceiver section is an analog voltage whose value represents the relative strength of any RF carrier that is detected within the frequency band of the radio. This signal must be qualified through firmware by confirming the presence of a valid packet preamble.

U904 is used as a buffer to isolate the RSSI monitoring circuit from the high-impedance RF transceiver baseband signal (U902-pin5). The buffered output is fed to a full-wave rectifier section comprised of U905, D905, R916 and R915 through capacitor C911. The full-wave rectified output of U905 is filtered by R917 and C912, and buffered by U906. The output of U906 (RSSI_OUT) is the RSSI signal that is monitored by the microcontroller through the onboard analog-to-digital converter.

The RSSI monitoring circuit has such low power-supply requirements (< 1mA) that it is powered by an output pin of the microcontroller (RSSI_PWR). This allows the RSSI monitoring circuit to be easily shut down, as needed, by the firmware.

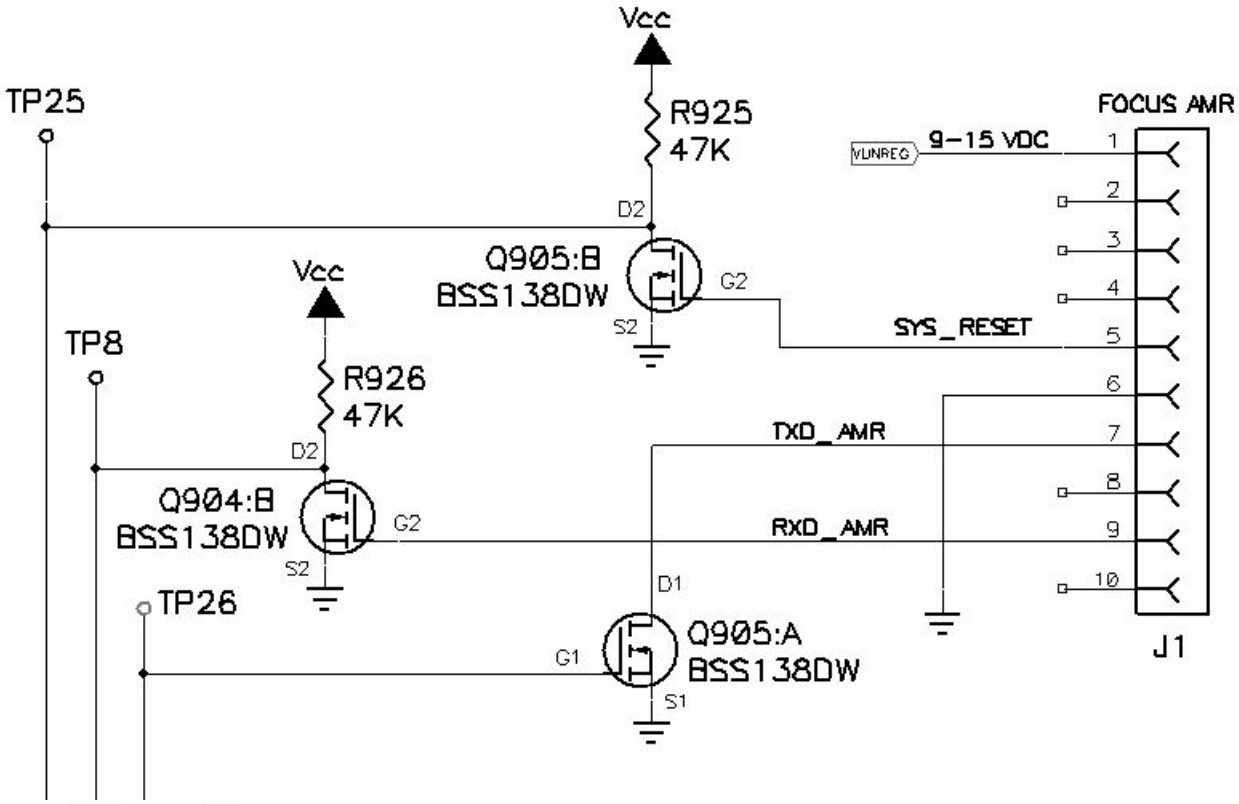


5. Serial I/O and interfacing

These circuits are the serial (RS232 and TTL) I/O components for the FOCUS AMR communication ports. They consist of the firmware-implemented UART with buffered I/O, the hardware UART internal to the microcontroller, and RS232 interface/level translation and protection circuits.

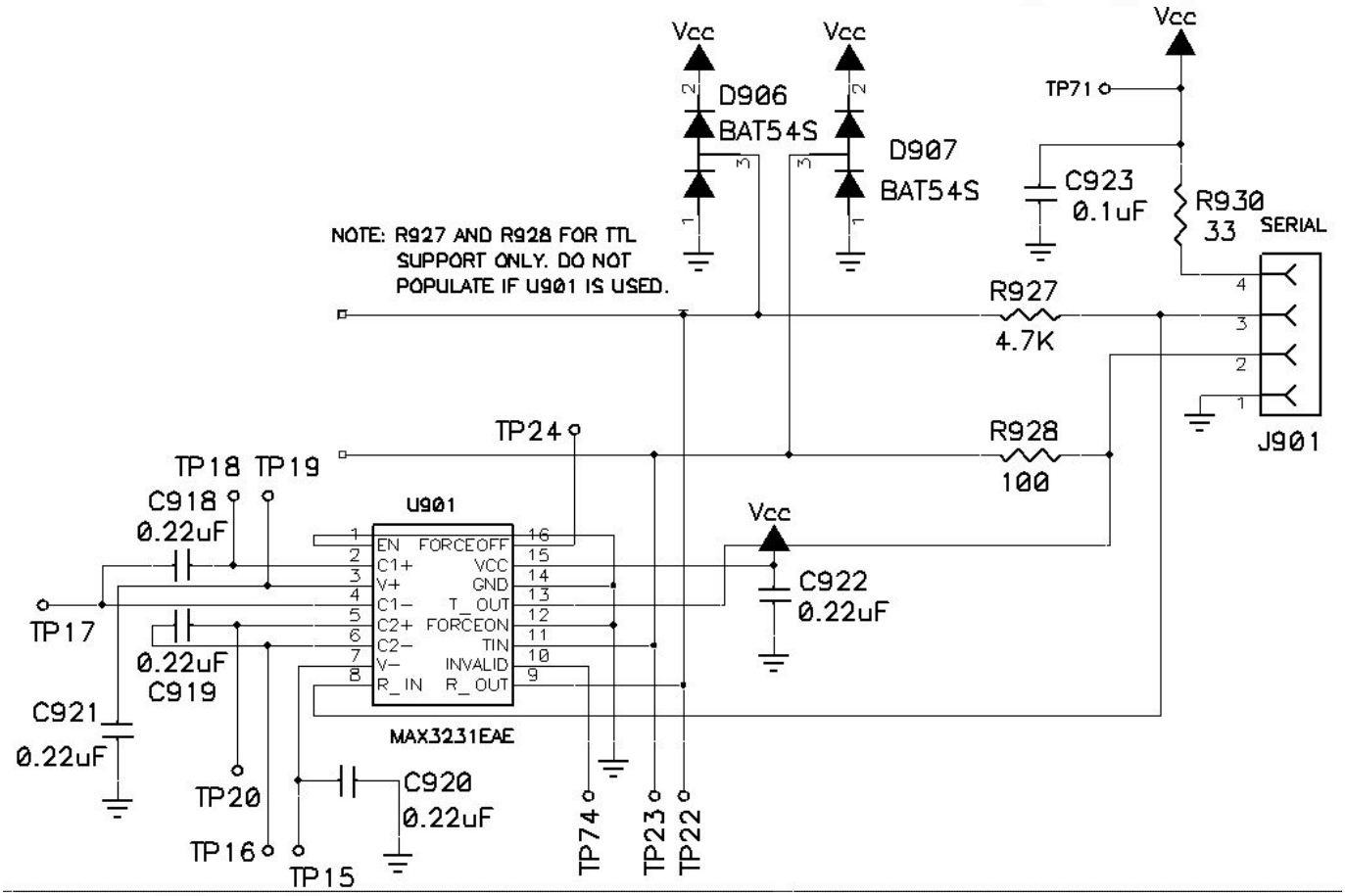
The firmware UART signals are brought out to connector J1 through MOSFET transistors Q904B and Q905A. These transistors invert the serial transmit and receive signals and perform the required level shifting between voltages present on the FOCUS AMR section and the FOCUS metrology section. They also provide the required isolation during a power-outage condition, when the AMR section continues to operate for an extended period using backup power while the metrology section remains powered down.

The metrology SYS_RESET signal at J1 is also buffered and made available for monitoring by the microcontroller firmware.



5.1 Serial/RS232 level translation

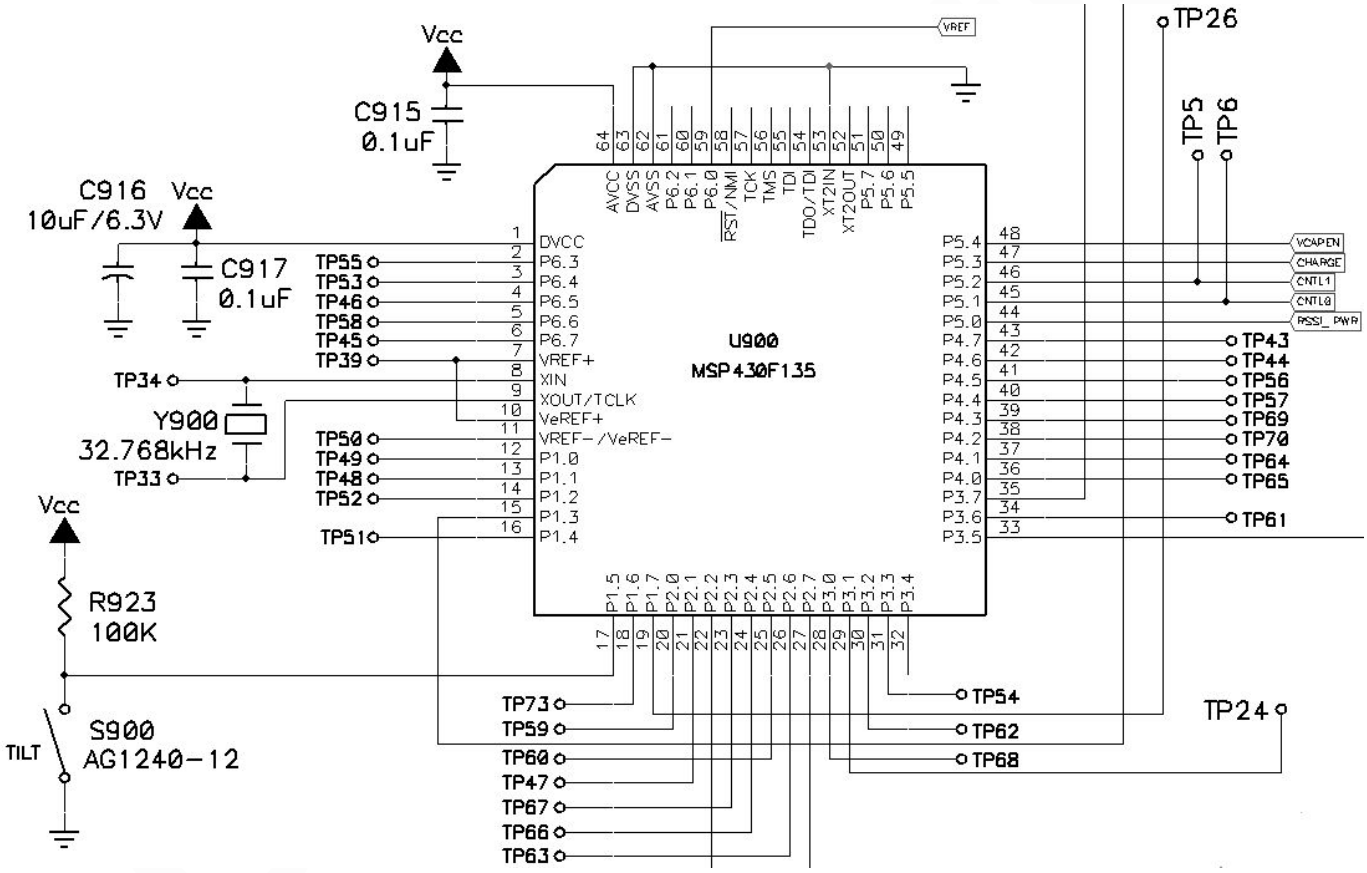
The hardware UART signals are brought out to connector J901 through resistors R927 and R928 and allow TTL level communication. If RS232 level communication is needed, these resistors are not installed and interface/level translation components are populated instead. This level translation between TTL and RS232 voltage levels is performed by a MAX3231 (U901). Diodes D906 and D907 are used as protection components so that signal levels above Vcc and lower than ground (0V) cannot damage components on the FOCUS AMR section. To allow for auxiliary power requirements of certain peripheral devices, 3 volts DC is also made available at connector J901. The supply current at this pin should be limited to less than 5 milliamps.



6. Microcontroller

This microcontroller is the heart of the FOCUS AMR section and is responsible for the overall operation. The features of the Texas Instruments MSP430F135 (or MSP430F148) microcontroller relevant to the design are:

- Asynchronous Serial Communication Interface (USART)
- Forty-eight programmable I/O (PIO) pins
- 512/2048 byte SRAM memory and 16/48 Kbyte Flash memory space
- Low supply-voltage range (1.8V to 3.6V) and ultralow-power consumption
- 12-bit A/D converter with internal reference, sample-and-hold and autoscan feature



The microcontroller operates using a single, low cost, 32 KHz watch crystal (Y900). This low-speed oscillator is typically used as a reference for internal timers and RTC operation. The main system/instruction clock is generated using an internal DCO (digitally controlled oscillator), which is frequency-programmable up to 8 MHz through the firmware. In order to maintain greater accuracy in the DCO over temperature and operating voltage, the DCO frequency can be trimmed periodically by the firmware using the 32 KHz oscillator as a stable reference.

To aid in functional testing of the board, the buffered 32 KHz oscillator clock can also be made available externally, through firmware configuration, on any of several I/O pins. Test points have also been provided for all unused I/O pins on the microcontroller.

Tamper sensing is provided using a non-mercury tip-over switch S900. This switch is normally open in the vertical position, and closes when the switch body rotates more than 30 degrees from vertical in any direction.

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7. PCB Layout Recommendations

1) The FOCUS AMR section will be composed of a 4-layer, FR4 material, one ounce copper PCB. The top and bottom layers of the PCB will be used as signal layers and the inner two layers will consist of a ground plane and power plane (3V, Vcc plane).

2) All the components will be mounted only on the top-side of the board, which will be silk-screened and solder-masked. The bottom side of the board does not need silk-screening.

3) An attempt should be made to keep the following trace lengths to a minimum:

   - The traces related to the crystal oscillator section on U900, which pertains to the following components: Y900, and pins 8 and 9 on U900 should be kept as short as possible.

   - As a general guideline, all the power supply de-coupling capacitors for the various IC's (C915, C916, etc.) should be placed as close as possible to the power supply pins on the IC's they are connected to, and trace lengths to power and ground should be kept as short as possible.

4) Special attention should be paid to the placement of RF components, including the antenna. All passive components required for RF transceiver operation should be placed as close as possible to the pins they are connected to, keeping trace lengths to a minimum. All connections to power and ground planes should be short, low inductance traces. Manufacturer recommended power-supply decoupling components should be used.

   Where possible, a minimum clearance of 0.25 inches from the PCB antenna to power and ground planes should be maintained, as well as to components, vias and traces. The antenna feed from the RF transceiver should be kept as short as possible, with minimum trace lengths connecting impedance-matching network components L900, L901, C909 and C910.

   Refer to the RF Monolithics *TR-1000 Data Sheet*, and *ASH Transceiver Designer's Guide* for more information.

5) To allow for In-Circuit Testing (ICT) using a "bed-of-nails" fixture, a pad/via/test point should be brought to the bottom of the board for all the nodes present in the design, excluding the RF section, allowing 100% ICT coverage. Each of these test points should have a diameter of 35-40 mils and a minimum center to center spacing of 100 mils.

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8. Firmware

The FOCUS AMR section firmware running in the MSP430F135 (or MSP430F148) microcontroller has four distinct memory areas associated with it:

- *SRAM area*: the SRAM area is used to store frequently modified data and variables, which includes the data buffers and stack space. The SRAM area is volatile and its contents are lost when the microcontroller is powered off.
- *Data Flash area*: the data Flash area is used to store data and variables that are not modified very often. Data stored in the Data Flash area is non-volatile and its contents are preserved even when the microcontroller is powered off.
- *Code Flash area*: the code Flash area is split in two halves, with only one half being active at any one time. The microcontroller runs the code stored in the active half. When new firmware is downloaded via RF, the new code image is first downloaded to the inactive code Flash area. After the downloaded image is validated, it is marked active and the currently active code Flash area is marked inactive. On subsequent restart of the system, the new code image is executed. The code Flash area is non-volatile and its contents are preserved even when the microcontroller is powered off.
- *Special Function Register (SFR) area*: the SFR area consists of memory locations within the memory map that controls the peripherals within the microcontroller. These registers include the 8-bit (e.g. USART) and 16-bit peripherals (e.g. TimerA) implemented within the microcontroller. The contents of these registers are not preserved when the microcontroller is powered off.

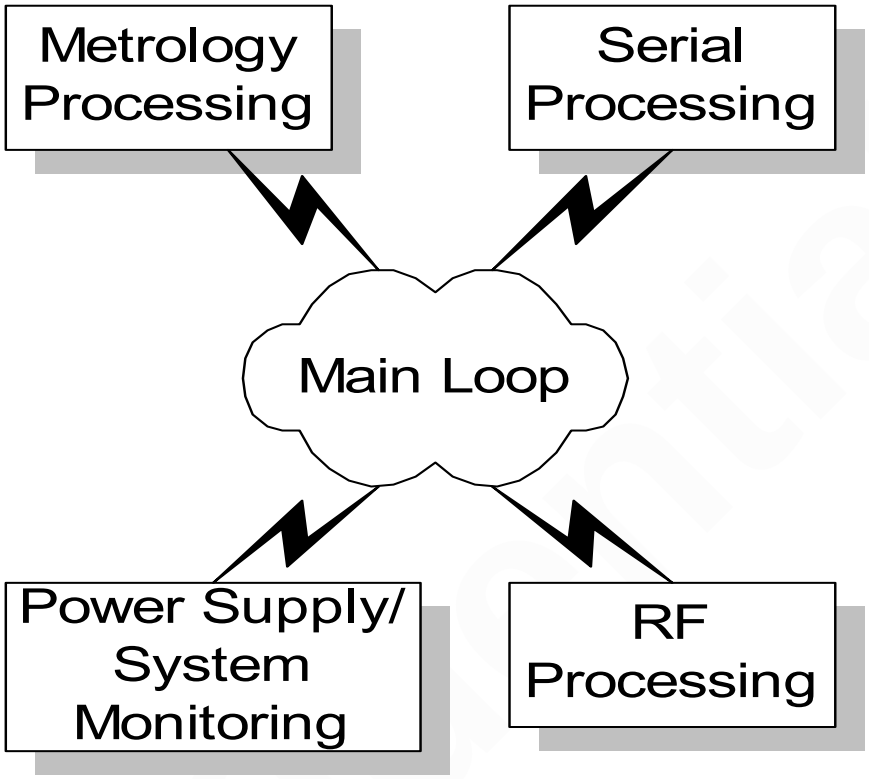
The memory map of the firmware is shown in the figure below:

Code Flash area #1	0xE000 - 0xFFFF (8192 bytes)
Code Flash area #2	0xC000 - 0xDFFF (8192 bytes)
Unimplemented	0x1100 - 0xBFFF (44800 bytes)
Data Flash area	0x1000 - 0x10FF (256 bytes)
Unimplemented	0x0400 - 0x0FFF (3072 bytes)
SRAM area	0x0200 - 0x03FF (512 bytes)
SFR area	0x0000 - 0x01FF (512 bytes)

The firmware consists of the following major functional blocks:

a) Metrology Processing
b) Serial Processing
c) Power supply/system monitoring
d) RF processing
e) Main processing loop that is basically just an endless loop that calls each of the blocks listed above in turn.

In addition, there are a few smaller firmware blocks that handle (re)programming of the onboard Flash memory and system initialization.



8.1 Metrology Processing

The metrology processing block handles all aspects of serial data communication between the FOCUS AMR section on connector J1 and the FOCUS metrology section. It establishes sessions with the metrology section in accordance with the ANSI C12.18 protocol and allows reading and writing of the standard ANSI tables stored in the metrology section. The standard consumption reading table (table # 23) is read on a periodic basis to maintain a history of consumption data, but requests to read or write all other ANSI tables are initiated by the host via the RF network. The lower sixteen bits (two bytes) of the negative watt-hour count returned by the metrology section when table 23 is read is stored in the firmware. On subsequent reads of table 23, the new negative watt-hour count is compared with the previously stored value and a change in this value indicates a reverse flow error condition. This error condition is recorded by the firmware and the host can query for any such errors via the RF network.

The following ANSI C12.18 commands are used for communication: IDENTIFY, LOGON, SECURITY, TABLEREAD and TERMINATE. The SECURITY command uses an initial default password of "95661252". This password is stored in the Data Flash section of the firmware and can be changed via the RF network by the host.

If a table read or write needs to be executed by the host, it will need to send the complete TABLEREAD or TABLEWRITE data bytes as part of command 20 sub-function 1. The firmware does not assign a meaning to the data bytes and does not attempt to parse the data bytes in the command, but simply establishes a new session and

transmits the data bytes to the metrology section. The firmware will send a response code and any response data bytes back to the host:

- If a response packet is received, the complete response packet received is transmitted back to the host without being parsed or interpreted. If a response is not received from the metrology section within 250 milliseconds (default value), a timeout error is returned to the host. This timeout period is stored in the Data Flash section of the firmware and can be changed via the RF network by the host.

- The response from the metrology section can be a maximum of 64 bytes, including the ANSI protocol overhead bytes. If the response exceeds this length, all the response packet bytes are discarded and a "response packet too large" error is returned back to the host.

- The firmware monitors the SYS_RESET signal output by the metrology section before transmitting any data packets. If this signal is asserted, indicating that the metrology section is not ready, transmission of the data packet is abandoned and an error reported back to the host. Retries are not implemented.

More information on the ANSI protocol and tables can be found in the ANSI C12.18, C12.19, C12.21 and the Landis+GYR implementation documents.

8.2 Serial Processing

The serial processing block handles all aspects of serial data communication between the FOCUS AMR section and the transparent data port on connector J901. If the host needs to transfer data on the transparent port, it will need to send the complete data bytes as part of command 20 sub-function 0. The firmware does not assign a meaning to the data bytes and does not attempt to parse the data bytes in the command, but simply transmits the data bytes. Any response data bytes that are received is transmitted back to the host without being interpreted or parsed. The transparent serial data port is typically used for the load control function using the BLP collar.

8.3 Power supply/system monitoring

The power supply and system monitoring block handles all aspects of monitoring the VUNREG power supply voltage, controlling the charging of the Supercapacitor backup power supply, monitoring the state of the tamper switch and controlling/adjusting the operating frequency of the microcontroller (DCO).

- The VUNREG voltage is periodically monitored by the firmware on the ADC input pin VREF. If the VUNREG voltage falls below 8.5VDC, an impending AC mains failure condition is assumed. In preparation for an orderly shutdown, the consumption data counts are saved to non-volatile Flash memory, the Supercapacitor charge circuit is disabled by deasserting the CHARGE pin and the microcontroller enters a low–power sleep mode. Switchover from the primary power source on VUNREG to the backup power source on the Supercapacitor during the AC mains failure is automatic and no firmware intervention is necessary.

- The voltage on the Supercapacitor is periodically monitored by the firmware by asserting the VCAPEN pin and measuring the voltage on the ADC input pin VCAP. If the voltage on the Supercapacitor falls below 5.5VDC, the Supercapacitor charge circuit is enabled by asserting the CHARGE pin. If the Supercapacitor voltage rises above 5.7VDC, the charge circuit is disabled by deasserting the CHARGE pin. The firmware also monitors the

SYS_RESET signal output by the FOCUS metrology section and if it is found asserted, the Supercapacitor charge circuit is turned off.

- The state of the tilt/tamper switch S900 is periodically monitored by the firmware. If the switch is found asserted, a tamper error has occurred. This error condition is recorded by the firmware and the host can query for any such errors via the RF network.

- When a power fail condition is detected by the firmware, it transmits an RF emergency power fail message. If a tamper condition is detected in addition to the power fail condition, the power fail message is sent immediately. If a tamper condition is not detected, the power fail message is sent after a random period of time. The radio transmitting the power fail message expects an acknowledgement in response. If this acknowledgement is not received, it will continue to retry transmitting the power fail message. Once an acknowledgement is received, the radio will enter a low-power sleep mode. If the radio is configured to be a repeater device, it will forward all RF messages it receives to the site controller, even during a power fail condition, until the charge on the Supercapacitor is no longer enough to power the radio. The holdup time on the Supercapacitor depends on the amount of RF traffic and can last up to eight minutes. If the radio is not configured to be a repeater device, the holdup time on the Supercapacitor can last up to several hours in sleep mode.

- The basic clock module is configured to oscillate with a low-power 32786Hz external watch crystal providing a stable time base for the system and low power stand-by operation. The system clock SMCLK is configured to operate at 2MHz from the digital controlled oscillator (DCO). The DCO is an integrated ring oscillator with RC-type characteristics whose frequency varies with temperature, voltage, and from microcontroller device to microcontroller device. The DCO frequency is adjusted by the firmware periodically to operate at a stable 2MHz frequency despite its RC-type characteristics.

8.4 RF processing

The RF processing block handles all aspects of communicating with RFM radio chip and handling the transmission and reception of the RF packets. The RF packets are Manchester encoded at 4800 bits per second, yielding a 2400 bps message bit rate. The RF packets are a minimum of 14 bytes and a maximum of 128 bytes, prior to Manchester encoding.

When the FOCUS radio is powered up, the firmware goes through a self-initialization sequence where it attempts to "register" itself in the RF network. As part of this self-initialization sequence, it transmits a beacon every five minutes or so indicating to other radios that may be present in the network that a new radio has come alive. Other radios that hear this beacon from the newly powered radio respond to the new radio. The new radio then builds a list of radios that it can communicate with and forwards this list to the site controller. The site controller decides the optimal RF paths for the radios and instructs the radios as to the RF paths they need to take for communication.

Provisions have been made in the firmware so that it is possible to download new firmware via the RF network to the FOCUS radios and then have the radios switch over to the new firmware version. This allows upgradability after the radios have been installed in the field without physical intervention.

More information on the RF protocol can be found in the Statsignal “SOS OEA RF Packet Message Protocol” document, #9000075.