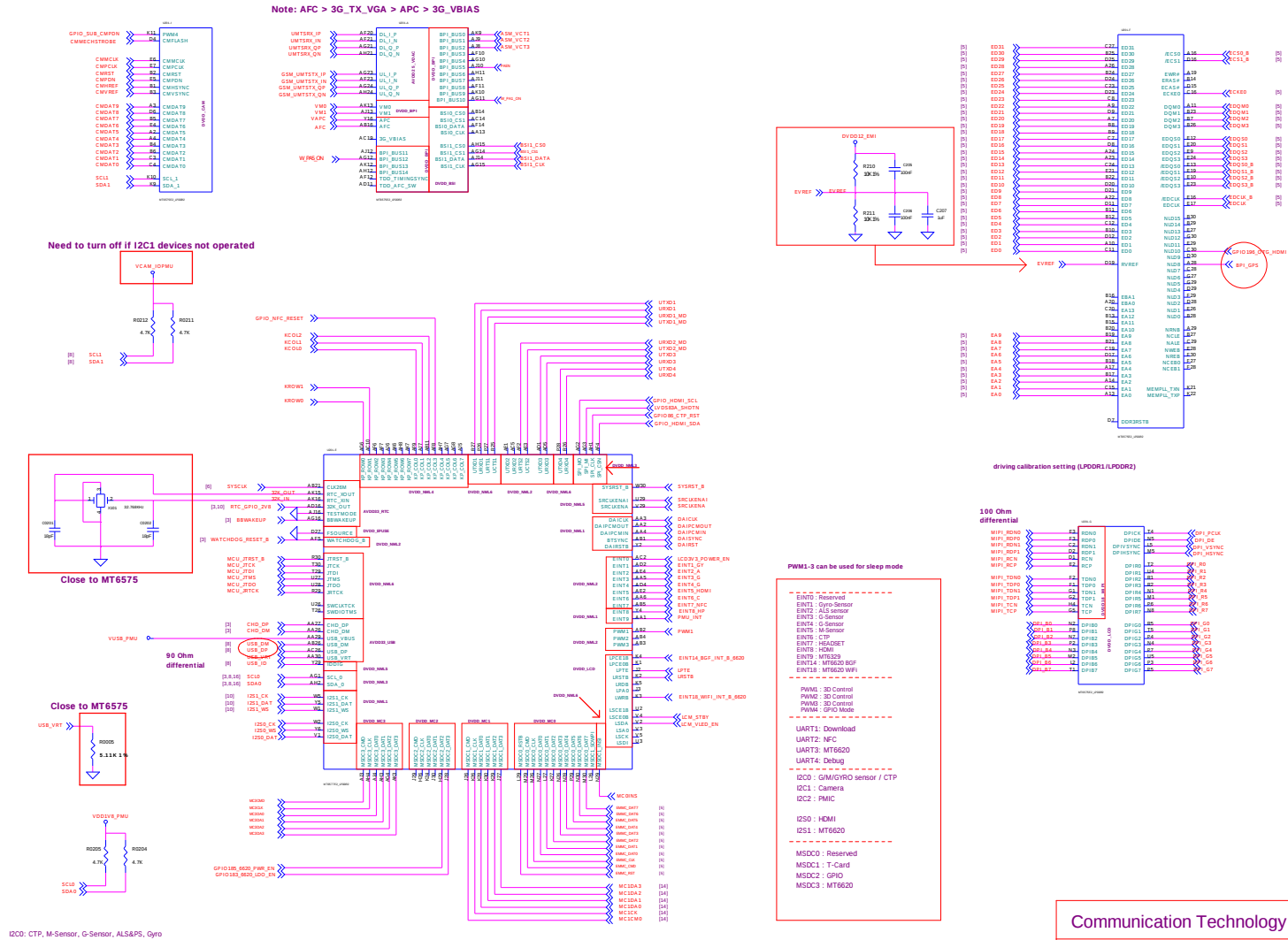
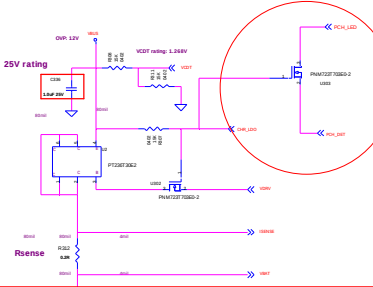


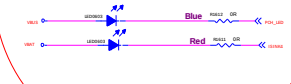


1. Close to Battery Connector.
(Rense (R312) < 10mm)
2. Main path should be 40mil.
(VBUS -> U2011's E -> U2012's C -> R312 -> VBAT)
3. Star connection from R312 to BAT Connector

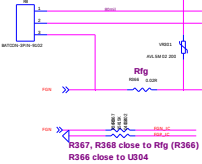
Charger



Indicator LED



BATTERY CONNECTOR



MP Test Points



Add Zener Diode
Place on the path
from VBAT to IC
(Battery connector
or test point or IO
connector)
500mW



Between IC and IO port



Keep at least 1
VIA1-2 each ball



Separate SIO1/2 and SCLK1/2
SIO1/SCLK trace 6mil



Close to MT6575



Close to MT6575



Close to MT6575



Close to MT6575



Close to MT6575



Close to MT6575



Close to MT6575



150mV/0.5mV 4mil
differential to Rense



Direct to main GND



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball

TVOUT trace:
W=8mil, S=6mil,
GND>20mil with GND vias



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



Keep at least 1
VIA1-2 each ball



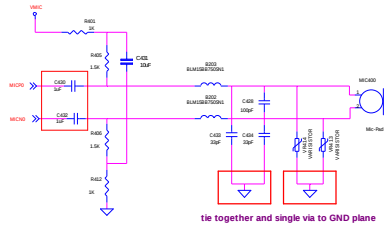
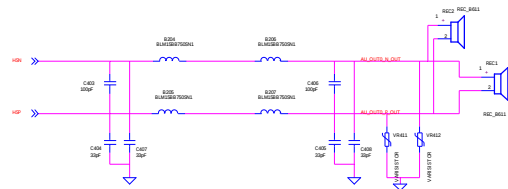
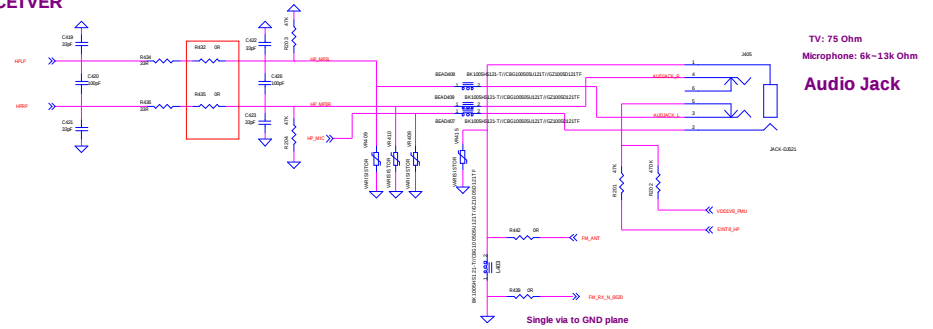
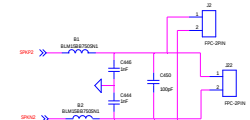
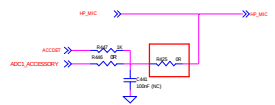
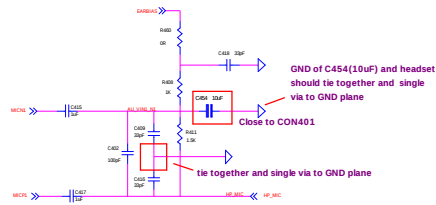
Keep at least 1
VIA1-2 each ball

	Symbol	Vout (V)	Iout (mA)
Buck	VPA	0.0 - 3.4 (10mV/step)	800
	VPROC	0.75 - 1.3 (25mV/step)	1500
	VRFB	1.025	250
	VCORE	0.75 - 1.3 (25mV/step)	1000
	VIOLB	1.0	1000
Analog	VRFB	2.85	200
	VICOD	2.8	300
	VCAMA	1.0/1.2/2.0/2.8	200
	VA1	1.0/1.2/2.0/2.8	100
	VA2	2.0/2.8	100
Digital	VM12_1	1.2	300
	VM12_2	1.2	300
	VM12_INT	1.2	300
	VIOZB	2.8	100
	VISAL	1.0/1.2	100
Vibrator	VISM2	1.0/1.2/1.8/2.0/2.8/3.0/3.3	100
	VUSB	3.3	100
	VCAMD	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	300
	VCAM_IO	1.3/1.5/1.8/2.0/2.8/3.0/3.3	100
	VCAM_AIT	1.3/1.5/1.8/2.0/2.8/3.0/3.3	200
RTC	VMC	1.3/1.5/1.8/2.0/2.8/3.0/3.3	200
	VMCH	1.3/1.5/1.8/2.0/2.8/3.0/3.3	400
	VGP	1.3/1.5/1.8/2.0/2.8/3.0/3.3	100
	VOP1	1.3/1.5/1.8/2.0/2.8/3.0/3.3	100
	VOP2	1.3/1.5/1.8/2.0/2.8/3.0/3.3	200
RTC	VRTC	1.0/1.2/2.0/2.8	2

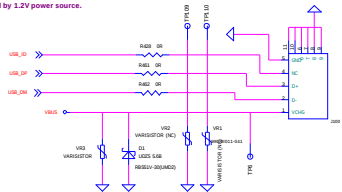
Communication Technology Co., Ltd

TITLE:

MODEL: MT6577	CODE:	DRAWN: ZOUIS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 3 OF 15	APPROVED:	DATED:

[illegible][illegible][illegible][illegible][illegible]

If mini-A connector insert => CID < 0V => Low
If mini-B connector insert => CID > 1.2V => High
IDPULLUP pin is replaced by 1.2V power source.



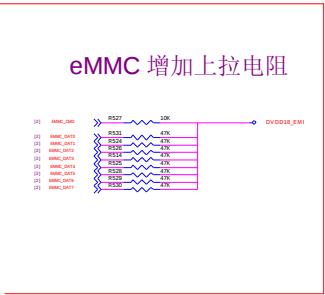
Communication Technology Co.,Ltd			
TITLE: AUDIO_USB			
MODEL:MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 4 OF 11	APPROVED:	DATED:

eMMC 增加上拉电阻

Diagram illustrating the connection of eMMC pins to a pull-up resistor network. The pins are connected to a common bus, and the resistor values are indicated as 10K.

Pin connections and resistor values:

- DQ0-DQ15: 10K
- DQ16-DQ31: 10K
- DQ32-DQ47: 10K
- DQ48-DQ63: 10K



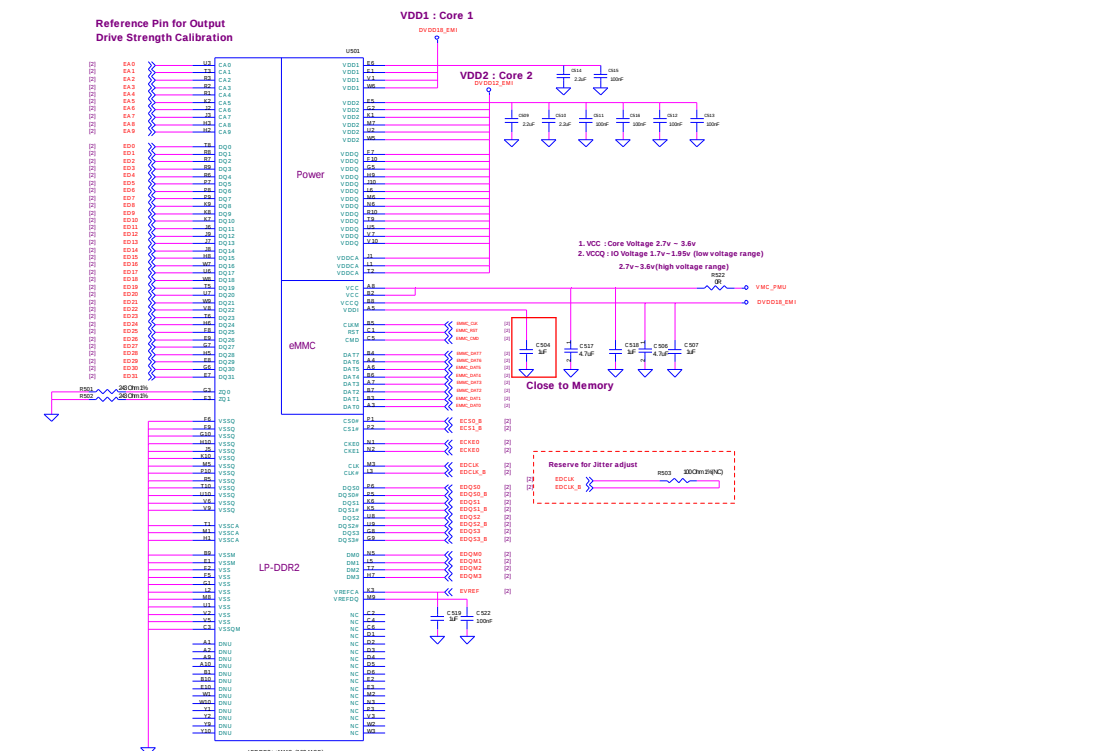
MCP

S48 VDD1=1.8V,VDD2=1.20V,VDDCA ,VDDQ= 1.20V

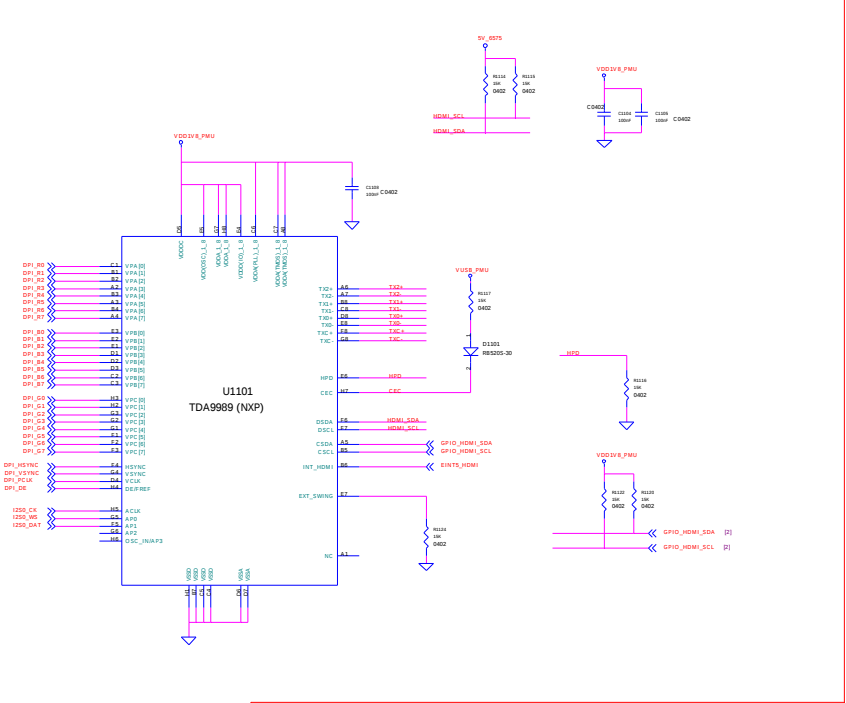
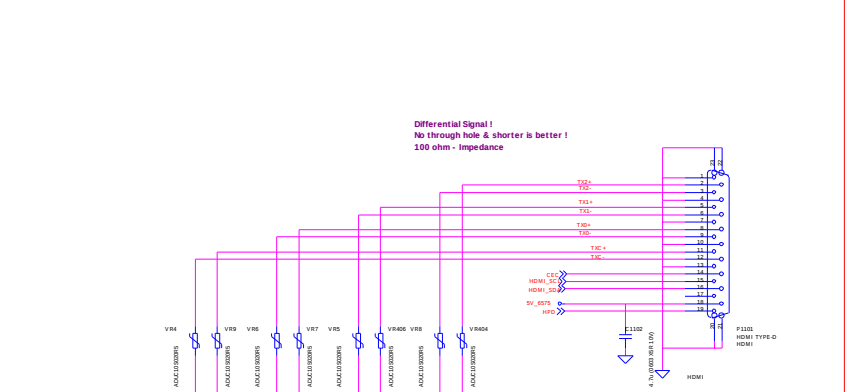
The timing diagram shows two signals over time:

- VDD1 : Core 1**: A purple signal that transitions from low to high at approximately 0.8 ns.
- Reference Pin for Output Drive Strength Calibration**: A blue signal that starts at 0V, rises to about 1.6V at 0.8 ns, and then settles around 1.7V after 1.2 ns.

Key time points are marked on the x-axis: 0.8 ns, 1.2 ns, and 1.6 ns.



The schematic illustrates a differential signal connection between two printed circuit boards (PCBs). On the left, a series of eight vias connect pads labeled V8A through V8H to corresponding pads on the right, labeled V8B through V8H. The top four pairs of pads are connected to a common ground plane (GND) via vias. The bottom four pairs of pads are connected to a common ground plane (GND) via vias. The signal traces are color-coded: red for TX+, blue for TX-, green for RX+, and yellow for RX-. A 100 ohm impedance is indicated for the signal traces. The ground plane is labeled GND. A note specifies "Differential Signal ! No through hole & shorter is better ! 100 ohm - impedance".

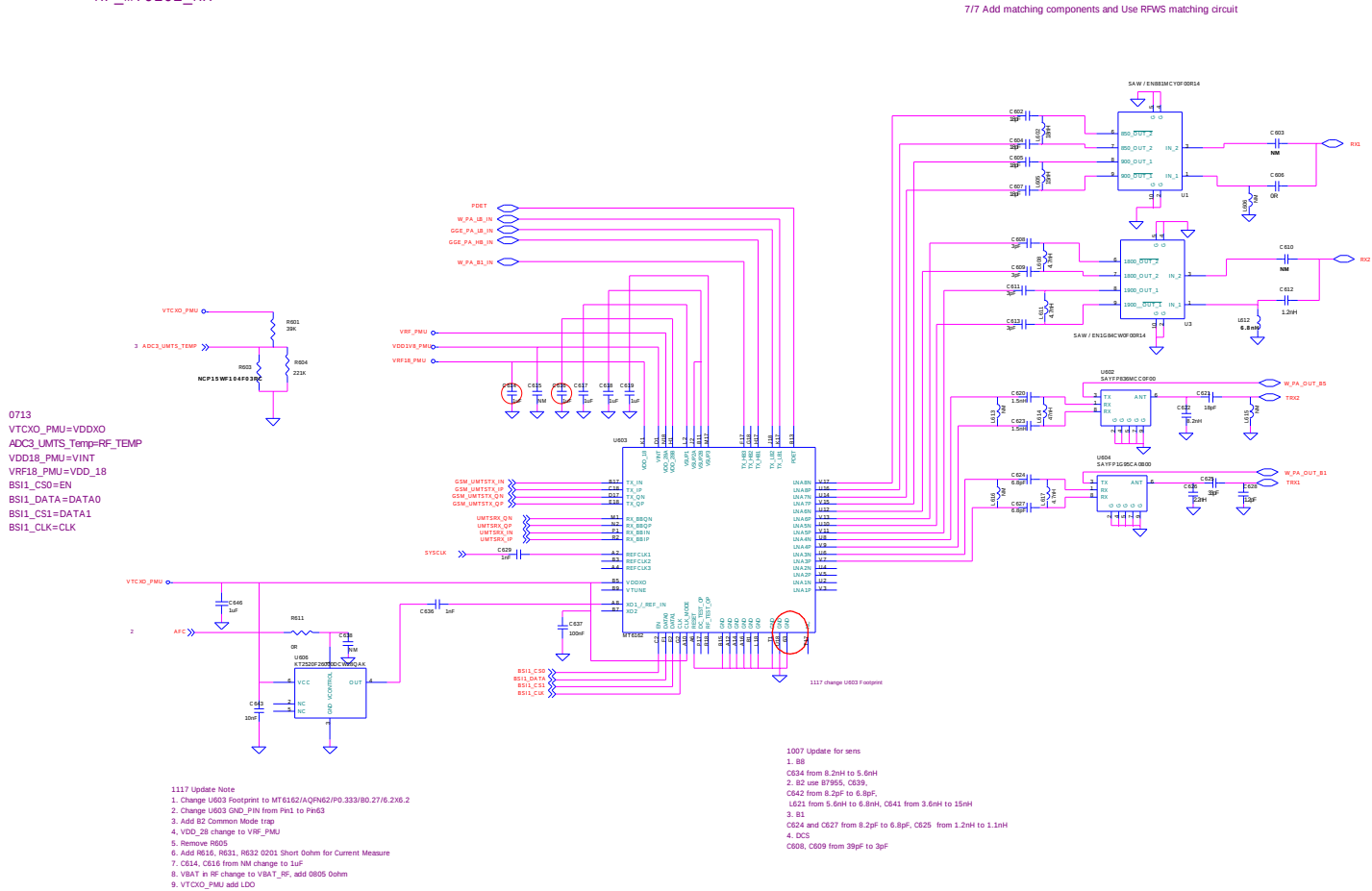


Communication Technology Co.,Ltd

TITLE:	05 Memory (eMMC + x32LPDDR2)		

MODEL: MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 5 OF 11	APPROVED:	DATED:

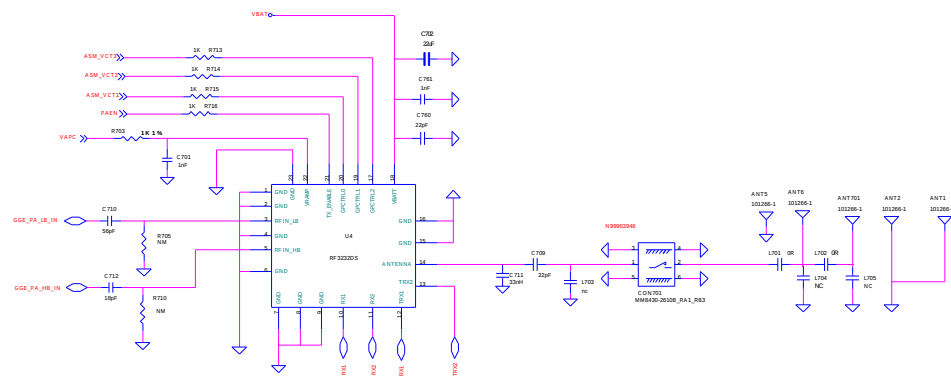
RF_MT6162_RX



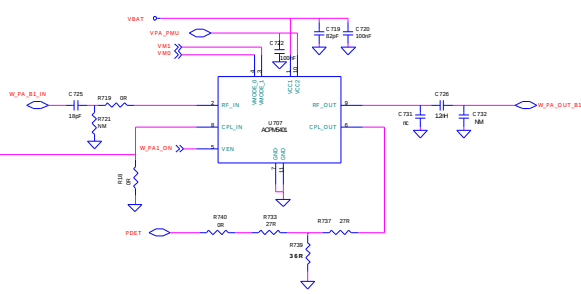
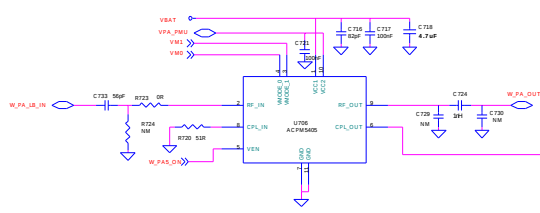
Communication Technology Co.,Ltd

TITLE: RF_MT6162_RX

MODEL:MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 6 OF 11	APPROVED:	DATED:



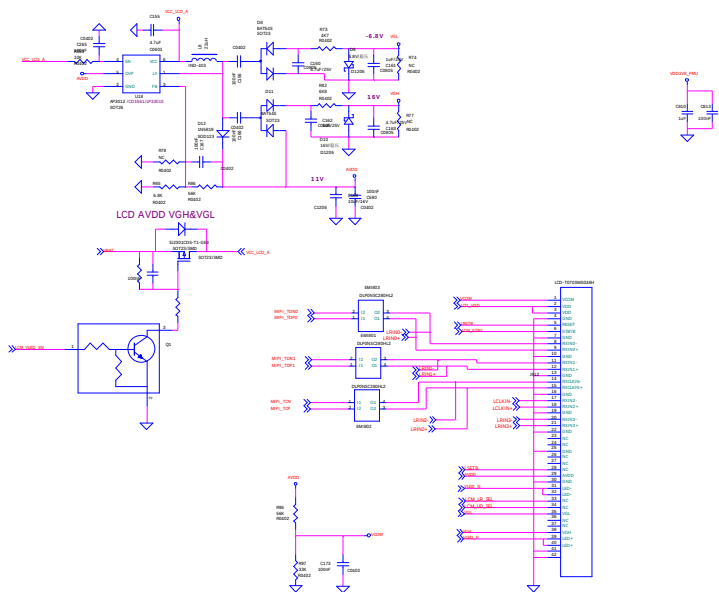
RF3232DS Control Truth Table				
	TX_EN	Vct2	Vct1	Vct0
Standby	0	0	0	0
RX1	0	1	0	0
RX2	0	0	1	0
TRX1	0	0	1	1
TRX2	0	0	0	1
LOW BAND	1	0	1	0
HIGH BAND	1	0	1	1



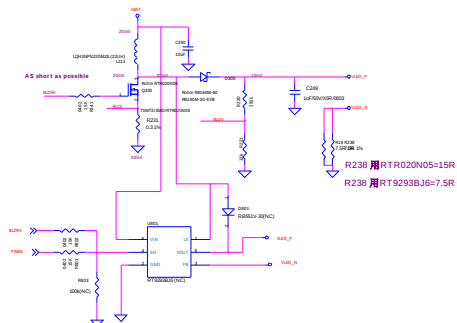
0713 Update Net Name
 ADCS_UMTS_POWER =GGE_PA_VDET
 EDGE_MODE =GGE_PA_MODE
 ADCS_UMTS_POWER =GGE_PA_VDET
 VAPC =GGE_PA_VRAM
 BANDSW =GGE_PA_BS
 PAEN =GGE_PA_ENABLE

 VM1 =-W_PA_VMODE1
 VM0 =-W_PA_VMODE0
 W_PA5_ON =-W_PA_BS_EN
 W_PA3_ON =-W_PA_BS_EN
 W_PA1_ON =-W_PA_BS_EN
 W_PA2_ON =-W_PA_BS_EN

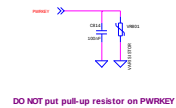
Communication Technology Co.,Ltd			
TITLE: RF_TX_ASM			
MODEL:MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 7 OF 11	APPROVED:	DATED:



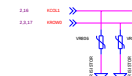
BACKLIGHT DRIVER



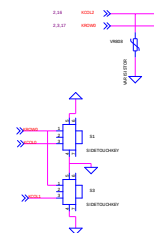
Power Key



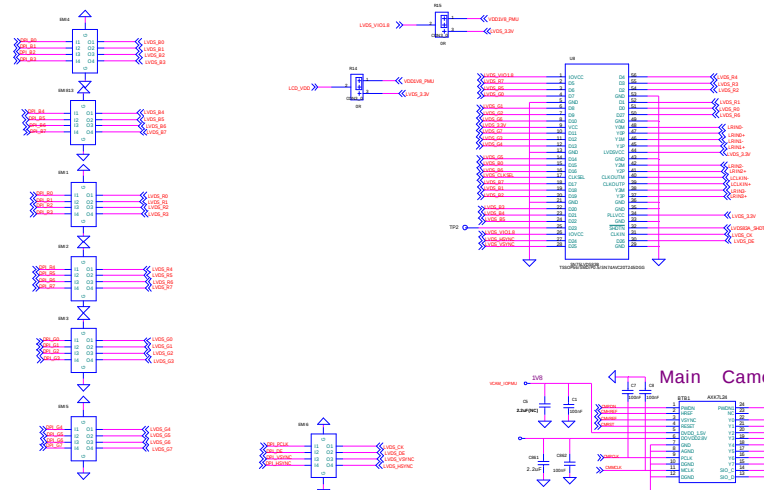
Volume Up



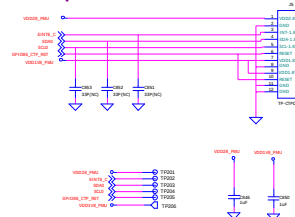
Volume Down



	POWER	LOCK	HOME	BACK	APP	SEARCH
CTP_1	1	2	3	4	5	6
CTP_2	7	8	9	10	11	12
CTP_3	13	14	15	16	17	18
CTP_4	19	20	21	22	23	24
CTP_5	25	26	27	28	29	30



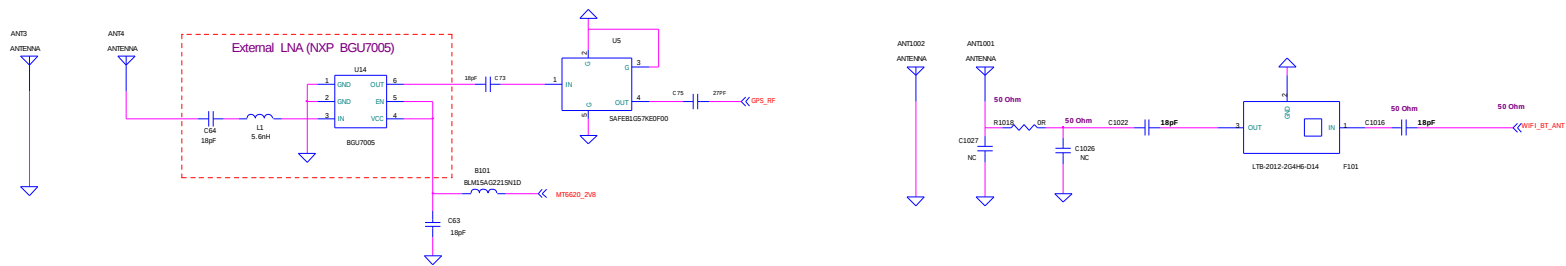
Capacitive Touch Panel



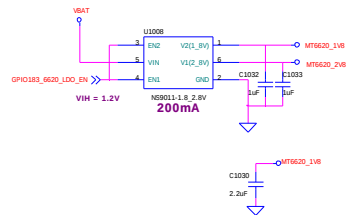
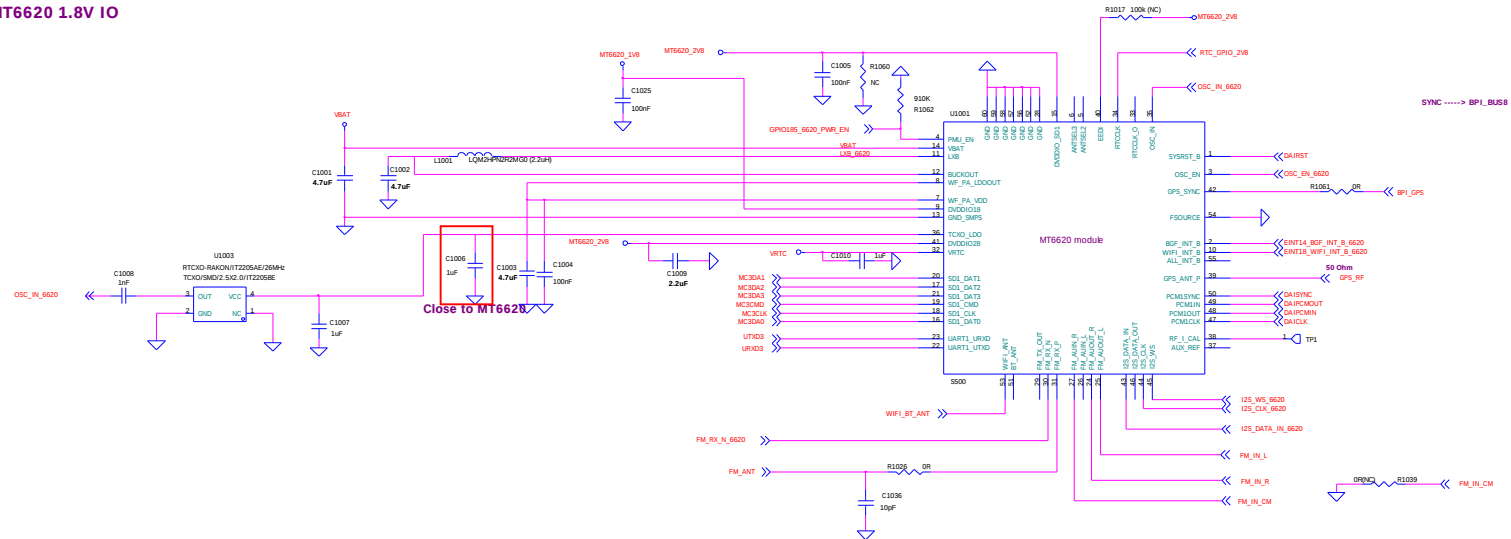
Communication Technology Co.,Ltd

TITLE: LCD_CTP_CAMERA

MODEL:MT6577	CODE:	DRAWN: ZOUS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 8 OF 11	APPROVED:	DATED:



MT6620 1.8V IO



	XTEST	FED1	ANTSEL_3	
clock setting	2.8V TCXO or OSC	0	0	Default
	1.8V TCXO or OSC	0	1	0
	XTAL	0	0	1
	external clock mode	0	1	1

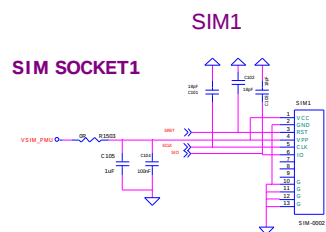
	XTEST	ANTSEL_2	ANTSEL_1	
WiFi host interface	WiFi-SIO1	0	0	Default
	WiFi-SIO2	0	0	1
	WiFi-SPI	0	1	0
	WiFi_reserved	0	1	1

	XTEST	ANTSEL_0	
BT/common host interface	UART1	0	Default
	SDIO2	0	1

Communication Technology Co.,Ltd

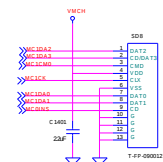
TITLE: MT6620_BT_FM_GPS_WIFI

MODEL: MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 9 OF 11	APPROVED:	DATED:



MSDC1

SD CARD



CD:
H: Card remove
L: Card insert

Communication Technology Co.,Ltd

TITLE: SIM& TF

MODEL:MT6577	CODE:	DRAWN: ZOUJS	DATED:
TITLE: SCHEMATIC	REV: A0	CHECKED:	DATED:
SIZE: A4	SHEET: 11 OF 11	APPROVED:	DATED:

