Technical Theory

Controller Circuit Descriptions

The controller section consists of the following main functional blocks(see Figure 2-1)

- **Functional Controller (U25)**
- **Message Storage (U24)**
- **Primary Code Storage (U23)**
- **Power Management (U304)**
- **Display Module**
- **Backlighting (U3)**
- **Serial Interface (U28)**
- **Audio (U31)**

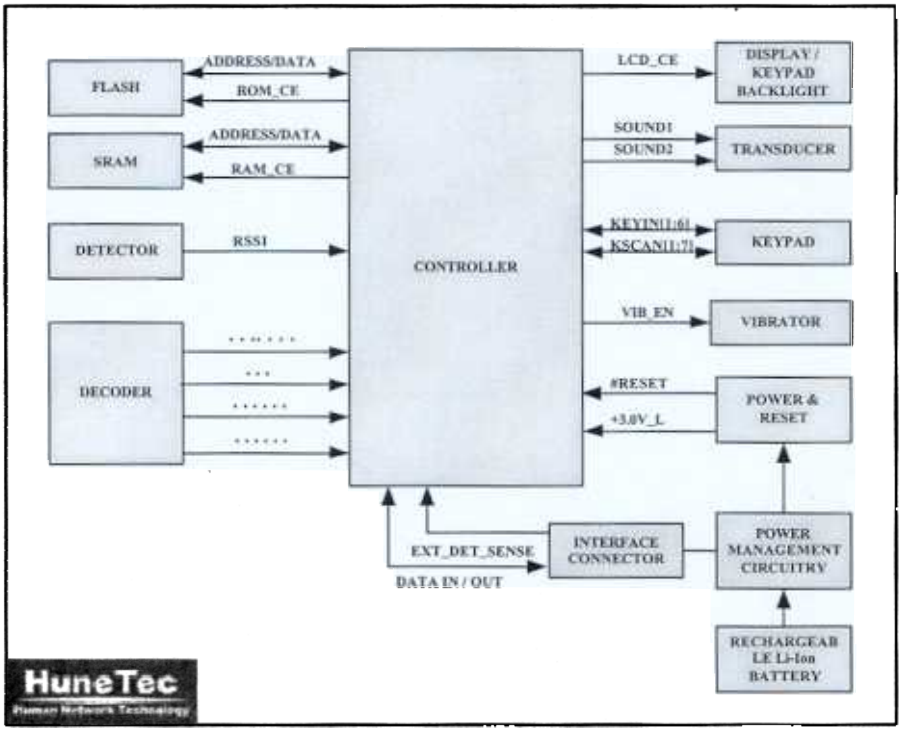

Figure 2-1. Controller Functional Block Diagram

1. Functional Controller

The functional controller (U25) provides user interface of the unit. The functional controller affects the following components:

Display Module

Message storage (U24)

Primary Code Storage (U23)

Decoder (U26)

Alert generators (vibrator at U17; transducer at U30)

Display (U7) and Keypad Backlight

Serial communication (U28)

- Primary code storage (U23)

2. Digital Signal Processor

The digital signal processor (U14) is responsible for the decoding received information.

3. Message Storage

The message storage IC (U24) is a 4M bit SRAM (Static Random Access Memory) contained in a 44-pin package

4. Primary Code Storage

The primary code storage IC (U23) is a 16-megabit flash memory IC contained in a 48-pin package.

5. Power Management

After Battery voltage is authorized, voltage is authorized to internal LDO Regulator (U13, U18, U410, U411, U412) and Reset generator through V_{IN} of Power & reset IC (U304). CPU is initialized through Reset signal which is input to CPU as Reset IN. Output power V_{out}(+3V) for Power & reset IC is used for Logic such as Digital Part of Audio IC and CPU. Output power V_{out} (+3V) for External Regulator is used for Analog part of Audio IC and VCTCXO, PLL of Transceiver. Regulator is used for authorization for regular voltage of EL through Battery voltage.

6. Display Module

The display driver is a flex circuit that drives Lines by 24 characters display. This circuit attaches to the controller at contacts display module. The functional controller (U25) provides sole control over the driver.

The display driver has an internal voltage triple that generates the appropriate voltage levels needed to drive the display glass.

7. Backlight

The backlight consists of the following elements:

- Electro-Luminescent (EL) panels
- An EL driver (U3)
- EL contacts

When active, the EL panel draws approximately 90 volts peak-to-peak (200Hz) from the driver.

8. Serial Port Interface

The serial port interface provides a connection between the HRD-100 communicator and programming fixture.

9. AUDIO

Audio IC (U31) is a mono bridged audio power amplifier with DC voltage volume control.

Transceiver Circuit Descriptions

Specifications

1. Receiver

Item	Specification
Frequency	929~932MHz, 935~942MHz
Channel Spacing	12.5KHz / 10KHz
Bit Rate	1600~9600bps
Signaling Modulation	2 or 4 Level FSK
Frequency Deviation	800Hz and 2400Hz
Receiver Sensitivity	20uV/M with 80 char(TBD)
Frequency Accuracy	1ppm
Adjacent Channel Rejection	> 50dB from Sensitivity to -80dBm > 40dB at -70dB Signal Level > 30dB at -60dB Signal Level
Co-Channel Rejection	< 15dB at -105dBm < 10dB at -102dBm < 6dB at -95dBm
Spurious Response Rejection	> 55dB at -105dBm
Image Rejection	> 55dB at -105dBm
Inter-Modulation Distortion Rejection	> 50dB from Sensitivity to -80dBm > 40dB at -70dB Signal Level > 30dB at -60dB Signal Level
Simulcast Delay Spread Tolerance	> 1/4 symbol width at -105dBm and 15dB C/I > 1/4 Symbol width at -102dBm and 10dB C/I > 1/4 Symbol width at -55dBm and 6dB C/I

2. Transmitter

Item	Specification
Frequency Range	896~902MHz

Channel Spacing	12.5KHz/10KHz
Bit Rate	800~9600bps
Signaling Modulation	4Level FSK
Frequency Deviation	800Hz and 2400Hz
Frequency Accuracy	-2.5ppm < X < 2.5ppm
Frequency Stability	-1.0ppm < X < 1.0ppm
Output Power	0.75W into Antenna
ERP	0.2W minimum over 8 positions
Spurious Emission In-Band/Out-Band	< -50dB
Occupied Bandwidth	8.5KHz

Circuit Descriptions

The following information describes the circuitry specific to HRD-100 pagers with 900MHz transceivers. See Figure 3-1

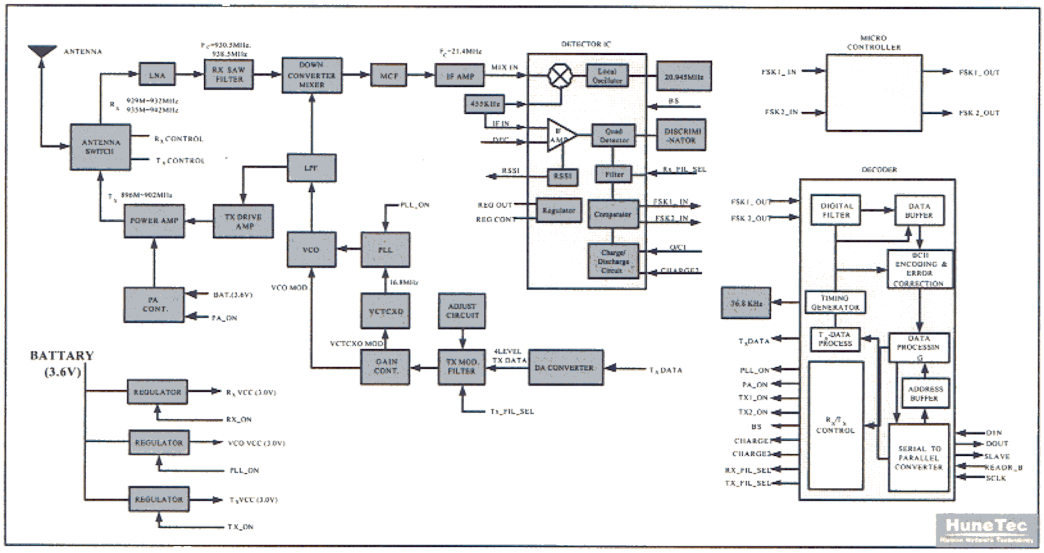

Figure 3-1 Transceiver Functional Block Diagram

The transceiver board consis ts of the following major component sections:

- # Antenna (ANT1)
- # Antenna Switch (U102)
- # Receiver Automatic Gain Control Circuit
- # Low Noise Amplifier (U8)
- # Receiver Surface Acoustic Wave Filter (U2)
- # Receiver First Mixer (U104)
- # Crystal Filter for First IF (MCF1)
- # IF Detector IC (U12)

Decoder (U26)

Operational Amplifier (U9, U19)

Transmit VCO/ Receiver First LO VCO (VCO1)

Phase locked Loop

Power Amplifier (U4)

Driver Amplifier (U6)

Antenna

Antenna is for optimal receiving of transmission signal from base station.

Reduce damage of weak signal under general external environment and voltage from device to a minimum.

2. Antenna Switch

The RF switch is it can be controlled with positive, negative or a combination of both voltages. Some standard implementations include antenna changeover, Transmit/Receive and diversity switching over 3W.

3. AGC (Automatic Gain Controller) Circuit

Level of signal which device receiving should maintain regular signal and AGC is for Power control of device.

4. LNA (Low Noise Amplifier)

LNA is used for reducing noise to a maximum for optimal signal and amplify signal that need to receive separately.

5. RF SAW (Surface Acoustic Wave) Filter

RF Saw Filter is used for band pass for the signal of receiving frequency and reduce other signal except receiving frequency in order to receive selected receiving frequency of Pager.

6. Down Converter (MIXER)

Down Converter is used for one output against two input signal and making IF signal by combining amplified RF signal from LNA with Local signal.

Adjust RF signal of 930.5MHz ±1.5MH & 938.5MHz±3.5MHz and local signal of 909.1MHz & 917.1MHz to downward as the next IF signal of 45MHz.

7. Crystal Filter for First IF (MCF1)

The filter is centered 45MHz. The output of the first mixer has four frequency components. The filter allows the passage of the desired IF frequency

8. IF Detector IC (U12)

The IF Detector IC is a 4-level frequency-shift keying (FSK) comparator and a bit rate filter switch.

9. Decoder (U26)

The decoder supports 1600, 3200, and 6400 bps decoding. Intermediate frequency signals are demodulated, synchronized, de-interleaved and error corrected prior to entry into a holding buffer. The holding buffer is then fed into a synchronous serial peripheral interface (SPI) which then converts the data into a parallel format. A resident real-time clock operates off a 76.8kHz crystal.

10. Operational Amplifier (U9, U19)

The Operational Amplifier is quad C-MOS operated on a single-power-supply, low voltage and low operating current

11. VCO(Voltage Controlled Oscillator)

VCO is used for creation of Local signal of ±1.5MHz.

12. VCTCXO(Voltage Controlled Temperature Compensated Crystal Oscillator)

VCTCXO is used for voltage supply for reference frequency of main set input.

It creates 16.8MHz frequency and input to PLL IC.

It controlled by voltage for exact frequency tuning.

12. PLL(Phase locked Loop)

PLL(PLL2) is frequency combiner of Dual mode. It output IF signal and Local signal if demultiplied signal and Phase of phase comparator is same.

13. Regulator

Regulator is used for authorization for regular voltage of VCO and RX circuit through Battery voltage.

14. Driver Amplifier

Drive amplifier (U6) is circuit for promote efficiency through supply amplified signal to power amp.

15. Power Amplifier

Power amplifier (U4) is amplifier circuit for the amplification of output signal in Drive amplifier (U6) in order to transmit the signal to base station through Antenna.