



Wireless CPU Quik Q2687 Product Technical Specification

Revision: 002

Date: September 2006

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Wireless CPU Quik Q2687

Product Technical Specification

Reference: **WA_ENG_Q2687_PTS_001**
Revision: **002**
Date: **September 11, 2006**



Powered by the Wavecom Operating System and Open AT®

Cautions

This platform contains a modular transmitter. This device is used for wireless applications. Note that all electronics parts and elements are ESD sensitive.

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Overview

This document defines and specifies the Wireless CPU Quik Q2687, available under this version:

- **Q2687:** EGSM/GPRS/EDGE 900/1800/850/1900 MHz version with 32 Mb of Burst Flash memory and 8 Mb of SRAM (32/8)

Document History

Level	Date	List of revisions	
001	07/12/2005	Creation (Preliminary version)	
002	03/01/2006	Reference number changed to WA_ENG_Q2687_PTS_001. Overview - Memory changed to SRAM "Parallel" word is added on the second line of the first paragraph.(Chapter 2.1) Input Supply voltage added, Vmin = 3.2V and Vmax = 4.5V (Chapter 2.2.1) Power Consumption table for EDGE is added (Chapter 2.2.2) Parallel Interface table, pins 51 and 53 are labeled as GPIO1 and GPIO2 (Chapter 2.5) Auxiliary Microphone (MIC1) external bias is added and typical application circuit Chapter 2.12.1.3) Electrical Characteristics Table, maximum CHG_IN Voltage is changed to 6.0V (Chapter 2.13) Notes on Caution, Trademark and Copyright is updated General Description has been modified (Chapter 1) Functional architecture is modified (Chapter 1.2) Dimensions typo error is corrected (Chapter 1.1.1) "Soldered connection" and "UFL Connector" are added for RF connection (Chapter 1.1.6)	
003	28/07/2006	"Overview" updated "Table of Figures" added "Caution" updated 1: "References" added 2: "General Description" updated 2.1.4 : "Interfaces" updated 2.1.6 : "Connection interfaces" updated 2.2 : "Functional description" updated 3.1: "General Purpose Connector (GPC)" updated 3.1 : "Power supply description" updated 3.2.1 : "Power Consumption" updated 3.3: " Electrical information for digital I/O" updated 3.4: "Serial interface" updated 3.5: "Parallel interface" updated 3.7: "Main Serial link (UART1)" updated 3.8: "Auxiliary serial link (UART2)" updated	

Level	Date	List of revisions	
		3.10: "General Purpose Input/output" updated 3.11: "Analog to Digital Converter" updated 3.12: "Digital to Analog Converter" added 3.13: "Temperature Sensor Interface" added 3.14: "Analog audio interface" updated 3.15: "Buzzer output" updated 3.16: "Battery charging interface" updated 3.17: "ON/~OFF signal" updated 3.18: "BOOT signal" updated 3.19: "Reset signal (~RESET)" updated 3.20: "External interrupt" updated 3.21: "VCC_2V8 and VCC_1V8 output" updated 3.22: "BAT-RTC (Back-up Battery)" updated 3.22: "FLASH-LED signal" updated 3.24: "Digital audio interface (PCM)" updated 3.25: "USB 2.0 interface" added 3.26.1: "RF connections" updated 0: "Caution: " updated 4: "Technical specification" updated 4.2: "Environmental Specification" updated 5: " Connector and peripheral device references" updated	

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1 References

1.1 Reference documents

For more details, several reference documents may be consulted. The Wavecom reference documents are provided in the Wavecom documents package, contrary to the general reference documents which are not authored by Wavecom.

1.1.1 Wavecom reference documents

- [1] Automotive Environmental Control Plan for Q2687 Wireless CPU
WM_QUA_Q2687_DCP_001
- [2] Q2687 Wireless CPU Customer Design Guidelines
WM_DEV_Q2687_PTS_007
- [3] Q2687 Wireless CPU Process Customer Guidelines
WM_PRJ_Q2686_PTS_004
- [4] AT Commands Interface Guide for OS 6.61
WM_DEV_OAT_UGD_014

1.1.2 General reference document

- [5] "I²C Bus Specification", Version 2.0, Philips Semiconductor 1998
- [6] ISO 7816-3 Standard

1.2 List of abbreviations

Abbreviations	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable

Abbreviations	Definition
CLK	CLOCK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhance Data rates for GSM Evolution
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EGPRS	Enhance GPRS
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications

Abbreviations	Definition
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive

Abbreviations	Definition
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Wireless CPU
SMS	Short M essage S ervice
SPI	Serial P eripheral Interface
SPL	Sound P ressure L evel
SPK	S Pea K er
SRAM	Static R AM
TBC	To B e C onfirmed
TDMA	Time D ivision M ultiple A ccess
TP	Test P oint
TVS	Transient V oltage S uppressor
TX	Transmit
TYP	TYP ical
UART	Universal A synchronous R eceiver- T ransmitter
USB	Universal S erial B us
USSD	Unstructured S upplementary S ervices D ata
VSWR	Voltage S tanding W ave R atio

2 General Description

2.1 General information

Wireless CPU Quik Q2687 is a self-contained E-GSM/GPRS/EDGE 900/1800 and 850/1900 quad-band Wireless CPU with the following features:

2.1.1 Overall dimensions

- Length: 40 mm
- Width: 32.2 mm
- Thickness: 4 mm

2.1.2 Environment and mechanics

- Green policy: RoHS compliant
- Complete shielding

The Q2687 Wireless CPU is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".

Wireless CPUs which are compliant with this directive are identified by the RoHS logo on their label.



2.1.3 GSM/GPRS/EGPRS Features

- 2-Watt EGSM – GPRS 900/850 radio section running under 3.6 Volts
- 1-Watt GSM-GPRS1800/1900 radio section running under 3.6 Volts
- 0.5-Watt EGPRS 900/850 radio section running under 3.6 Volts
- 0.4-Watt EGPRS 1800/1900 radio section running under 3.6 Volts
- Hardware GSM/GPRS class 10 and EGPRS class 10 capable

2.1.4 Interfaces

- Digital section running under 2.8V and 1.8V.
- 3V/1V8 SIM interface
- Complete interfacing:

General Description

- o Power supply
- o Serial link
- o Analog audio
- o PCM digital audio
- o SIM card
- o Keyboard
- o USB 2.0 slave
- o Serial LCD (not available with AT commands)
- o Parallel port for specific applications (under Open AT® control only) TBD

2.1.5 Operating system

- Real Time Clock (RTC) with calendar
- Battery charger
- Echo Cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS Operating System stack

2.1.6 Connection interfaces

Wireless CPU Quik Q2687 has four external connections:

- Three for RF circuit:
 - o UFL connector
 - o Soldered connection
 - o IMP connection
- One for baseband signals:
 - o 100-pin I/O connector (compatible with Wireless CPU Quik Q2686)

2.2 Functional architecture

The global architecture of the Wireless CPU Quik Q2687 is described below:

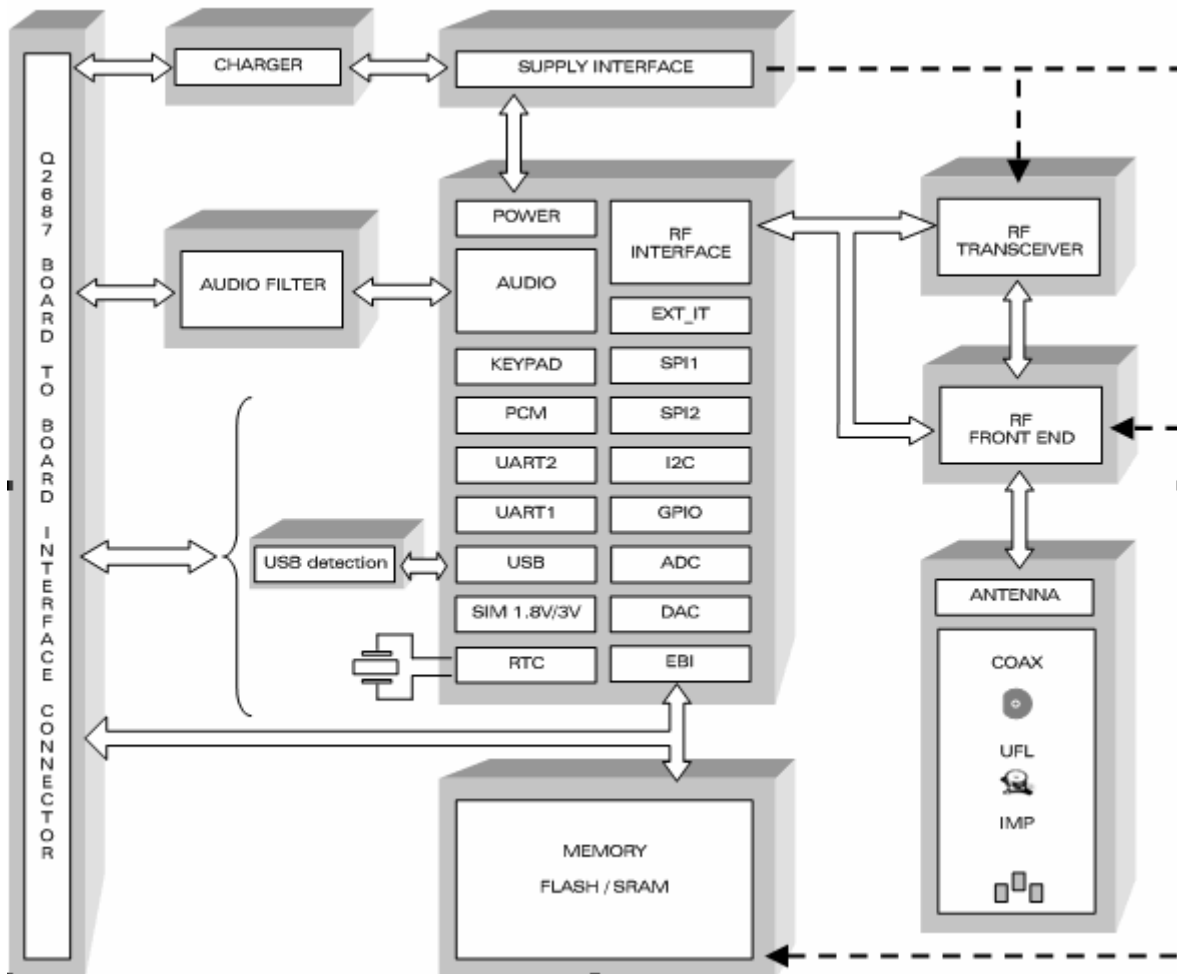


Figure 1: Functional architecture

2.2.1 RF functionalities

The Radio Frequency (RF) functionalities complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendation. The frequencies are:

	Transmit band (Tx)	Receive band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

The Radio Frequency (RF) part is based on a specific quad-band chip with a:

- Quad-band LNAs (Low Noise Amplifier)
- Direct Conversion Receiver
- Offset PLL/PL (Phase Locked Loop and Polar Loop) transmitter
- Frequency synthesizer
- Digitally controlled crystal oscillator (DCXO)
- Tx/Rx FEM (Front-End module) for quad-band GSM/GPRS

2.2.2 Baseband functionalities

The digital part of the Wireless CPU Quik Q2687 is composed of a PCF5213 PHILIPS chip. This chipset uses a 0,18 μ m mixed technology CMOS, which allows massive integration as well as low current consumption.

2.3 Operating System

Wireless CPU Quik Q2687 is designed to integrate various types of specific process applications such as vertical applications (telemetry, multimedia, automotive).

The Operating System offers a set of AT commands to control the Wireless CPU. With this standard Operating System, some interfaces of the Wireless CPU are not available, since they are dependent on the peripheral devices connected to the Wireless CPU.

The Operating System is Open AT® compliant.

3 Interfaces

3.1 General Purpose Connector (GPC)

A 100-pin connector is provided to interface the Wireless CPU Quik Q2687 with a board containing a serial or parallel LCD module, a keyboard, a SIM connector, and a battery connection.

The interfaces available on the GPC are described below.

chapter	Name	Driven by AT commands	Driven by Open AT®
3.4	Sérial Interface		X
3.5	Parallel Interface		X
3.6	Keyboard Interface	X	X
3.7	Main Sérial Link	X	X
3.8	Auxiliary Sérial Link	X	X
3.9	SIM Interface	X	X
3.10	Général Purpose IO	X	X
3.11	Analog to Digital Converter	X	X
3.12	Analog audio Interface	X	X
3.13	PWM / Buzzer Output	X	X
3.14	Battery Charging Interface	X	X
3.18	External Interruption	X	X
3.20	BAT-RTC (Backup Battery)	X	X
3.21	FLASH-LED signal	X	X
3.22	Digital Audio Interface (PCM)	X	X
3.23	USB 2.0 Interface	X	X

3.2 Power Supply

The power supply is one of the key issues in the design of a GSM terminal.

Due to the burst emission mode used in GSM / GPRS, the power supply must be able to deliver high current peaks in a short time. During the peaks, the ripple (Uripp) on the supply voltage must not exceed a certain limit (see Table 1 Power supply voltage).

In communication mode, a GSM/GPRS class 2 terminal emits 577 μ s radio bursts every 4.615ms (See the Figure 2).

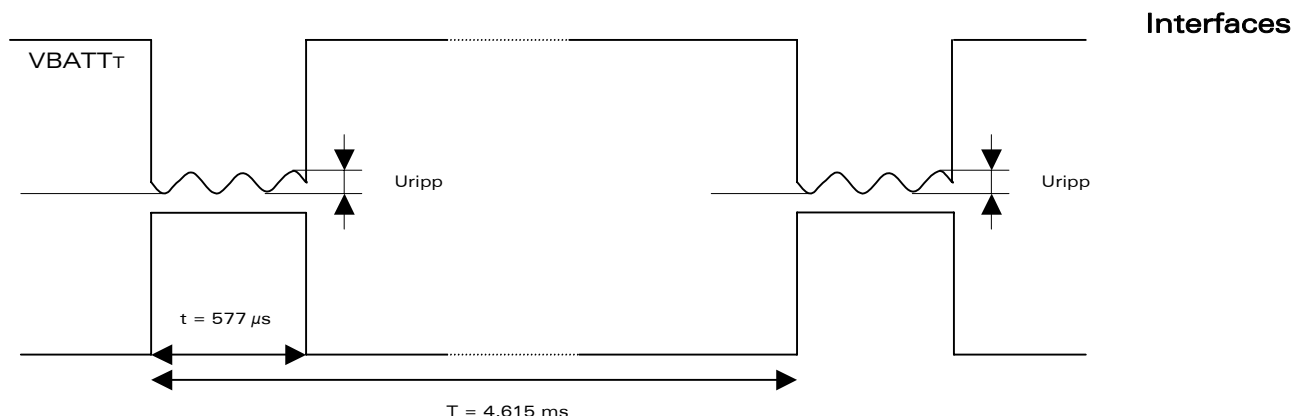


Figure 2: Power supply during burst emission

In communication mode, a GPRS class 10 terminal emits 1154 μs radio bursts every 4.615ms.

Only the VBATT power supply input is necessary to provide the Q2687 Wireless CPU.
VBATT:

- Directly supplies the RF components with 3,6 V. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error.

The RF Power Amplifier current (**2.0 A** peak in GSM /GPRS mode) flows with a ratio of:

- o 1/8 of the time (around 577 μs every 4.615ms for GSM /GPRS class 2),
- o 2/8 of the time (around 1154 μs every 4.615ms for GSM /GPRS class 10) and
- o The rise time is around 10 μs .
- Is internally used to provide via several regulators, the VCC_2V8 and VCC_1V8, the power supply required for the base band signals.

Wireless CPU Quik Q2687 shielding case is the grounding. The ground plane has to be connected to the motherboard through a complete layer on the PCB.

Input power Supply Voltage

	V _{MIN}	V _{NOM}	V _{MAX}	Ripple max (U _{ripp})
VBATT ^{1,2}	3.2	3.6	4.5	250mV (freq < 10kHz) 40mV (10kHz < freq < 100kHz) 5mV (freq > 100kHz)

Table 1 Power supply voltage

(1): This value has to be maintained during the burst (with 2.0A Peak in GSM, GPRS or EGPRS mode)

(2): The maximum operating Voltage Stationary Wave Ratio (VSWR) is 2:1

Interfaces

When supplying the Wireless CPU from a battery, the total impedance (battery + protections + PCB) should be <150 mOhms.

Caution:

When the Wireless CPU is in Alarm mode, no voltage must be applied on any pin of the 100-pin connector except on BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power ON the Wireless CPU.

3.2.1 Power consumption

Power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (AT or Open AT™).

All the following information is given assuming a 50 Ω RF output.

The following consumption values were obtained by performing measurements on Wireless CPU samples at a temperature of 25° C.

Three VBATT values are used to measure the consumption, VBATTmin (3.2V), VBATTmax (4.5V) and VBATTtyp (3.6V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For a more detailed description of the operating modes, see the Appendix of the AT Command Interface Guide OS 6.61 [4]

For more information about the consumption measurement procedure, see Wireless CPU Quik Q2687 Customer Design Guidelines [2].

3.2.1.1 Power consumption without Open AT® processing

The following measurement results are relevant only when:

- There is no Open AT® application
- The Open AT® application is disabled
- No processing is required by the Open AT® application

Power consumption without Open AT® application						
Operating mode	Parameters	I _{MIN} average VBATT=4,5V	I _{NOM} average VBATT=3,6V	I _{MAX} average VBATT=3,2V	I _{MAX} peak	unit
Alarm Mode		20.5	17.2	16.2		μA
Fast Idle Mode	Paging 9 (Rx burst occurrence ~2s)	14.4	15.3	16.6	160 _{RX}	mA
	Paging 2 (Rx burst occurrence ~0,5s)	15.6	16.8	17.7	160 _{RX}	mA
Slow Idle Mode ¹	Paging 9 (Rx burst occurrence ~2s)	1.94	1.84	1.80	160 _{RX}	mA
	Paging 2 (Rx burst occurrence ~0,5s)	4.3	4.4	4.6	160 _{RX}	mA
Fast Standby Mode		32.8	37.8	42.4		mA

Interfaces

Power consumption without Open AT [®] application							
Slow Standby Mode				1.2	1.1	1.0	mA
Connected Mode	850/900 MHz	PCL5 (TX power 33dBm)		235/235	241/242	240/237	1600 TX mA
		PCL19 (TX power 5dBm)		87/90	93/96	97/100	350 TX mA
	1800/1900 MHz	PCL0 (TX power 30dBm)		220/229	226/235	230/239	1500 TX mA
		PCL15 (TX power 0dBm)		91/91	97/97	101/101	340 TX mA
GPRS	Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	225/226	231/232	230/227	1600 TX mA
			Gam.17 (TX power 5dBm)	83/86	89/92	93/95	330 TX mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	211/219	217/225	220/229	1500 TX mA
			Gam.18 (TX power 0dBm)	86/87	92/92	96/96	320 TX mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	407/406	414/415	408/401	1600 TX mA
			Gam.17 (TX power 5dBm)	121/126	127/132	131/136	340 TX mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	378/392	384/400	388/405	1500 TX mA
			Gam.18 (TX power 0dBm)	127/128	133/134	137/138	330 TX mA
EGPRS	Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz	Gam.6 (TX power 27dBm)	161/157	167/163	171/167	1300 TX mA
			Gam.17 (TX power 5dBm)	90/93	97/100	101/104	400 TX mA
		1800/1900 MHz	Gam.5 (TX power 26dBm)	167/172	173/178	177/183	1400 TX mA
			Gam.18 (TX power 0dBm)	93/94	100/100	104/104	400 TX mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.6 (TX power 27dBm)	278/270	285/277	290/282	1300 TX mA
			Gam.17 (TX power 5dBm)	134/140	142/147	146/152	420 TX mA
		1800/1900 MHz	Gam.5 (TX power 26dBm)	291/303	298/310	302/314	1400 TX mA
			Gam.18 (TX power 0dBm)	141/142	148/149	153/154	420 TX mA

TX means: the current peak is RF transmission burst (Tx burst)

RX means: the current peak is RF reception burst (Rx burst)

¹ **Slow Idle Mode** consumption is dependent on the SIM card used. Some SIM cards respond faster than others, the longer the response time, the higher the

Interfaces

consumption. The measurements were performed on a large number of 3V SIM cards, and the results shown in the above table in brackets are the minimum and maximum currents measured from the SIM cards used.

3.2.1.2 Power consumption with Open AT® software

The power consumption with Open AT® software used is Dhrystone application, and the following consumption results were measured while performing on the Dhrystone application.

Power consumption with Dhrystone Open AT® application								
Operating mode		Parameters		I _{MIN} average VBATT=4,5V	I _{NOM} average VBATT=3,6V	I _{MAX} average VBATT=3,2V	I _{MAX} peak	unit
Alarm Mode				N/A	N/A	N/A		µA
Fast Idle Mode		Paging 9 (Rx burst occurrence ~2s)		33	38	41	160 _{RX}	mA
		Paging 2 (Rx burst occurrence ~0,5s)		33	38	42	160 _{RX}	mA
Slow Idle Mode		Paging 9 (Rx burst occurrence ~2s)		NA	NA	NA	NA	mA
		Paging 2 (Rx burst occurrence ~0,5s)		NA	NA	NA	NA	mA
Fast Standby Mode				32	38	40		mA
Slow Standby Mode				NA	NA	NA		mA
Connected Mode		850/900 MHz	PCL5 (TX power 33dBm)	235/235	241/242	240/237	1600 _{TX}	mA
			PCL19 (TX power 5dBm)	87/90	93/96	97/100	350 _{TX}	mA
		1800/1900 MHz	PCL0 (TX power 30dBm)	220/229	226/235	230/239	1500 _{TX}	mA
			PCL15 (TX power 0dBm)	91/91	97/97	101/101	340 _{TX}	mA
GPRS	Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	225/226	231/232	230/227	1600 _{TX}	mA
			Gam.17 (TX power 5dBm)	83/86	89/92	93/95	330 _{TX}	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	211/219	217/225	220/229	1500 _{TX}	mA
			Gam.18 (TX power 0dBm)	86/87	92/92	96/96	320 _{TX}	mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	407/406	414/415	408/401	1600 _{TX}	mA
			Gam.17 (TX power 5dBm)	121/126	127/132	131/136	340 _{TX}	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	378/392	384/400	388/405	1500 _{TX}	mA
			Gam.18 (TX power 0dBm)	127/128	133/134	137/138	330 _{TX}	mA

Power consumption with Dhrystone Open AT® application								
EGPRS	Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz	Gam.6 (TX power 27dBm)	161/157	167/163	171/167	1300 _{TX}	mA
			Gam.17 (TX power 5dBm)	90/93	97/100	101/104	400 _{TX}	mA
		1800/1900 MHz	Gam.5 (TX power 26dBm)	167/172	173/178	177/183	1400 _{TX}	mA
			Gam.18 (TX power 0dBm)	93/94	100/100	104/104	400 _{TX}	mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.6 (TX power 27dBm)	278/270	285/277	290/282	1300 _{TX}	mA
			Gam.17 (TX power 5dBm)	134/140	142/147	146/152	420 _{TX}	mA
		1800/1900 MHz	Gam.5 (TX power 26dBm)	291/303	298/310	302/314	1400 _{TX}	mA
			Gam.18 (TX power 0dBm)	141/142	148/149	153/154	420 _{TX}	mA

3.2.1.3 Consumption waveform samples

The consumption waveforms are given for a EGSM900 network configuration with AT software running on the Q2687/OS6.61 Wireless CPU.

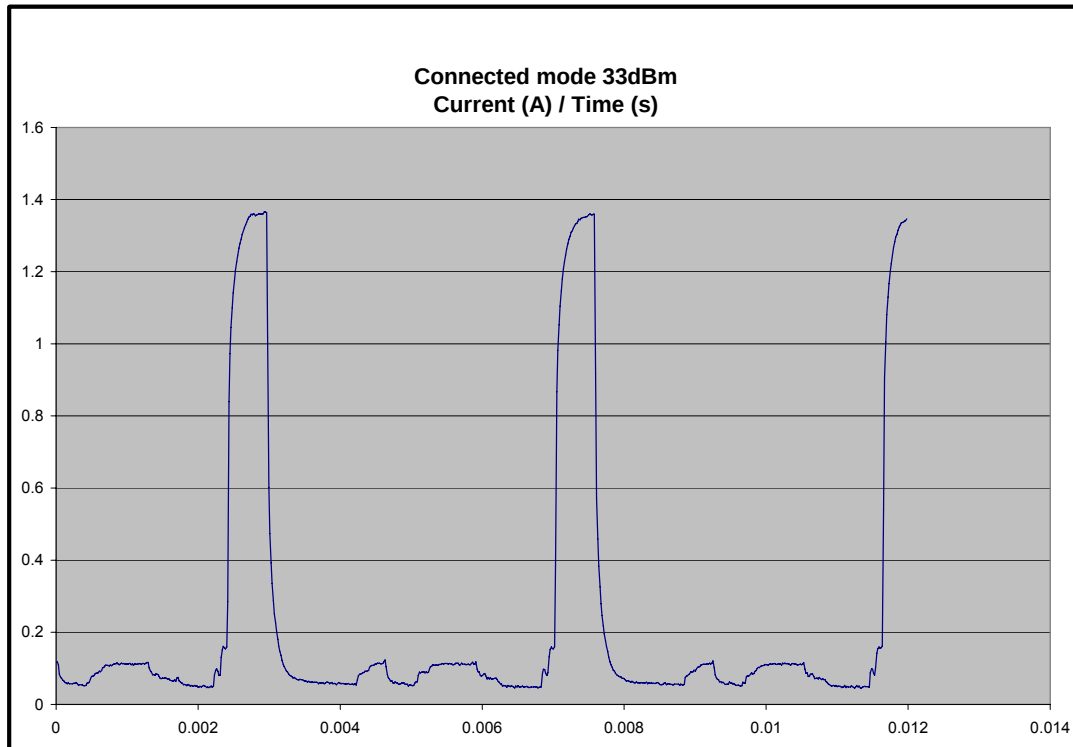
The VBATT voltage value is 3.6V typical.

Four significant operating mode consumption waveforms are described as:

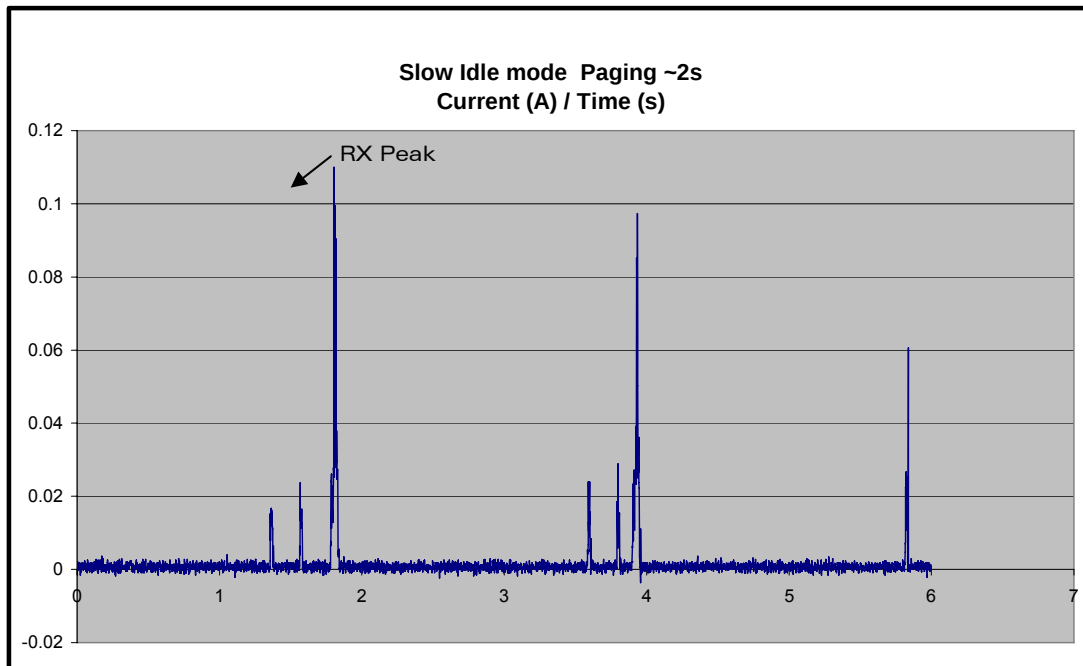
- Connected Mode (PCL5: Tx power 33dBm)
- Slow Idle mode (Paging 9)
- Fast idle mode (Paging 9)
- Transfer mode (GPRS class 10, PCL3: Tx power 33dBm)

The following waveform displays only the form of the current and for correct current values, see the section 3.2.1.1.

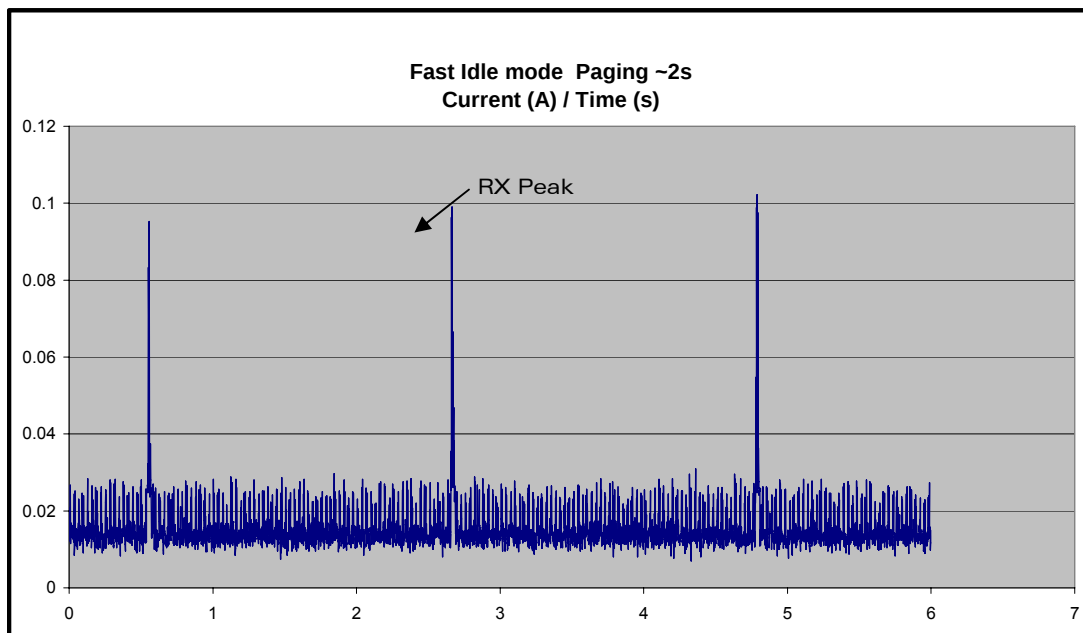
3.2.1.3.1 Connected mode current waveform



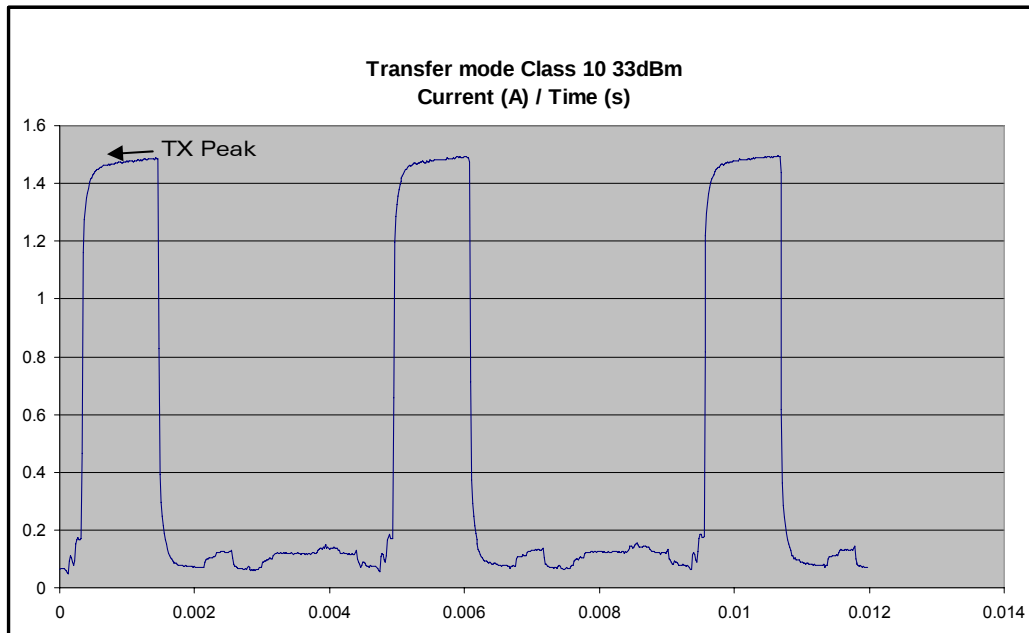
3.2.1.3.2 Slow Idle mode current waveform



3.2.1.3.3 Fast Idle mode current waveform



3.2.1.3.4 Transfer mode Class 10 current waveform



3.2.1.4 Power supply pin-out

Power Supply Pin-out

Signal	Pin number
VBATT	1,2,3,4
GND	Shielding

The grounding connection is made through the shielding ⇒ the four leads must be soldered to the ground plane.

3.3 Electrical information for digital I/O

The three types of digital I/O on the Wireless CPU Quik Q2687 are: 2.8Volt CMOS, 1.8Volt CMOS, and Open drain.

The three types are as described below:

Electrical characteristics of digital I/O

2.8 Volt type (2V8)						
Parameter		I/O type	Min.	Typ	Max.	Condition
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output pin	V _{IL}	CMOS	-0.5V*		0.84V	
	V _{IH}	CMOS	1.96V		3.2V*	
	V _{OL}	CMOS			0.4V	I _{OL} = - 4 mA
	V _{OH}	CMOS	2.4V			I _{OH} = 4 mA
	I _{OH}				4mA	
	I _{OL}				- 4mA	

*Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltage above the maximum voltage as specified in the above table, **except for the UART1 interface, which is 3.3V tolerant.**

1.8 Volt type (1V8)						
Parameter		I/O type	Min.	Typ	Max.	Condition
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V _{IL}	CMOS	-0.5V*		0.54V	
	V _{IH}	CMOS	1.33V		2.2V*	
	V _{OL}	CMOS			0.4V	I _{OL} = - 4 mA
	V _{OH}	CMOS	1.4V			I _{OH} = 4 mA
	I _{OH}				4mA	
	I _{OL}				- 4mA	

*Absolute maximum ratings

Interfaces

Open drain output type						
Signal name	Parameter	I/O type	Minimum	Typ	Maximum	Condition
FLASH-LED	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			8mA	
BUZZ-OUT	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			100mA	
SDA / GPIO27 and SCL / GPIO26	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			
	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The I/Os reset states are described in each interface description chapter. Definitions of these states are as given below:

Reset state definition	
Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~60K resistor.
Pull-up	Internal pull-up with ~60K resistor to supply 1V8 or 2V8 depending on I/O type.
Z	High impedance
Undefined	Caution: undefined must not be used in your application if a special state is required at reset. These pins may be a toggling signal during reset.

3.4 Serial interface

The Wireless CPU Quik Q2687 may be connected to an LCD Wireless CPU driver through either by two SPI bus or an I²C 2-wire interface.

3.4.1 SPI bus

Both SPI bus interfaces include:

- A CLK signal

- An I/O signal
- An I signal
- A CS signal complying with the standard SPI bus.

SPI bus characteristics:

- Master mode operation
- SPI speed ranges from 101.5 Kbit/s to 13 Mbit/s in master mode operation
- 3 or 4-wire interface
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

3.4.1.1 SPI waveforms

Waveform for SPI transfer with 4-wire configuration in master mode 0 (chip selection is not displayed).

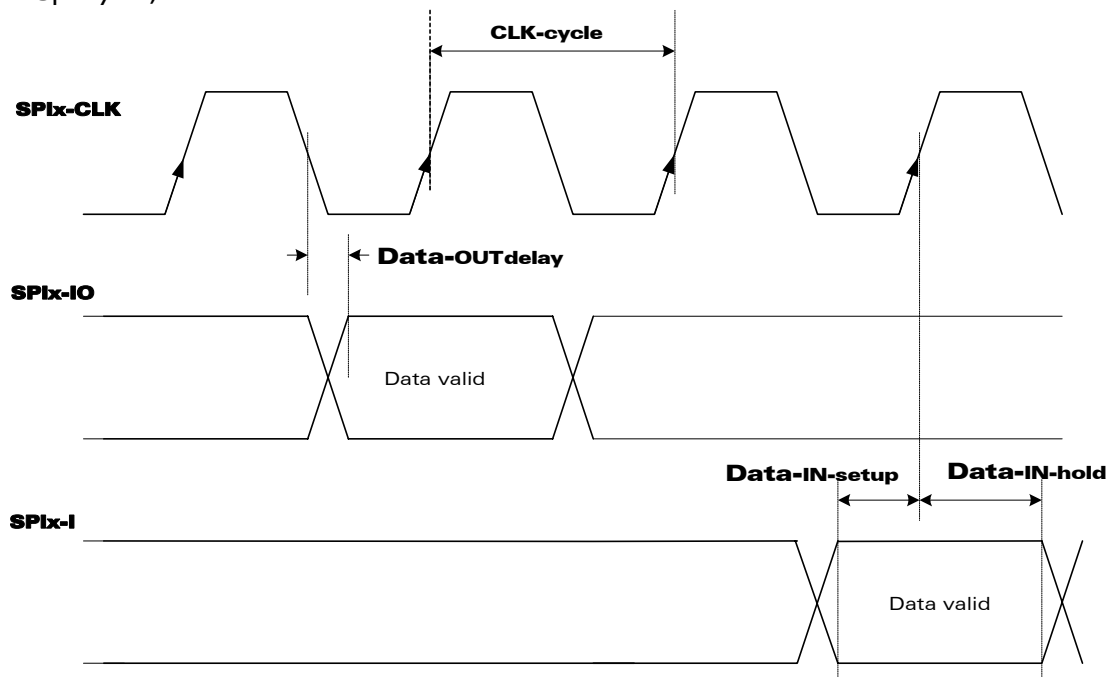


Figure 3: SPI Timing diagrams, Mode 0, Master, and 4-wire

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
CLK-cycle	SPI clock frequency	0.1015		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

3.4.1.2 SPI configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire type	4-wire type
Master	13 Mb/s	0,1,2,3	Half	SPIx-CLK; SPIx-IO; ~SPIx-CS	SPIx-CLK; SPIx-IO; SPIx-I; ~SPIx-CS

For the 4-wire configuration, SPIx-I/O is used as output only and SPIx-I is used as input only.

For the 3-wire configuration, SPIx-I/O is used for both as input and output.

3.4.1.3 SPI1 bus

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI1-CLK	23	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	25	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	24	I	2V8	Z	SPI Serial input	GPIO30
~SPI1-CS	22	O	2V8	Z	SPI Enable	GPIO31

For Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition, refer to section 3.3, "Electrical information for digital I/O".

3.4.1.4 SPI2 bus

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI2-CLK	26	O	2V8	Z	SPI Serial Clock	GPIO32
SPI2-IO	27	I/O	2V8	Z	SPI Serial input/output	GPIO33
SP2-I	29	I	2V8	Z	SPI Serial input	GPIO34
~SPI2-CS	28	O	2V8	Z	SPI Enable	GPIO35

See section 3.3 "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.4.2 I²C bus

The I²C interface includes a clock signal (SCL) and data signal (SDA) complying with a 100Kbit/s-standard interface (standard mode: s-mode).

The I²C bus is always in master mode.

The maximum speed transfer range is 400Kbit/s (fast mode: f-mode).

For more information on the I²C bus, see the "I²C Bus Specification Version 2.0" from PHILIPS.

3.4.2.1 I²C waveforms

I²C bus waveform in master mode configuration:

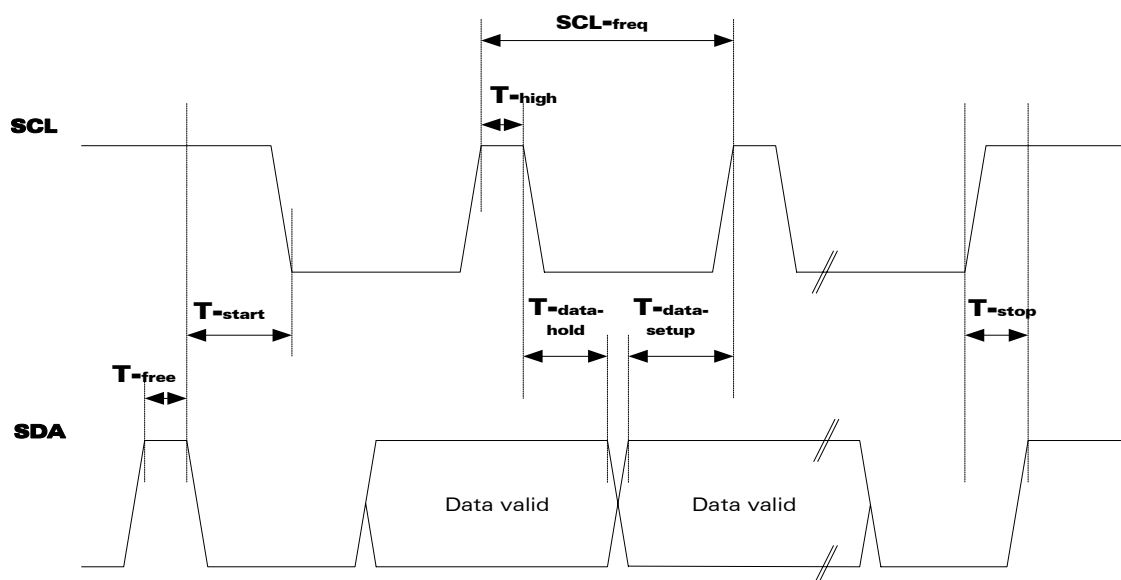


Figure 4: I²C Timing diagrams, Master

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
SCL-freq	I ² C clock frequency	100		400	KHz
T-start	Hold time START condition	0.6			μs
T-stop	Setup time STOP condition	0.6			μs
T-free	Bus free time, STOP to START	1.3			μs
T-high	High period for clock	0.6			μs
T-data-hold	Data hold time	0		0.9	μs
T-data-setup	Data setup time	100			ns

3.4.2.2 I²C bus pin-out

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SCL	44	O	Open drain	Z	Serial Clock	GPIO26
SDA	46	I/O	Open drain	Z	Serial Data	GPIO27

See section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.5 Parallel Interface

The Wireless CPU Quik Q2687 offers a 16-bit wide parallel bus interface.

Few signals are multiplexed. It is possible to have these configurations.

For software information, see the document [4].

- CS3*, A1, GPIO1, GPIO2
- CS3*, A1, A24, GPIO1
- CS3*, A1, A24, A25
- CS3*, CS2*, A1, GPIO2
- CS3*, CS2*, A1, A24

Signal	Pin number	Reset state	I/O	I/O type	Description	Multiplexed with
D0	85	Pull down	I/O	1v8	Data bus	Not mux
D1	87	Pull down	I/O	1v8	Data bus	Not mux

Interfaces

Signal	Pin number	Reset state	I/O	I/O type	Description	Multiplexed with
D2	89	Pull down	I/O	1v8	Data bus	Not mux
D3	91	Pull down	I/O	1v8	Data bus	Not mux
D4	93	Pull down	I/O	1v8	Data bus	Not mux
D5	95	Pull down	I/O	1v8	Data bus	Not mux
D6	97	Pull down	I/O	1v8	Data bus	Not mux
D7	99	Pull down	I/O	1v8	Data bus	Not mux
D8	100	Pull down	I/O	1v8	Data bus	Not mux
D9	98	Pull down	I/O	1v8	Data bus	Not mux
D10	96	Pull down	I/O	1v8	Data bus	Not mux
D11	94	Pull down	I/O	1v8	Data bus	Not mux
D12	92	Pull down	I/O	1v8	Data bus	Not mux
D13	90	Pull down	I/O	1v8	Data bus	Not mux
D14	88	Pull down	I/O	1v8	Data bus	Not mux
D15	86	Pull down	I/O	1v8	Data bus	Not mux
/OE-R/W	81	1	O	1v8	Read Operation	Not mux
/WE-E	84	1	O	1v8	Write Operation	Not mux
/CS3	83	1	O	1v8	User Chip select	Not mux
/CS2	51	Undefined	I/O	1v8	User Chip Select	A25/GPIO1
A1	42	1	O	1v8	Address bus 1	Not mux
A24	53	Undefined	I/O	1v8	Data/Command selection	GPIO2

3.6 Keyboard interface

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4) and
- 5 columns (COL0 to COL4).

Scanning is digital and debouncing is performed in the Wireless CPU Quik Q2687.

No discrete components such as Rs, Cs (Resistors, Capacitors) are needed.

Pin description of the Keyboard interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
ROW0	68	I/O	1V8	0	Row scan	GPIO9
ROW1	67	I/O	1V8	0	Row scan	GPIO10
ROW2	66	I/O	1V8	0	Row scan	GPIO11
ROW3	65	I/O	1V8	0	Row scan	GPIO12
ROW4	64	I/O	1V8	0	Row scan	GPIO13
COL0	59	I/O	1V8	Pull-up	Column scan	GPIO4
COL1	60	I/O	1V8	Pull-up	Column scan	GPIO5
COL2	61	I/O	1V8	Pull-up	Column scan	GPIO6
COL3	62	I/O	1V8	Pull-up	Column scan	GPIO7
COL4	63	I/O	1V8	Pull-up	Column scan	GPIO8

See section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.7 Main serial link (UART1)

A flexible 6-wire serial interface is available, complies with V24 protocol signaling, but not with V28 (electrical interface) due to a 2.8-Volt interface.

The signals are as follows:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)
- Data Terminal Ready (~CT108-2/DTR)
- Data Set Ready (~CT107/DSR).

The set of RS-232 signals may be required for GSM DATA services application and is generated by the General Purpose I/O provided by the Wireless CPU Quik Q2687.

The two additional signals are:

- Data Carrier Detect (~CT109/DCD) and
- Ring Indicator (CT125/RI).

Pin description of UART1 interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103/TXD1*	71	I	2V8	Z	Transmit serial data	GPIO36
CT104/RXD1*	73	O	2V8	1	Receive serial data	GPIO37
~CT105/RTS1*	72	I	2V8	Z	Request To Send	GPIO38
~CT106/CTS1*	75	O	2V8	Z	Clear To Send	GPIO39
~CT107/DSR1*	74	O	2V8	Z	Data Set Ready	GPIO40
~CT108-2/DTR1*	76	I	2V8	Z	Data Terminal Ready	GPIO41
~CT109/DCD1 *	70	O	2V8	Undefined	Data Carrier Detect	GPIO43
~CT125/RI1 *	69	O	2V8	Undefined	Ring Indicator	GPIO42
CT102/GND*	Shielding leads		GND		Ground	

See Section "3.3 Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

*According to PC view

The **rise** and **fall time** of the reception signals (mainly due to CT103) must be less than **300 ns**.

The Q2687 Wireless CPU is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

The maximum baud rate of UART1 is **115 Kbit/s**.

3.8 Auxiliary serial link (UART2)

The Bluetooth application on auxiliary serial interface (UART2) is available on Wireless CPU Quik Q2687 product. See the Application Note WM_ASW_AOT_APN_016 and the document [4].

Pin description of UART2 interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103 / TXD2*	31	I	1V8	Z	Transmit serial data	GPIO14
CT104 / RXD2*	30	O	1V8	Z	Receive serial data	GPIO15
~CT106 / CTS2*	32	O	1V8	Z	Clear To Send	GPIO16
~CT105 / RTS2*	33	I	1V8	Z	Request To Send	GPIO17

See Section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

* According to PC view

The Q2687 is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

The maximum baud rate of UART2 is **115** Kbit/s.

3.9 SIM interface

The Subscriber Identification Module (SIM) may be directly connected to the Wireless CPU Quik Q2687 via this dedicated interface.

3.9.1 General Description

The five signals are:

- SIM-VCC: SIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: SIM card detect

The SIM interface controls a 3V/1V8 SIM. This interface is fully compliant with the GSM 11.11 recommendations related to SIM functions.

Pin description of SIM interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SIM-CLK	14	O	2V9 / 1V8	0	SIM Clock	Not mux
~SIM-RST	13	O	2V9 / 1V8	0	SIM Reset	Not mux
SIM-IO	11	I/O	2V9 / 1V8	*Pull-up	SIM Data	Not mux
SIM-VCC	9	O	2V9 / 1V8		SIM Power Supply	Not mux
SIMPRES	12	I	1V8	Z	SIM Card Detect	GPIO18

*SIM-IO pull-up is about 10K ohm

See Section 3.3 "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical Characteristics of the SIM interface

Parameter	Conditions	Min.	Typ	Max.	Unit
SIM-IO V_{IH}	$I_{IH} = \pm 20\mu A$	0.7xSIMVCC			V
SIM-IO V_{IL}	$I_{IL} = 1mA$			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = $20\mu A$	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = $20\mu A$	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = $-200\mu A$			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.6V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	μs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

Note:

When **SIMPRES** is used, a **low to high** transition means that the SIM card is inserted and a **high to low** transition means that the SIM card is removed.

3.10 General Purpose Input/Output

The Wireless CPU Quik Q2687 provides up to 44 General Purpose I/O. They are used to control any external device such as a LCD or a Keyboard backlight.

All grey highlighted I/O are 1V8 whereas the others (not highlighted in grey) are 2V8.

Pin description of the GPIO

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
GPIO1	51	I/O	1V8	Undefined	A25/~CS2*
GPIO2	53	I/O	1V8	Undefined	A24*
GPIO3	50	I/O	1V8	Z	INT0
GPIO4	59	I/O	1V8	Pull up	COL0
GPIO5	60	I/O	1V8	Pull up	COL1
GPIO6	61	I/O	1V8	Pull up	COL2
GPIO7	62	I/O	1V8	Pull up	COL3
GPIO8	63	I/O	1V8	Pull up	COL4
GPIO9	68	I/O	1V8	0	ROW0
GPIO10	67	I/O	1V8	0	ROW1
GPIO11	66	I/O	1V8	0	ROW2
GPIO12	65	I/O	1V8	0	ROW3
GPIO13	64	I/O	1V8	0	ROW4
GPIO14	31	I/O	1V8	Z	CT103 / TXD2
GPIO15	30	I/O	1V8	Z	CT104 / RXD2
GPIO16	32	I/O	1V8	Z	~CT106 / CTS2
GPIO17	33	I/O	1V8	Z	~CT105 / RTS2
GPIO18	12	I/O	1V8	Z	SIMPRES
GPIO19	45	I/O	2V8	Z	Not mux
GPIO20	48	I/O	2V8	Undefined	Not mux
GPIO21	47	I/O	2V8	Undefined	Not mux
GPIO22	57	I/O	2V8	Z	Not mux**

Interfaces

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
GPIO23	55	I/O	2V8	Z	Not mux**
GPIO24	58	I/O	2V8	Z	Not mux
GPIO25	49	I/O	2V8	Z	INT1
GPIO26	44	I/O	Open drain	Z	SCL
GPIO27	46	I/O	Open drain	Z	SDA
GPIO28	23	I/O	2V8	Z	SPI1-CLK
GPIO29	25	I/O	2V8	Z	SPI1-IO
GPIO30	24	I/O	2V8	Z	SP1-I
GPIO31	22	I/O	2V8	Z	~SPI1-CS
GPIO32	26	I/O	2V8	Z	SPI2-CLK
GPIO33	27	I/O	2V8	Z	SPI2-IO
GPIO34	29	I/O	2V8	Z	SP2-I
GPIO35	28	I/O	2V8	Z	~SPI2-CS
GPIO36	71	I/O	2V8	Z	CT103 / TXD1
GPIO37	73	I/O	2V8	1	CT104 / RXD1
GPIO38	72	I/O	2V8	Z	~CT105 / RTS1
GPIO39	75	I/O	2V8	Z	~CT106 / CTS1
GPIO40	74	I/O	2V8	Z	~CT107 / DSR1
GPIO41	76	I/O	2V8	Z	~CT108-2 / DTR1
GPIO42	69	I/O	2V8	Undefined	~CT125 / RI1
GPIO43	70	I/O	2V8	Undefined	~CT109 / DCD1
GPIO44	43	I/O	2V8	Undefined	Not mux

See Section "3.3 Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

* If the parallel bus is used, these pins will be mandatory for the parallel bus functionality. See "Section 3.5"

** If a Bluetooth module is used with the Q2687 Wireless CPU, this GPIO must be reserved.

3.11 Analog to Digital Converter

Two Analog to Digital Converter (ADC) inputs are provided by the Wireless CPU Quik Q2687. The converters are 10-bit resolution, ranges from 0V to 2V.

Pin description of the ADC

Signal	Pin number	I/O	I/O type	Description
BAT-TEMP*	20	I	Analog	A/D converter
AUX-ADC	21	I	Analog	A/D converter

This input is reserved for a battery charging temperature sensor, see Section 3.16, "Battery Charging interface".

Electrical Characteristics of the ADC

Parameter		Min	Typ	Max	Unit
Resolution			10		bits
Sampling rate				138 ¹	sps
Input signal range		0		2	V
INL (Integral non linearity)			15		mV
DNL (Differential non linearity)			2.5		mV
Input impedance	BAT-TEMP		1M*		Ω
	AUX-ADC		1M		Ω

* Internal pull-up to 2.8V

¹ Sampling rate only for AUX-ADC and Open AT® application

3.12 Digital to Analog Converter

One Digital to Analog Converter (DAC) input is provided by the Q2687 Wireless CPU. The converter is 8-bit resolution, ranges from 0V to 2.3V.

Pin description of the DAC

Signal	Pin number	I/O	I/O type	Description
AUX-DAC	82	O	Analog	D/A converter

This output assumes a typical external load of 2kΩ and 50pF in parallel.

Electrical Characteristics of the DAC

Parameter	Min	Typ	Max	Unit
Resolution		8		bits
Output signal range	0		2.3	V
Output voltage after reset		1.147		V
INL (Integral non linearity)	-5		+5	LSB
DNL (Differential non linearity)	-1		+1	LSB

3.13 Temperature Sensor Interface

A temperature sensor is implanted in the Q2687 Wireless CPU. The software may inform (via an ADC) the temperature in the Q2687 Wireless CPU. The following waveform describes the characteristic of this function.

For more details, see the document [4].

The average step is 15mV / °C.

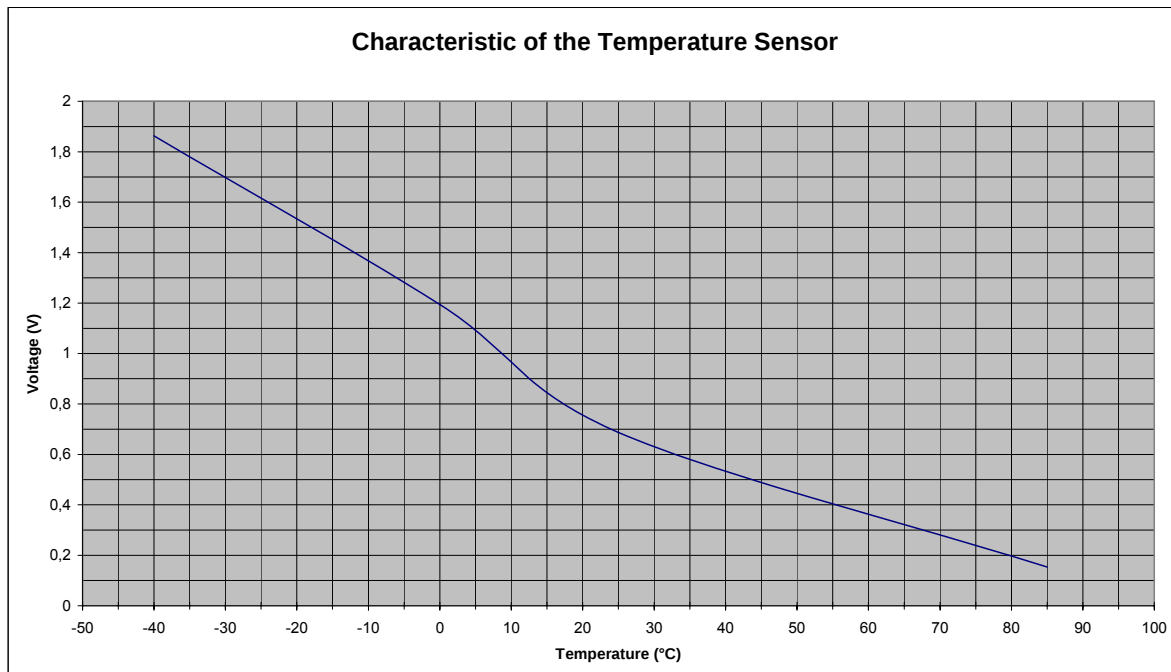


Figure 5: Characteristics of the Temperature Sensor

3.14 Analog audio interface

Two different microphone inputs and two different speaker outputs are supported.

The Wireless CPU Quik Q2687 also includes an echo cancellation feature, which allows hands-free functionality.

3.14.1 Microphone inputs

The MIC2 inputs already include the biasing for an electret microphone, thus allowing easy connection.

The MIC1 input requires external biasing, if an electret microphone is used.

3.14.1.1 Common microphone input characteristics

The connection may be either differential or single-ended but use of a differential connection in order to reject common mode noise and TDMA noise is strongly recommended. When using a single-ended connection, be sure to have a good ground plane, good filtering and also shielding, in order to avoid any disturbance on the audio path.

The gain of the MIC inputs is internally adjusted and may be tuned using an AT command.

Both may be configured either as differential or single-ended.

3.14.1.2 Main Microphone Inputs (MIC2)

By default, the MIC2 inputs are differential inputs, but may also be configured as single-ended. MIC2 inputs already include convenient biasing for an electret microphone. The electret microphone may be directly connected to these inputs.

AC coupling is already embedded in the Wireless CPU.

Pin description of MIC2

Signal	Pin number	I/O	I/O type	Description
MIC2P	36	I	Analog	Microphone 2 positive input
MIC2N	34	I	Analog	Microphone 2 negative input

3.14.1.3 Auxiliary Microphone Inputs (MIC1)

By default, the MIC1 inputs are single-ended, but may also be configured as differential. An external biasing is needed if an electret microphone is used.

AC coupling is already embedded in the Wireless CPU.

Pin description of MIC1

Signal	Pin number	I/O	I/O type	Description
MIC1P	40	I	Analog	Microphone 1 positive input
MIC1N	38	I	Analog	Microphone 1 negative input

3.14.1.4 Microphone electrical characteristics

The characteristics of both Wireless CPU Quik Q2687 microphone inputs are defined in the following tables.

MIC2 Characteristics					
Parameter		Min.	Typ	Max.	Unit
Internal Biasing	Voltage	2	2.1	2.2	V
	Output Current			1.5	mA
Impedance single-ended	Internal AC coupling		100		nF
	MIC2P (MIC2N left open)	1100	1340	1600	Ω
	MIC2P (MIC2N = GND)	900	1140	1400	Ω
	MIC2N (MIC2P left open)	1100	1340	1600	Ω
	MIC2N (MIC2P = GND)	900	1140	1400	Ω
Input voltage	Differential Input Voltage*			346	mV _{RMS}
	Absolute maximum ratings	0		6V **	V

MIC1 Characteristics					
Parameter		Min.	Typ	Max.	Unit
Internal Biasing	Voltage		N/A		V
	Output Current		N/A		A
Impedance single-ended	Internal AC coupling		100		nF
	MIC1P (MIC1N left open)	70	100	162	k Ω
	MIC1P (MIC1N = GND)	70	100	162	k Ω
	MIC1N (MIC1P left open)	70	100	162	k Ω
	MIC1N (MIC1P = GND)	70	100	162	k Ω
Input voltage	Differential Input Voltage *			346	mV _{RMS}
	Absolute maximum ratings	0		6	V

* The input voltage depends on the input microphone gain set by AT command.

** Because MIC2P is internally biased, a coupling capacitor must be used to connect an audio signal provided by an active generator. Only a passive microphone may be directly connected to the MIC2P and MIC2N inputs.

3.14.2 Common speaker output characteristics

The connection is single-ended on SPK1 and either a differential or single-ended on SPK2. Use of a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover, in single-ended mode, 1/2 of the power is lost. When using a single-ended connection, be sure to have a good ground plane, a good filtering and also shielding, in order to avoid any disturbance on the audio path.

3.14.2.1 Differential Connection

Impedance of the speaker amplifier output in differential mode is shown below:

Parameter	Typ	Unit
Z (SPK2P, SPK2N)	8	Ω

3.14.2.2 Single-ended connection

Impedance of the speaker amplifier output in single-ended mode is shown below:

Electrical Characteristics

Parameter	Typ	Unit
Z (SPK1P, SPK1N)	16 or 32	Ω
Z (SPK2P, SPK2N)	4	Ω

3.14.3 Speaker outputs

3.14.3.1 Speaker 2 outputs

Pin description of Speaker 2 outputs

Signal	Pin number	I/O	I/O type	Description
SPK2P	39	O	Analog	Speaker 2 positive output
SPK2N	41	O	Analog	Speaker 2 negative output

3.14.3.2 Speaker 1 outputs

Pin description of Speaker 1 outputs

Signal	Pin number	I/O	I/O type	Description
SPK1P	35	O	Analog	Speaker 1 positive output
SPK1N	37	O	Analog	Speaker 1 negative output

3.14.3.3 Speaker output power

The maximum power output of the two speakers is not the same due to different configurations between Speaker1, which is only single-ended, and speaker2, which may be differential. Speaker2 thus provides more power.

The maximum specifications given below are available with the maximum power output configuration values set by AT command.

Speaker1 single-ended SPK1P output characteristics					
Parameter		Min.	Typ	Max.	Unit
Output Biasing	Voltage		1.30		V
Output Voltage		0		2.75	V _{PP}
Output Power	Single-ended with 32-ohm load			27	mW
Output Current	Maximum tolerated			85	mA

Only SPK1P may be used.

Interfaces

Speaker2 differential output characteristics					
Parameter		Min.	Typ	Max.	Unit
Output Biasing	Voltage SPK2P and SPK2N		1.30		V
Output Voltage	Voltage on SPK2P	0		0.9	V _{PP}
	Voltage on SPK2N	0		0.9	V _{PP}
	Diff voltage (SPK2P – SPK2N)	0		1.8	V _{PP}
Output Power	Differential with 8-ohm load			48	mW
Output Current	Maximum tolerated			110	mA

If a single-ended solution is used with the speaker2 output, only one of the two SPK2s must be selected. The result is maximum output power divided by 2.

3.15 Buzzer output

This output is controlled by a pulse width modulation controller and may be used only as buzzer.

BUZZ-OUT is an open drain output. A buzzer may be directly connected between this output and VBATT. The maximum current is 100 mA (PEAK).

Pin description of PWM/Buzzer output

Signal	Pin number	I/O	I/O type	Reset state	Description
BUZZ-OUT	15	O	Open drain	Z	Buzzer output

See Section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical Characteristics

Parameter	Condition	Minimum	Maximum	Unit
V _{OL on}	I _{ol} = 100mA		0.4	V
I _{PEAK}	VBATT = VBATTmax		100	mA
Frequency		1	50000	Hz

3.16 Battery charging interface

The Wireless CPU Quik Q2687 supports one battery charging circuit, two algorithms and one hardware charging mode (pre-charging) for 3 battery technologies:

- Ni-Cd (Nickel-Cadmium) with algorithm 0
- Ni-Mh (Nickel-Metal Hydride) with algorithm 0
- Li-Ion (Lithium-Ion) with algorithm 1

The two algorithms control a switch, which connects the CHG-IN signal to the VBATT signal. The algorithm controls the frequency and the connected time of the switch. During the charging procedure, battery charging level is controlled and when the Li-Ion algorithm is used, battery temperature is monitored via the BAT-TEMP ADC input.

One more charging procedure is available in the Q2687 Wireless CPU. This is called "Pre-charging" mode, but is a special charging mode as it is activated only when the Wireless CPU is OFF. Control is thus performed by the hardware. The purpose of this charging mode is to avoid battery damage by preventing the battery from being discharged to below the minimum battery level.

3.16.1 Ni-Cd / Ni-Mh charging algorithm

To charge the battery, the algorithm measures battery level when the switch is open (T2) and charges the battery by closing the switch (T3). When the battery is charged (battery voltage reaches BattLevelMax) the switch is open for time T3.

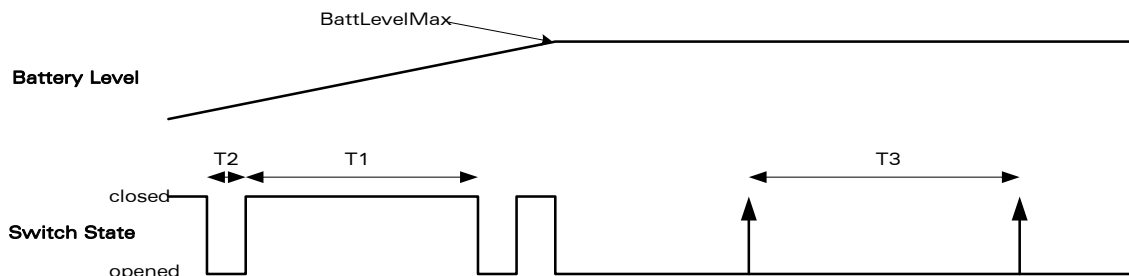


Figure 6 : Ni-Cd / Ni-Mh charging waveform

Electrical Characteristics of Ni-Cd / Ni-Mh battery timing charge

Parameter	Min	Typ	Max	Unit
T1		1		s
T2		0.1		s
T3		5		s

Note: T1,T2,T3, and BattLevelMax may be configured by AT command.

The battery level is monitored by the software (but not the temperature)

3.16.2 Li-Ion charging algorithm

The Li-Ion algorithm provides battery temperature monitoring, which is highly recommended to prevent battery damage during the charging phase.

The Li-Ion charger algorithm may be configured into three phases:

1. Constant charge
2. Start of pulse charge
3. End of pulse charge

The three phases can be seen in the following waveform diagram for full-charging:

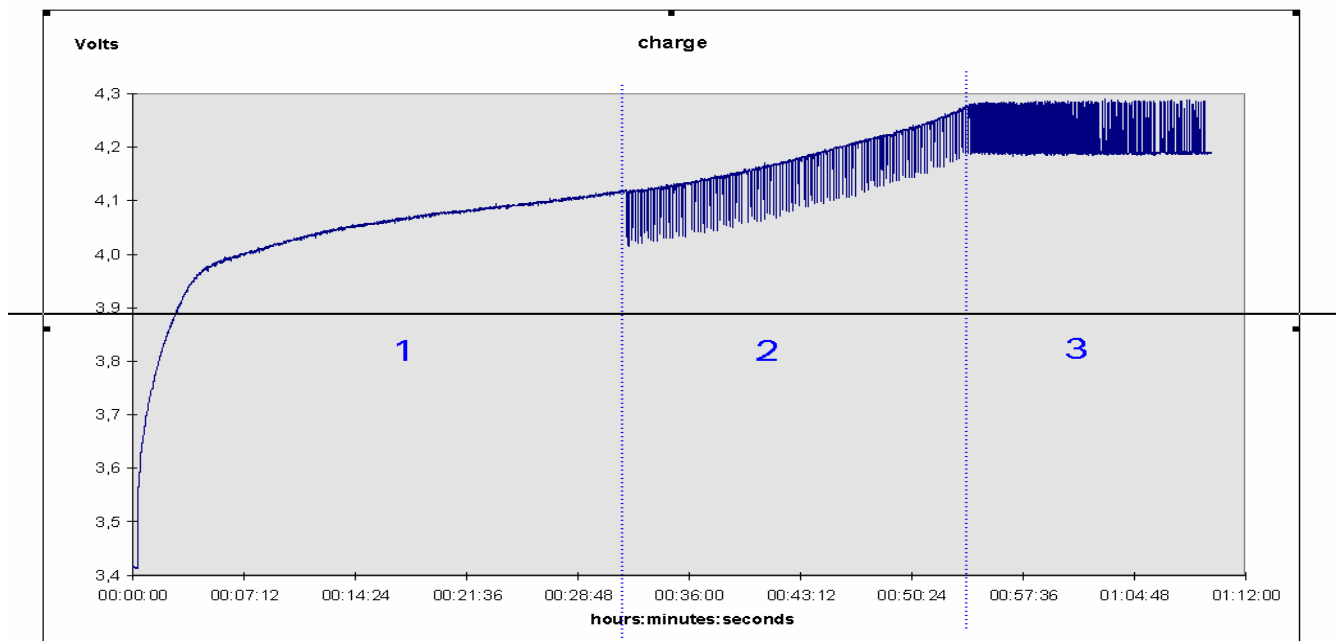


Figure 7: Li-Ion full-charging waveform

Electrical Characteristics of Li-Ion battery timing charge

Parameter		Min	Typ	Max	Unit
Step 1 switching	Closed		Always		s
Step 2 switching	Open		0.1		s
	Closed		1		s
Step 3 switching	Open	0.1		10	s
	Closed		1		s

3.16.3 Controlled pre-charging hardware

The pre-charging mode which is hardware controlled (but not the software controlled) is also available. This mode is only activated when the Wireless CPU is

Interfaces

OFF and when VBATT is in the voltage range of $2.8V < VBATT < 3.2V$. The charger power supply must be connected to CHG-IN (pin 6,8). In pre-charging mode, the battery is charged with a direct current of 50mA. The FLASH-LED blinks, when this mode is activated.

This mode is not a real charging mode as it is not possible to obtain a full charge with it, but it is useful to save the battery life by preventing the battery from being discharged to below the low limit voltage value.

3.16.4 Temperature monitoring

Temperature monitoring is only available for the Li-Ion battery with algorithm 1. The BAT-TEMP (pin 20) ADC input must be used to sample the temperature analog signal provided by an NTC temperature sensor. The minimum and maximum temperature range may be set by AT command.

Pin description of battery charging interface

Signal	Pin number	I/O	I/O type	Description
CHG-IN	6,8	I	Analog	Current source input
BAT-TEMP	20	I	Analog	A/D converter

Electrical characteristics of battery charging interface

Parameter		Minimum	Typ	Maximum	Unit
Charging operating temperature		0		50	°C
BAT-TEMP (pin 20)	Resolution		10		bits
	Sampling rate		216		S/s
	Input Impedance (R)		1M		Ω
	Input signal range	0		2	V

Interfaces

Parameter		Minimum	Typ	Maximum	Unit
CHG-IN (pin 6, 8)	Voltage (for I=I _{max})	4.6*			V
	Voltage (for I=0)			6*	V
	Current I _{max}			800	mA

* To be configured as specified by the battery manufacturer

3.17 ON / ~OFF signal

This input is used to switch the Wireless CPU Quik Q2687 ON or OFF.

A high-level signal must be provided on the ON/~OFF pin to switch ON the Wireless CPU. The voltage of this signal must be maintained for a minimum of 2000ms. This signal may be left at high level until it is switched off.

To switch OFF the Wireless CPU, the ON/OFF pin must be released. The Wireless CPU may be switched off via the Operating System.

3.17.1 Operating sequences

3.17.1.1 Power ON

Once the Wireless CPU is supplied, the application must set the ON/OFF signal to high to start the Wireless CPU power ON sequence. The ON/OFF signal must be held for 2000ms minimum. After this period, an internal mechanism keeps it on hold. During the power ON sequence, an internal reset is automatically performed by the Wireless CPU for 40ms (typical). During this phase, any external reset should be avoided. Once initialization is complete (timing is SIM- and network-dependent), the AT interface answers "OK" to the application. For further details, please check the AT Commands Interface Guide.

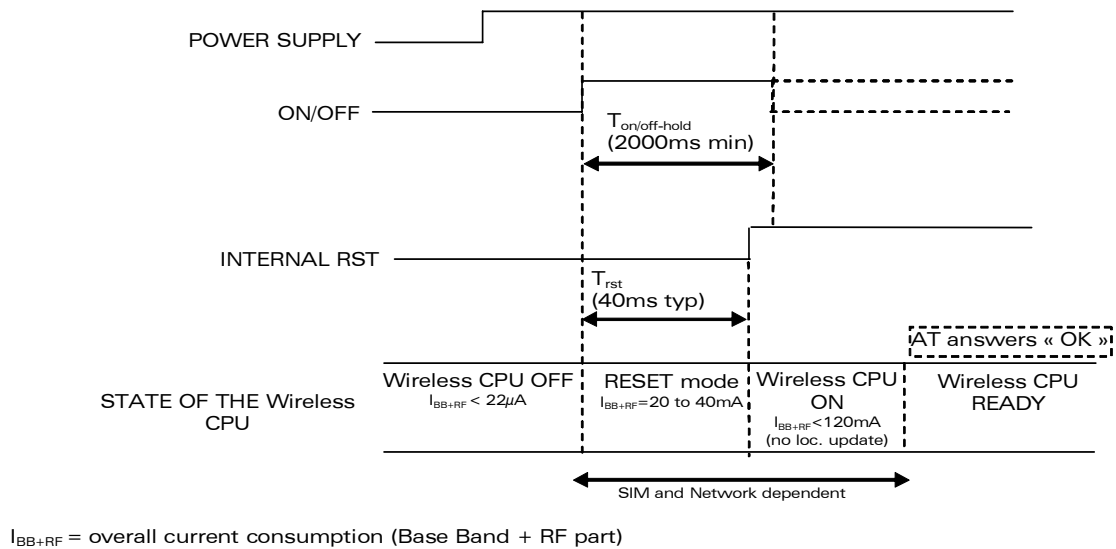


Figure 8 : Power-ON sequence (no PIN code activated)

3.17.1.2 Power OFF

To power OFF the Wireless CPU correctly, the application must set the ON/OFF signal to low and then send the AT+CPOF command to de-register from the network and switch OFF the Wireless CPU. Once the "OK" response is issued by the Wireless CPU, the power supply may be switched off.

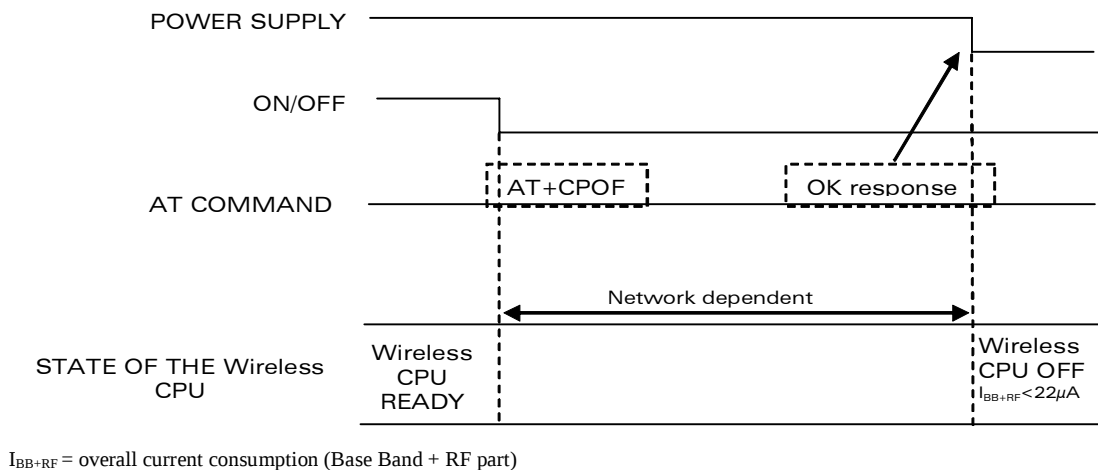


Figure 9 : Power-OFF sequence

Pin description

Signal	Pin number	I/O	I/O type	Description
ON/~OFF	19	I	CMOS	Wireless CPU Power ON

Electrical characteristics of the signal

Parameter	I/O type	Minimum	Maximum	Unit
V_{IL}	CMOS		$VBATT \times 0.2$	V
V_{IH}	CMOS	$VBATT \times 0.8$	$VBATT$	V

3.18 BOOT signal

A specific BOOT control pin is available to download the Wireless CPU Quik Q2687 (only if the standard Xmodem download, controlled with AT command, is not possible).

A specific PC software program, provided by Wavecom, is needed to perform this specific download.

The BOOT pin must be connected to VCC_1V8 for this specific download.

Operating mode description

BOOT	Operating mode	Comment
Leave open	Normal use	No download
Leave open	Download XMODEM	AT command for Download AT+WDWL
1	Download specific	Need Wavecom PC software

For more information, see AT Commands Interface Guide for OS6.61 [4].

This BOOT pin must be left open for normal use or to download Xmodem.

However, in order to render the development and maintenance phases easier, it is **highly recommended** to set a test point, either a jumper or a switch on the VCC_1V8 (pin 5) power supply.

Pin description

Signal	Pin number	I/O	I/O type	Description
BOOT	16	I	1V8	Download mode selection

3.19 Reset signal (~RESET)

This signal is used to force a reset procedure by providing low level for at least 200 μ s. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power up only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven either by an open collector or an open drain.

The Wireless CPU remains in reset mode as long as the ~RESET signal is held low.

Caution

This signal should only be used for "emergency" resets.

An Operating System reset is preferred to a hardware reset.

Reset sequence:

To activate the "emergency" reset sequence, the ~RESET signal has to be set to low for 200 μ s minimum. Once the reset is completed, the AT interface answers "OK" to the application.

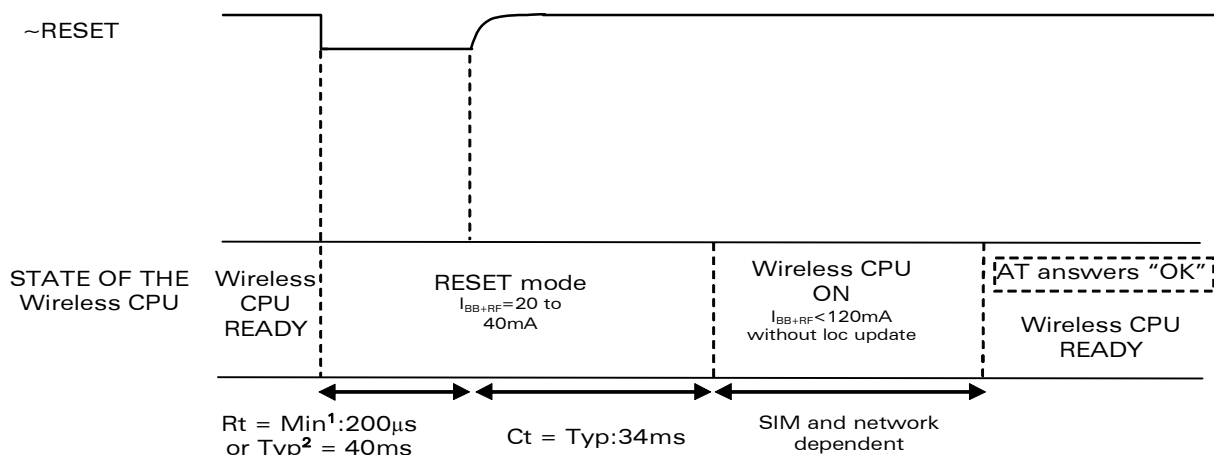


Figure 10: Reset sequence waveform

At power-up, the ~RESET time (R_t) is carried out after switching ON the Wireless CPU. It is generated by the internal voltage supervisor.

The ~RESET time is provided by the internal RC component. In order to keep the same time, avoid connecting another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

C_t is the cancellation time required for Wireless CPU initialization. C_t is automatically carried out by after hardware reset.

Electrical characteristics of the signal

Parameter	Minimum	Typ	Maximum	Unit
Input Impedance (R)*		330K		Ω
Input Impedance (C)		10n		F
~RESET time (Rt) ¹	200			μ s
~RESET time (Rt) ² at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V _H	0.57			V
V _{IL}	0		0.57	V
V _{IH}	1.33			V

* Internal pull-up

* V_H: Hysterisis Voltage

1 This reset time is the minimum to be carried out on the ~RESET signal when the power supply is already stable.

2 This reset time is internally carried out by the Wireless CPU power supply supervisor only when the Wireless CPU power supplies are powered ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
~RESET	18	I/O Open Drain	1V8	Wireless CPU Reset

3.20 External interrupt

The Wireless CPU Quik Q2687 provides two external interrupt inputs. These interrupt inputs may be activated on:

- High to low edge
- Low to high edge
- Low to high and high to low edge
- Low level
- High level

When used, the interrupt inputs must not be left open.

If not used, they must be configured as GPIOs.

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
INT1	49	I	2V8	Z	External Interrupt	GPIO25
INT0	50	I	1V8	Z	External Interrupt	GPIO3

See Section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical characteristics of the signals

Parameter		Minimum	Maximum	Unit
INT1	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT0	V_{IL}		0.54	V
	V_{IH}	1.33		V

3.21 VCC_2V8 and VCC_1V8 output

These outputs may only be used to connect pull-up resistor. VCC_2V8 and VCC_1V8 must be used as a reference supply. These voltages supplies are available when the Wireless CPU is ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
VCC_2V8	10	O	Supply	Digital supply
VCC_1V8	5	O	Supply	Digital supply

Electrical characteristics of the signals

Parameter		Minimum	Typ	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.76	1.8	1.94	V
	Output Current			15	mA

3.22 BAT-RTC (Back-up Battery)

The Wireless CPU Quik Q2687 provides an input/output to connect a Real Time Clock (RTC) power supply.

3.22.1 Interface description

This pin is used as a back-up power supply for the internal Real Time Clock (RTC). The RTC is supported by the Wireless CPU when VBATT is available, but a back-up power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

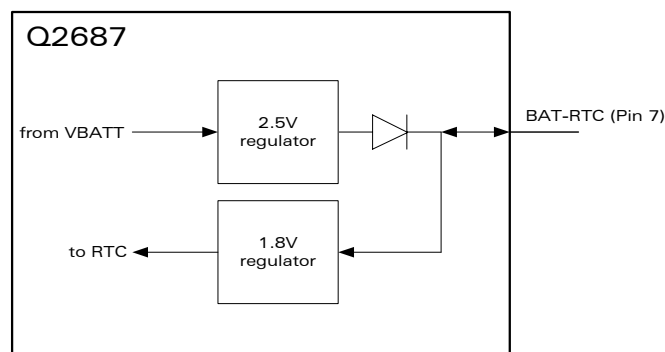


Figure 11: Real Time Clock power supply

If the RTC is not used, this pin may be left open.

If VBATT is available, the back-up battery may be charged by the internal 2.5V power supply regulator.

Pin description

Signal	Pin number	I/O	I/O type	Description
BAT-RTC	7	I/O	Supply	RTC Back-up supply

Electrical characteristics of the signal

Parameter	Minimum	Typ	Maximum	Unit
Input voltage	1.85		2.5	V
Input current consumption*	3.0	3.3	3.6	μ A
Output voltage	2.40	2.45	2.50	V
Output current			2	mA

*Provided by an RTC back-up battery when Wireless CPU power supply is OFF (VBATT = 0V).

3.23 FLASH-LED signal

FLASH-LED is an open drain output. An LED and a resistor may be directly connected between this output and VBATT.

When the Q2687 Wireless CPU is OFF, if $2.8V < VBATT < 3.2V$ and a charger is connected on CHG-IN inputs, this output flashes (100 ms ON, 900 ms OFF) to indicate the pre-charging phase of the battery.

When the Q2687 Wireless CPU is ON, this output is used to indicate network status.

FLASH-LED status

Q2687 state	VBATT status	FLASH-LED status	Wireless CPU Quik Q2687 status
Wireless CPU OFF	$VBATT < 2.8V$ or $VBATT > 3.2V$	OFF	Wireless CPU is OFF
	$2.8V < VBATT < 3.2V$	Pre-charge flash LED ON for 100 ms, OFF for 900 ms	Wireless CPU is OFF, Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
Wireless CPU ON	$VBATT > 3.2V$	Permanent	Wireless CPU switched ON, not registered on the network
		Slow flash LED ON for 200 ms, OFF for 2 s	Wireless CPU switched ON, registered on the network
		Quick flash LED ON for 200 ms, OFF for 600 ms	Wireless CPU switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Wireless CPU switched ON, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description
FLASH-LED	17	O	Open Drain Output	1 and Undefined	LED driving

See Section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

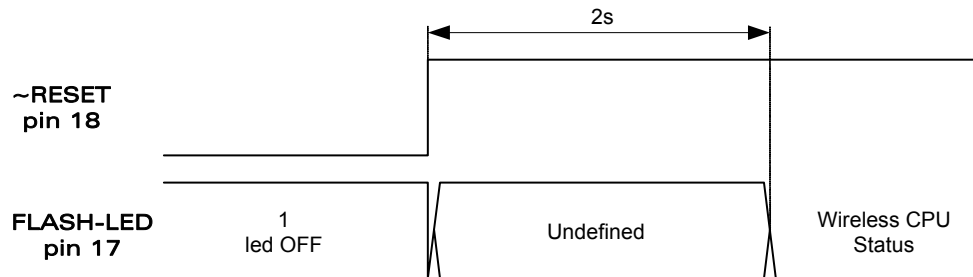


Figure 12: FLASH-LED state during RESET and Initialization time

FLASH-LED state is high during the RESET time and undefined during the software initialization time. During software initialization time, for 2 seconds max after RESET cancellation, the FLASH-LED signal is toggling and does not provide Wireless CPU status. After the 2s period, the FLASH-LED provides the true status of the Wireless CPU.

Electrical characteristics of the signal

Parameter	Condition	Minimum	Typ	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

3.24 Digital audio interface (PCM)

Digital audio interface (PCM) mode allows connectivity with audio standard peripherals. It may be used, for example, to connect an external audio codec.

The programmability of this mode allows to address a large range of audio peripherals.

PCM features:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 0
- Bit rate single clock mode at 768KHz only
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push-pull configuration on PCM-OUT and PCM-IN

The digital audio interface configuration cannot differ from the above specified features.

3.24.1 Description

The PCM interface consists of 4 wires:

- **PCM-SYNC** (output): The frame synchronization signal delivers an 8KHz frequency pulse that synchronizes the frame data in and the frame data out.
- **PCM-CLK** (output): The frame bit clock signal controls data transfer with the audio peripheral.
- **PCM-OUT** (output): The frame "data out" relies on the selected configuration mode.
- **PCM-IN** (input): The frame "data in" relies on the selected configuration mode.

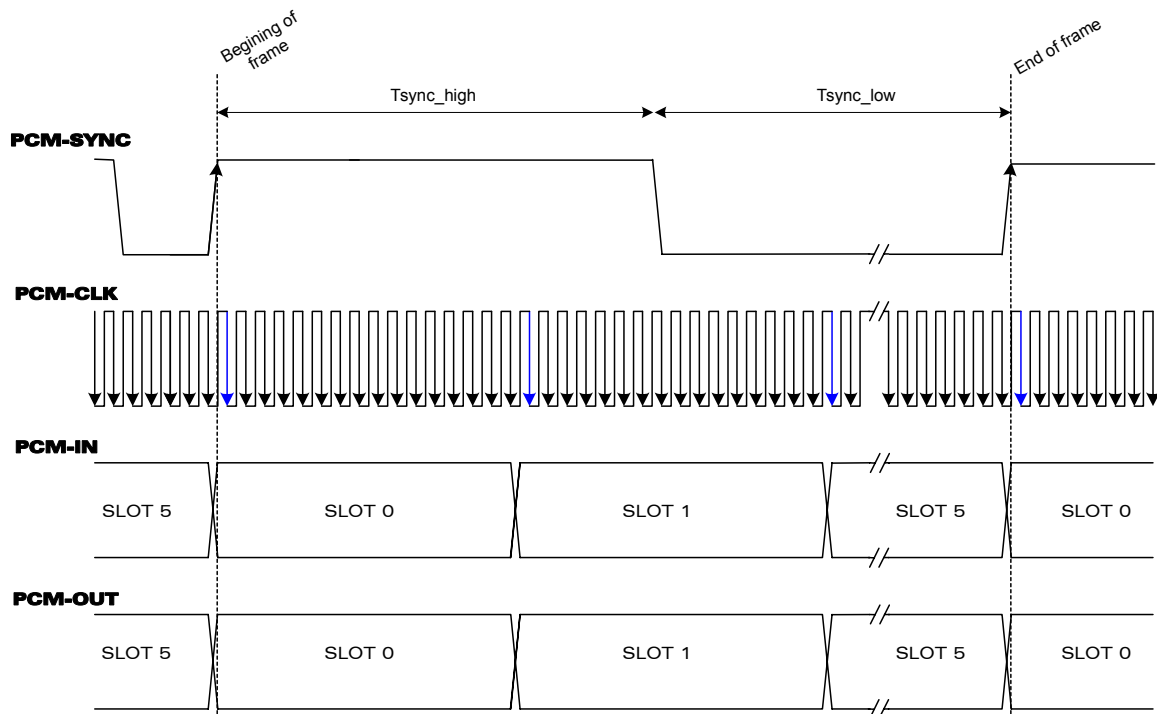


Figure 13: PCM frame waveform

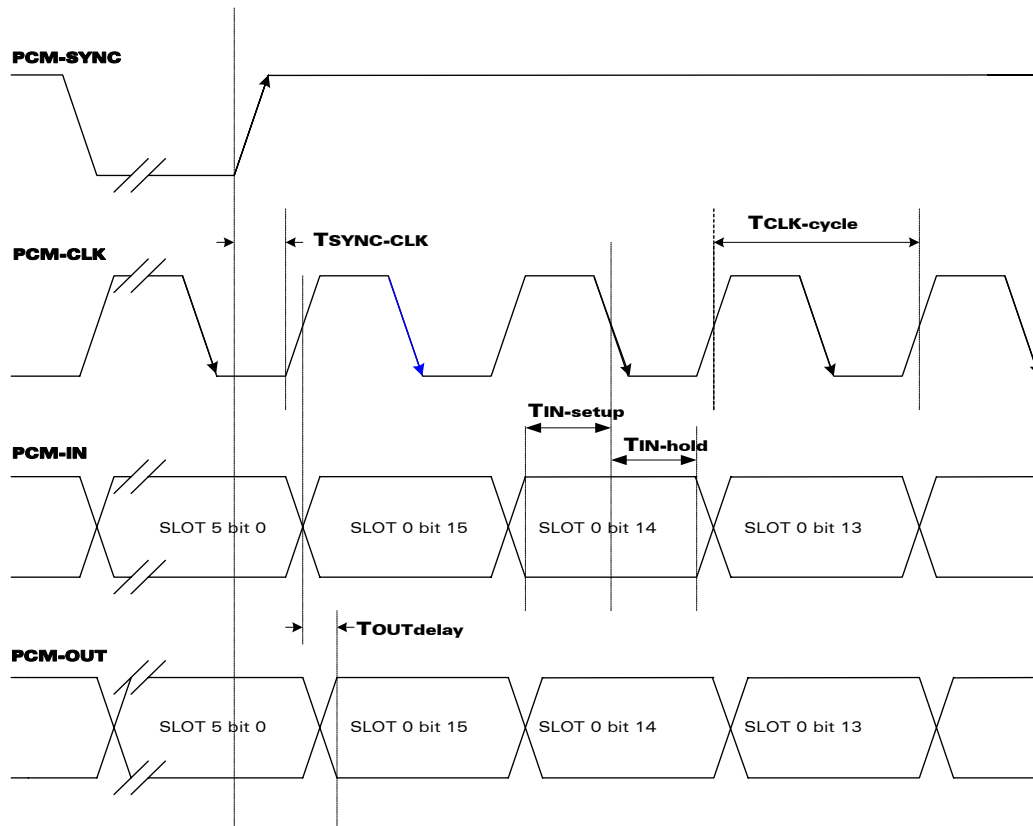


Figure 14: PCM sampling waveform

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
$T_{sync_low} + T_{sync_high}$	PCM-SYNC period		125		μs
T_{sync_low}	PCM-SYNC low time		93		μs
T_{sync_high}	PCM-SYNC high time		32		μs
T_{sync_CLK}	PCM-SYNC to PCM-CLK time		-154		Ns
$T_{CLK-cycle}$	PCM-CLK period		1302		Ns
$T_{IN-setup}$	PCM-IN setup time	50			Ns
$T_{IN-hold}$	PCM-IN hold time	50			Ns
$T_{OUT-delay}$	PCM-OUT delay time			20	Ns

Pin description of the PCM interface

Signal	Pin number	I/O	I/O type	Reset state	Description
PCM-SYNC	77	O	1V8	Pull-down	Frame synchronization 8Khz
PCM-CLK	79	O	1V8	Pull-down	Data clock
PCM-OUT	80	O	1V8	Pull-up	Data output
PCM-IN	78	I	1V8	Pull-up	Data input

See Section 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.25 USB 2.0 interface

A 4-wire USB slave interface is available that complies with USB 2.0 protocol signaling. But it is not compliant with the electrical interface, due to the 5V of VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM, and GND.

USB interface features:

- 12Mbit/s full-speed transfer rate
- 3.3V typ compatible
- USB Softconnect feature
- Download feature is not supported by USB
- CDC 1.1 – ACM compliant

Note:

A 5V to 3.3V typ voltage regulator is needed between the external interface power inline (+5V) and the Wireless CPU line (VPAD-USB).

Pin description of the USB interface

Signal	Pin number	I/O	I/O type	Description
VPAD-USB	52	I	VPAD_USB	USB Power Supply
USB-DP	54	I/O	VPAD_USB	Differential data interface positive
USB-DM	56	I/O	VPAD_USB	Differential data interface negative

Electrical characteristics of the signals

Parameter	Min	Typ	Max	Unit
VPAD-USB, USB-DP, USB-DM	3	3.3	3.6	V

3.26 RF interface

The impedance is 50 Ohms nominal and the DC impedance is 0 Ohm.

3.26.1 RF connections

U.FL Connector

A wide variety of cables fitted with U.FL connectors is offered by different suppliers.

Soldered solution

The soldered solution will preferably be based on an RG178 coaxial cable.

IMP connector

This connector is dedicated to board-to-board applications and must be soldered on the customer board. The supplier is Radiall (reference: R107 064 900).

Notes:

- The Wireless CPU Quik Q2687 does not support an antenna switch for a car kit but this function may be implemented externally and may be driven using a GPIO.
- The antenna cable and connector should be selected in order to minimize losses in the frequency bands used for GSM 850/900MHz and 1800/1900MHz.
- 0.5dB may be considered as the maximum value of loss between the Wireless CPU and an external connector.
- For mounting, assembling and handling of the IMP connector, contact the supplier, Radiall, directly. Wavecom may not provide customer support for use of this connector.

3.26.2 RF performance

RF performance is compliant with the ETSI GSM 05.05 recommendation.

The main Receiver parameters are:

- GSM850 Reference Sensitivity = -104 dBm Static & TUHigh
- E-GSM900 Reference Sensitivity = -104 dBm Static & TUHigh
- DCS1800 Reference Sensitivity = -102 dBm Static & TUHigh
- PCS1900 Reference Sensitivity = -102 dBm Static & TUHigh
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

Transmitter parameters:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature

3.26.3 Antenna specifications

The antenna must meet the following requirements as specified in the table below:

- The optimum operating frequency depends on the application. Either a dual-band or a quad-band antenna may operate in these frequency bands and must have the following characteristics:

Characteristic		Q2687			
		E-GSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50 Ohms			
VSWR	Rx max	1.5:1			
	Tx max	1.5:1			
Typical radiated gain		0dBi in one direction at least			

Caution:

Q2687 and Q2686 are compatible, nevertheless, if intends to use Q2686 be careful on these specific differences

Wireless CPU Quik Q2687

Interfaces

Pin #	Q2686		Q2687	
	Signal Name	Multiplexed with	Signal Name	Multiplexed with
42	Reserved	-	A1	Not mux
51	GPIO1	Not mux	GPIO1	~CS2/A25
53	GPIO2	Not mux	GPIO2	A24
82	Reserved	-	AUX-DAC	Not mux

4 Technical specifications

4.1 General Purpose Connector pin-out description

Pin Number	Signal Name		I/O type	Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux						
1	VBATT			VBATT	I		Power Supply	
2	VBATT			VBATT	I		Power Supply	
3	VBATT			VBATT	I		Power Supply	
4	VBATT			VBATT	I		Power Supply	
5	VCC_1V8			VCC_1V8	O		1.8V Supply Output	NC
6	CHG-IN			CHG-IN	I		Charger input	NC
7	BAT-RTC			BAT-RTC	I/O		RTC Battery connection	NC
8	CHG-IN			CHG-IN	I		Charger input	NC
9	SIM-VCC			1V8 or 3V	O		SIM Power Supply	
10	VCC_2V8			VCC_2V8	O		2.8V Supply Output	NC
11	SIM-IO			1V8 or 3V	I/O	Pull-up (about 10K)	SIM Data	
12	SIMPRES	GPIO18	C1	VCC_1V8	I	Z	SIM Detection	NC
13	~SIM-RST			1V8 or 3V	O	0	SIM reset Output	
14	SIM-CLK			1V8 or 3V	O	0	SIM Clock	
15	BUZZ-OUT		A1	Open Drain	O	Z	Buzzer Output	NC
16	BOOT			VCC_1V8	I		Not Used	Add a test point / a jumper/ a switch to VCC_1V8 (Pin 5) in case Download Specific mode is used (See product specification for details)
17	FLASH-LED		A1	Open Drain	O	1 and Undefined	Flash Led Output	NC
18	~RESET		C4	VCC_1V8	I/O		RESET Input	NC or add a test point
19	ON/~OFF			VBATT	I		ON / ~OFF Control	
20	BAT-TEMP		A3	Analog	I		Analog temperature	Pull to GND
21	AUX-ADC		A2	Analog	I		Analog to Digital	Pull to GND

Technical specifications

Pin Number	Signal Name		I/O type	Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux						
							Input	
22	~SPI1-CS	GPIO31	C1	VCC_2V8	O	Z	SPI1 Chip Select	NC
23	SPI1-CLK	GPIO32	C1	VCC_2V8	O	Z	SPI1 Clock	NC
24	SPI1-I	GPIO30	C1	VCC_2V8	I	Z	SPI1 Data Input	NC
25	SPI1-IO	GPIO29	C1	VCC_2V8	I/O	Z	SPI1 Data Input / Output	NC
26	SPI2-CLK	GPIO32	C1	VCC_2V8	O	Z	SPI2 Clock	NC
27	SPI2-IO	GPIO33	C1	VCC_2V8	I/O	Z	SPI2 Data Input / Output	NC
28	~SPI2-CS	GPIO35	C1	VCC_2V8	O	Z	SPI2 Chip Select	NC
29	SPI2-I	GPIO34	C1	VCC_2V8	I	Z	SPI2 Data Input	NC
30	CT104-RXD2	GPIO15	C1	VCC_1V8	O	Z	Auxiliary RS232 Receive	Add a test point for firmware upgrade
31	CT103-TXD2	GPIO14	C1	VCC_1V8	I	Z	Auxiliary RS232 Transmit	(TXD2) Pull-up to VCC_1V8 with 100kΩ and add a test point for firmware update
32	~CT106-CTS2	GPIO16	C1	VCC_1V8	O	Z	Auxiliary RS232 Clear To Send	(CTS2) Add a test point for firmware update
33	~CT105-RTS2	GPIO17	C1	VCC_1V8	I	Z	Auxiliary RS232 Request To Send	(RTS2) Pull-up to VCC_1V8 with 100kΩ and add a test point for firmware update
34	MIC2N		A4	Analog	I		Micro 2 Input Negative	NC
35	SPK1P		A5	Analog	O		Speaker 1 Output Positive	NC
36	MIC2P		A4	Analog	I		Micro 2 Input Positive	NC
37	SPK1N		A5	Analog	O		Speaker 1 Output Negative	NC
38	MIC1N		A4	Analog	I		Micro 1 Input Negative	NC
39	SPK2P		A5	Analog	O		Speaker 2 Output Positive	NC
40	MIC1P		A4	Analog	I		Micro 1 Input Positive	NC
41	SPK2N		A5	Analog	O		Speaker 2 Output Negative	NC
42	A1			VCC_1V8	O		Address bus 1	NC
43	GPIO44		C1	VCC_2V8	I/O	Undefined		NC
44	SCL	GPIO26	A1	Open Drain	O	Z	I ² C Clock	NC

Wireless CPU Quik Q2687

Technical specifications

Pin Number	Signal Name		I/O type	Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux						
45	GPIO19		C1	VCC_2V8	I/O	Z		NC
46	SDA	GPIO27	A1	Open Drain	I/O	Z	I ² C Data	NC
47	GPIO21		C1	VCC_2V8	I/O	Undefined		NC
48	GPIO20		C1	VCC_2V8	I/O	Undefined		NC
49	INT1	GPIO25	C1	VCC_2V8	I	Z	Interruption 1 Input	If INT1 is not used, it should be configured as GPIO
50	INT0	GPIO3	C1	VCC_1V8	I	Z	Interruption 0 Input	If INT0 is not used, it should be configured as GPIO
51	GPIO1	**	C1	VCC_1V8	I/O	Undefined		NC
52	VPAD-USB			VPAD-USB	I		USB Power supply input	NC
53	GPIO2	**	C1	VCC_1V8	I/O	Undefined		NC
54	USB-DP			VPAD-USB	I/O		USB Data	NC
55	GPIO23	**	C1	VCC_2V8	I/O	Z		NC
56	USB-DM			VPAD-USB	I/O		USB Data	NC
57	GPIO22	**	C1	VCC_2V8	I/O	Z		NC
58	GPIO24		C1	VCC_2V8	I/O	Z		NC
59	COL0	GPIO4	C8	VCC_1V8	I/O	Pull-up	Keypad column 0	NC
60	COL1	GPIO5	C8	VCC_1V8	I/O	Pull-up	Keypad column 1	NC
61	COL2	GPIO6	C8	VCC_1V8	I/O	Pull-up	Keypad column 2	NC
62	COL3	GPIO7	C8	VCC_1V8	I/O	Pull-up	Keypad column 3	NC
63	COL4	GPIO8	C8	VCC_1V8	I/O	Pull-up	Keypad column 4	NC
64	ROW4	GPIO13	C7	VCC_1V8	I/O	0	Keypad Row 4	NC
65	ROW3	GPIO12	C7	VCC_1V8	I/O	0	Keypad Row 3	NC
66	ROW2	GPIO11	C7	VCC_1V8	I/O	0	Keypad Row 2	NC
67	ROW1	GPIO10	C7	VCC_1V8	I/O	0	Keypad Row 1	NC
68	ROW0	GPIO9	C7	VCC_1V8	I/O	0	Keypad Row 0	NC
69	~CT125-RI	GPIO42	C1	VCC_2V8	O	Undefined	Main RS232 Ring Indicator	NC
70	~CT109-DCD1	GPIO43	C1	VCC_2V8	O	Undefined	Main RS232 Data Carrier Detect	NC
71	CT103-TXD1	GPIO36	C1	VCC_2V8	I	Z	Main RS232 Transmit	(TXD1) Pull-up to VCC_2V8 with 100kΩ and add a test point for

Wireless CPU Quik Q2687

Technical specifications

Pin Number	Signal Name		I/O type	Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux						
								firmware update
72	~CT105-RTS1	GPIO38	C1	VCC_2V8	I	Z	Main RS232 Request To Send	(RTS1) Pull-up to VCC_2V8 with 100kΩ and add a test point for firmware update
73	CT104-RXD1	GPIO37	C1	VCC_2V8	O	1	Main RS232 Receive	(RXD1) Add a test point for firmware update
74	~CT107-DSR1	GPIO40	C1	VCC_2V8	O	Z	Main RS232 Data Set Ready	NC
75	~CT106-CTS1	GPIO39	C1	VCC_2V8	O	Z	Main RS232 Clear To Send	(CTS1) Add a test point for firmware update
76	~CT108-2-DTR1	GPIO41	C1	VCC_2V8	I	Z	Main RS232 Data Terminal Ready	(DTR1) Pull-up to VCC_2V8 with 100kΩ
77	PCM-SYNC			VCC_1V8	O	Pull-down	PCM Frame Synchro	NC
78	PCM-IN		C5	VCC_1V8	I	Pull-up	PCM Data Input	NC
79	PCM-CLK			VCC_1V8	O	Pull-down	PCM Clock	NC
80	PCM-OUT			VCC_1V8	O	Pull-up	PCM Data Output	NC
81	/OE-R/W			VCC_1V8	O		Output Enable/Read not write	NC
82	AUX-DAC			Analog	O		Digital to Analog Output	NC
83	/CS3			VCC_1V8	O		Chip Select 3	NC
84	/WE-E			VCC_1V8	O		Write Enable	NC
85	D0			VCC_1V8	I/O		Data for Peripheral	NC
86	D15			VCC_1V8	I/O		Data for Peripheral	NC
87	D1			VCC_1V8	I/O		Data for Peripheral	NC
88	D14			VCC_1V8	I/O		Data for Peripheral	NC
89	D2			VCC_1V8	I/O		Data for Peripheral	NC
90	D13			VCC_1V8	I/O		Data for Peripheral	NC
91	D3			VCC_1V8	I/O		Data for Peripheral	NC
92	D12			VCC_1V8	I/O		Data for Peripheral	NC
93	D4			VCC_1V8	I/O		Data for Peripheral	NC
94	D11			VCC_1V8	I/O		Data for Peripheral	NC
95	D5			VCC_1V8	I/O		Data for Peripheral	NC
96	D10			VCC_1V8	I/O		Data for Peripheral	NC

Technical specifications

Pin Number	Signal Name		I/O type	Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux						
97	D6			VCC_1V8	I/O		Data for Peripheral	NC
98	D9			VCC_1V8	I/O		Data for Peripheral	NC
99	D7			VCC_1V8	I/O		Data for Peripheral	NC
100	D8			VCC_1V8	I/O		Data for Peripheral	NC

* The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

** For more information about the multiplexing of these signals, see "General purpose input/output", Section 3.10

4.2 I/O Circuit Diagram

The following tables and drawings shown are the internal interface of the Wireless CPU Quik Q2687.

4.2.1 Digital I/O - 2.8 Volts CMOS

Operating conditions:

Parameter	I/O type	Min	Typ	Max	Condition
2V8		2.74V	2.8V	2.86V	
V _{IL}	CMOS			0.84V	
V _{IH}	CMOS	1.96V			
V _{OL}	CMOS			0.4V	I _{OL} = -4mA
V _{OH}	CMOS	2.4V			I _{OL} = 4mA
I _{OH}				4mA	
I _{OL}				-4mA	

4.2.2 Digital I/O - 1.8 Volts CMOS

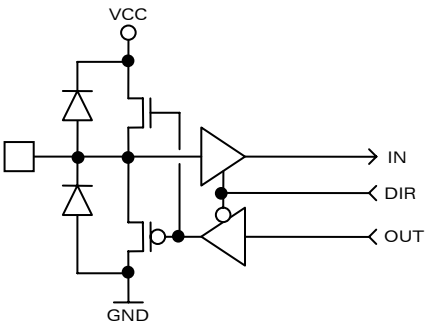
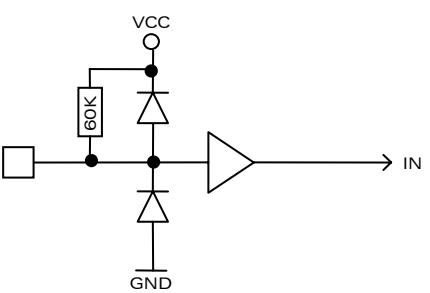
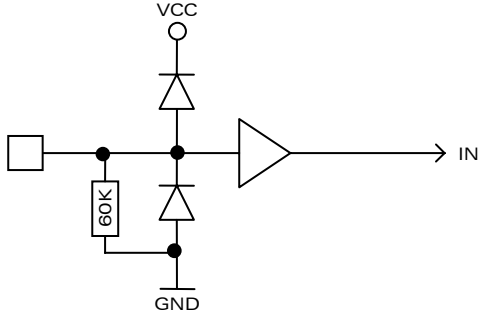
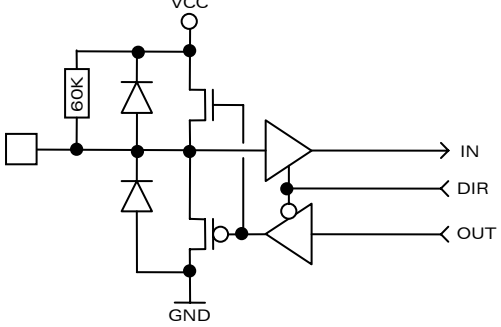
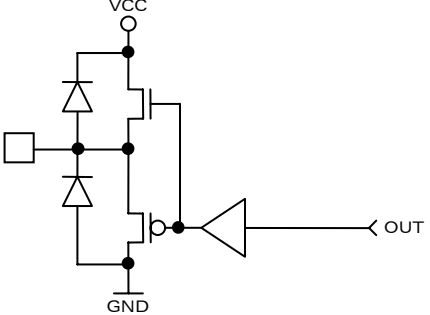
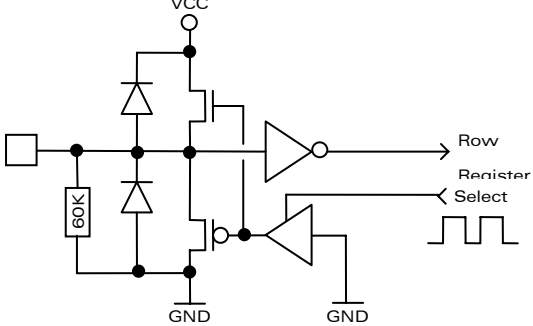
Operating conditions:

Parameter	I/O type	Min	Typ	Max	Condition
1V8		1.76V	1.8V	1.94V	
V _{IL}	CMOS			0.54V	
V _{IH}	CMOS	1.33V			
V _{OL}	CMOS			0.4V	I _{OL} = -4mA
V _{OH}	CMOS	1.4V			I _{OL} = 4mA

Technical specifications

Parameter	I/O type	Min	Typ	Max	Condition
I _{OH}				4mA	
I _{OL}				-4mA	

4.2.3 CMOS

Type	Circuit	Type	Circuit
C1	 For RS232 setting see Figure 15	C5	
C2		C6	
C3		C7	

Technical specifications

Type	Circuit	Type	Circuit
C4		C8	See Figure 16

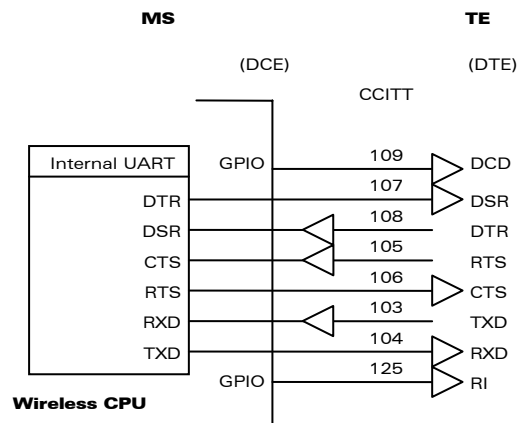


Figure 15: UART internal configuration

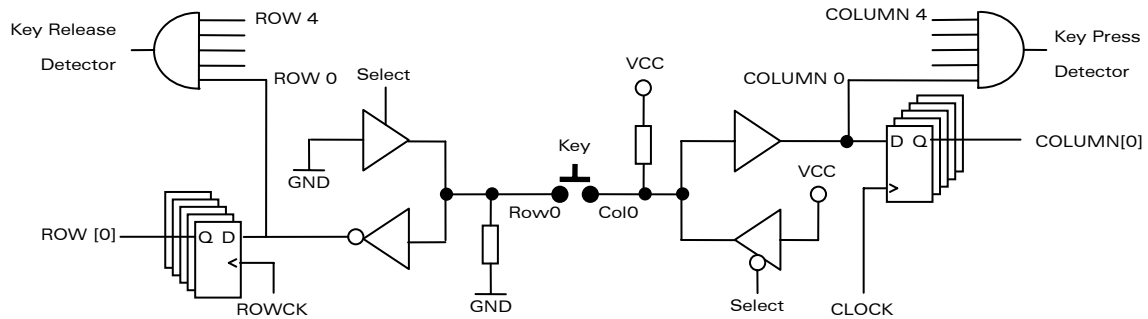


Figure 16: Keyboard internal configuration

4.2.4 Analog

Type	Circuit	Type	Circuit
A1		A4	
A2		A5	
A3			

4.3 Environmental Specifications

Wavecom specifies the following temperature range for the Q2687 product.

The Q2687 Wireless CPU is compliant with the following operating class.

Conditions	Temperature range
Operating / Class A	-20 °C to +55°C
Operating / Storage / Class B	-40 °C to +85°C

Function Status Classification:

Class A:

The Wireless CPU remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

Class B:

The Wireless CPU remains fully functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements and this deviation does not affect the ability of the Wireless CPU to connect to the cellular network and fully functional, as it does within the Class A range.

Wireless CPU Quik Q2687

Technical specifications

Q2687		ENVIRONNEMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Figure 17: Environmental classes

4.4 Mechanical specifications

4.4.1 Physical characteristics

The Wireless CPU Quik Q2687 has a complete self-contained shield.

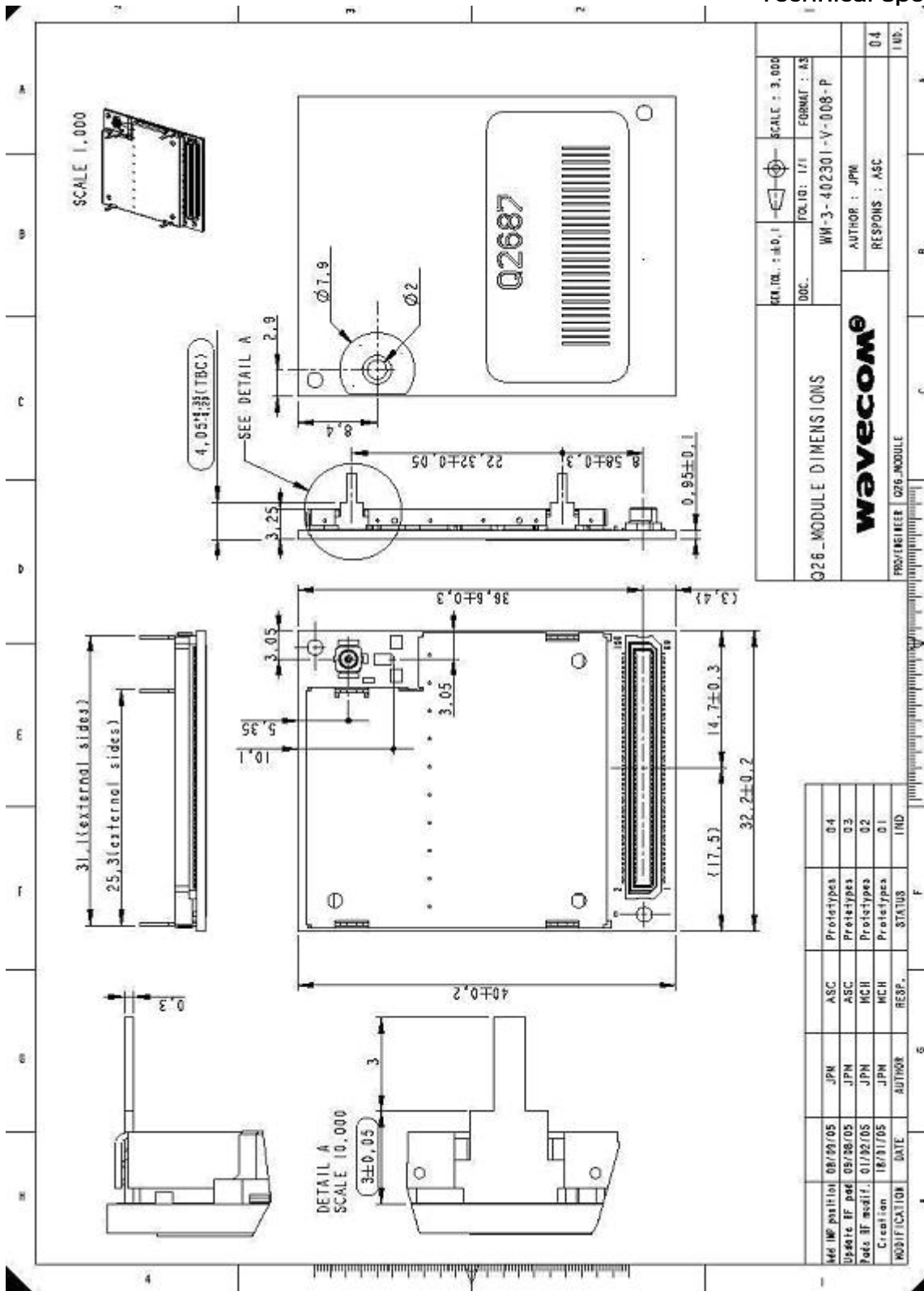
- Overall dimensions : 32.2x40x4 mm (except shielding pins)
- Weight : <10 g

4.4.2 Mechanical drawings

The mechanical specifications of the Wireless CPU Quik Q2687 are shown on the following page.

Wireless CPU Quik Q2687

Technical specifications



5 Connector and peripheral device references

5.1 General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the PANASONIC Group's P5K series, with the following reference:

AXK69510002

The matting connector has the following reference:

AXK59510001

The stacking height is 3.0 mm.

Wavecom recommends that you use the **AXK59510001** connector for your application to benefit from Wavecom's prices. For more information, contact Wavecom, specifying the Wavecom connector reference: **WM17077**.

For further details see the GPC data sheets in the Appendix. More information is also available from <http://www.panasonic.com/host/indusrl.html>

5.2 SIM Card Reader

- ITT CANNON CCM03 series (see <http://www.ittcannon.com>)
- AMPHENOL C707 series (see <http://www.amphenol.com>)
- JAE (see <http://www.jae.com>)
- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see <http://www.molex.com>)

5.3 Microphone

Possible suppliers:

- HOSIDEN
- PANASONIC
- PEIKER

5.4 Speaker

Possible suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

5.5 Antenna Cable

A wide variety of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails, Ex: Ref = **U.FL-2LP(V)-04-A-(100)**
- UF-L Ref = **U.FL-R-SMT**
- UF-L cable assemblies,
- Between series cable assemblies.

More information is also available from <http://www.hirose-connectors.com/>.

A coaxial cable may also be soldered on the RF pad. The following references have been certified for mounting on the Q2687 Wireless CPU:

- RG178
- RG316

5.6 RF board-to-board connector

The supplier for the IMP connector is Radiall (<http://www.radiall.com>), with the following reference:

- R107 064 900.

5.7 GSM antenna

GSM antennas and support for antenna adaptation may be obtained from manufacturers such as:

- ALLGON (<http://www.allgon.com>)
- IRSCHMANN (<http://www.hirschmann.com/>)

6 Design Guidelines

The purpose of the following paragraphs is to give design guidelines.

6.1 Hardware and RF

6.1.1 EMC recommendations

The EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band
- ESD protection **is mandatory** on all signals which have external accessibility (typically human accessibility). See Q2687 Wireless CPU Customer Design Guidelines WM_DEV_Q2687_PTS_007 [2] for ESD protection samples.
 - o Similarly, ESD protection is mandatory for the:
 - SIM (if accessible from outside)
 - Serial link
- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Length of the SIM interface lines (preferably <10cm)
- Ground plane: Wavecom recommends a common ground plane for analog/digital/RF grounds.
- A metallic case or plastic casing with conductive paint are recommended

Note:

The Wireless CPU does not include any protection against over-voltage.

6.1.2 Power Supply

The power supply is one of the key issues in the design of a GSM terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- The phase error and frequency error

Warning:

Careful attention should be paid to:

- The quality of the power supply: low ripple, PFM or PSM systems should be avoided (PWM converter preferred).
- Capacity to deliver high current peaks in a short time (pulsed radio emission).

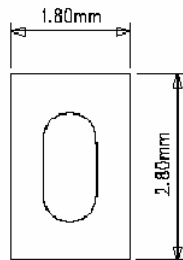
6.1.3 Layout requirement

CHIPS & BORING DIAMETER

of the WISMO QUIK mechanical insertion pins

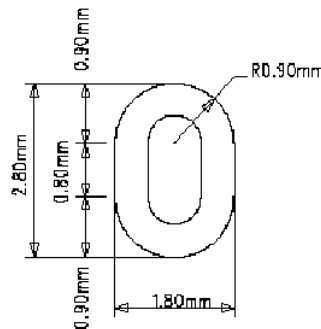
CASE N 1

To be used in priority



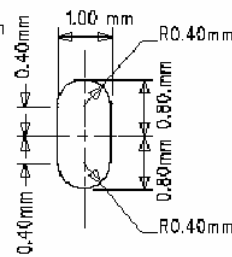
CASE N 2

on specific request



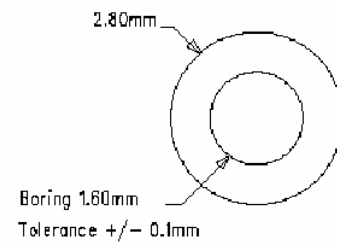
Tolerance $\pm 0.1\text{mm}$

1.00 mm reamer



CASE N 3

Other



THERMAL BRAKES DEFINITION

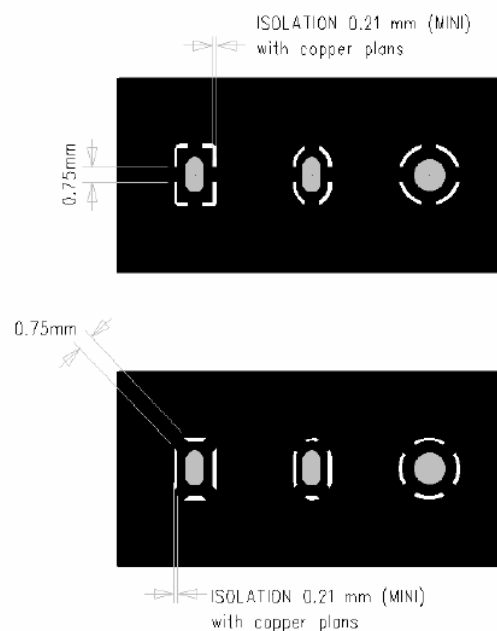


Figure 18: Layout requirement

6.1.4 Antenna

Warning:

Wavecom strongly recommends to work with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.

Both the mechanical and electrical antenna adaptation are one of the key issues in the design of GSM terminal.

6.2 Mechanical integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Leads of the Wireless CPU to be soldered to the Ground plane

6.3 Operating System upgrade

The Wireless CPU Quik Q2687 Operating System is stored in flash memory and may easily be upgraded.

IMPORTANT:

In order to follow regular changes in the GPRS standard and to offer a state-of-the-art Operating System, Wavecom recommends that the application designed around a WISMO (or WISMO based product) allow easy Operating System upgrades on the Wireless CPU via the standard Xmodem protocol. Therefore, the application shall either allow a direct access to the WISMO serial link through an external connector or implement any mechanism allowing the WISMO Operating System to be downloaded via Xmodem.

The Operating System file may be downloaded to the Wireless CPU using the Xmodem protocol. The AT+WDWL command allows the download process to be launched (see the description in the AT Command User Guide).

The serial signals required to proceed with Xmodem downloading are:

Rx, Tx, RTS, CTS and GND.

The Operating System file may also be downloaded to the Wireless CPU using the DOTA (download over the air) feature. This feature is available with the Open AT[®] interface. For more details, please, refer to the Open AT[®] documentation.

7 Appendix

7.1 Standards and Recommendations

GSM ETSI, 3GPP, GCF and NAPRD03 recommendations for Phase II & FCC.

Specification Reference	Title
3GPP TS 45.005 v5.5.0 (2002-08) Release 5	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception
GSM 02.07 V8.0.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); Mobile Stations (MS) features (GSM 02.07 version 8.0.0 Release 1999)
GSM 02.60 V8.1.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description, Stage 1 (GSM 02.60 version 8.1.0 Release 1999)
GSM 03.60 V7.9.0 (2002-09)	Technical Specification Group Services and System Aspects; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description; Stage 2 (Release 1998)
3GPP TS 43.064 V5.0.0 (2002-04)	Technical Specification Group GERAN; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Overall description of the GPRS radio interface; Stage 2 (Release 5)
3GPP TS 03.22 V8.7.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Functions related to Mobile Station (MS) in idle mode and group receive mode; (Release 1999)
3GPP TS 03.40 V7.5.0 (2001-12)	Technical Specification Group Terminals; Technical realization of the Short Message Service (SMS) (Release 1998)
3GPP TS 03.41 V7.4.0 (2000-09)	Technical Specification Group Terminals; Technical realization of Cell Broadcast Service (CBS) (Release 1998)

Appendix

Specification Reference	Title
ETSI EN 300 903 V8.1.1 (2000-11)	Digital cellular telecommunications system (Phase 2+); Transmission planning aspects of the speech service in the GSM Public Land Mobile Network (PLMN) system (GSM 03.50 version 8.1.1 Release 1999)
3GPP TS 04.06 V8.2.1 (2002-05)	Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station - Base Station System (MS - BSS) interface; Data Link (DL) layer specification (Release 1999)
3GPP TS 04.08 V7.18.0 (2002-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Mobile radio interface layer 3 specification (Release 1998)
3GPP TS 04.10 V7.1.0 (2001-12)	Technical Specification Group Core Networks; Mobile radio interface layer 3 Supplementary services specification; General aspects (Release 1998)
3GPP TS 04.11 V7.1.0 (2000-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Point-to-Point (PP) Short Message Service (SMS) support on mobile radio interface (Release 1998)
3GPP TS 45.005 v5.5.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception (Release 5)
3GPP TS 45.008 V5.8.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem link control (Release 5)
3GPP TS 45.010 V5.1.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem synchronization (Release 5)
3GPP TS 46.010 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Transcoding (Release 5)
3GPP TS 46.011 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Substitution and muting of lost frames for Full rate speech channels (Release 5)

Appendix

Specification Reference	Title
3GPP TS 46.012 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Comfort noise aspect for full rate speech traffic channels (Release 5)
3GPP TS 46.031 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Discontinuous Transmission (DTX) for full rate speech traffic channels (Release 5)
3GPP TS 46.032 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Voice Activity Detector (VAD) for full rate speech traffic channels (Release 5)
TS 100 913V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General on Terminal Adaptation Functions (TAF) for Mobile Stations (MS) (GSM 07.01 version 8.0.0 Release 1999)
GSM 09.07 V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General requirements on interworking between the Public Land Mobile Network (PLMN) and the Integrated Services Digital Network (ISDN) or Public Switched Telephone Network (PSTN) (GSM 09.07 version 8.0.0 Release 1999)
3GPP TS 51.010-1 v5.0.0 (2002-09)	Technical Specification Group GSM/EDGE ; Radio Access Network ;Digital cellular telecommunications system (Phase 2+);Mobile Station (MS) conformance specification; Part 1: Conformance specification (Release 5)
3GPP TS 51.011 V5.0.0 (2001-12)	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)
ETS 300 641 (1998-03)	Digital cellular telecommunications system (Phase 2); Specification of the 3 Volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)
GCF-CC V3.7.1 (2002-08)	Global Certification Forum – Certification criteria
NAPRD03 V2.6.0 (2002-06)	North America Permanent Reference Document for PTCRB tests

The Wireless CPU Quik Q2687 connected on a development kit board application is certified to be in accordance with the following Rules and Regulations of the Federal Communications Commission (FCC).

Power listed on the Gant is conducted for Part 22 and conducted for Part 24

This device contains GSM, GPRS Class 10 functions in the 900 and 1800MHz Band, which are not operational in U.S. Territories.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Antennas used for this OEM module must not exceed 3.3dBi gain for PCS 1900 MHz and 6dBd(8.14dBi) GSM 850 MHz for mobile and fixed operating configurations. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the RF exposure condition requires a separate equipment authorization.

The license module will have a FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:

Contains FCC ID: 09EQ2687

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- o this device may not cause harmful interference,
- o this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT:

Manufacturers of mobile or fixed devices incorporating Q2687 Wireless CPU are advised to:

- clarify any regulatory questions,
- have their completed product tested,
- have product approved for FCC compliance, and
- include instructions according to above mentioned RF exposure statements in end product user manual.

Please note that changes or modifications not stated clearly approved by the party responsible for compliance could void the user's authority to operate the equipment.

7.2 Safety recommendations (for information only)

IMPORTANT

FOR THE EFFICIENT AND SAFE OPERATION OF YOUR GSM APPLICATION BASED ON Wireless CPU Quik Q2687

PLEASE READ THIS INFORMATION CAREFULLY

7.2.1 RF safety

7.2.1.1 General

Your GSM terminal¹ is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

7.2.1.2 Exposure to RF energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

7.2.1.3 Efficient terminal operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However, your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

¹ based on WISMO2D

7.2.1.4 Antenna care and replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace the damaged antenna immediately. You may repair antenna yourself by following the instruction manual provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

7.2.2 General safety

7.2.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive, as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off the road and park before making or answering a call (if driving conditions so require).

7.2.2.2 Electronic devices

Most electronic equipments, for example in hospitals and motor vehicles are shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

7.2.2.3 Vehicle electronic equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

7.2.2.4 Medical electronic equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

7.2.2.5 Aircraft

Turn your terminal **OFF** before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you to have prior permission from the crew members to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem, while airborne.

7.2.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

7.2.2.7 Blasting areas

To avoid interfering with blasting operations, turn your unit **OFF** when in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

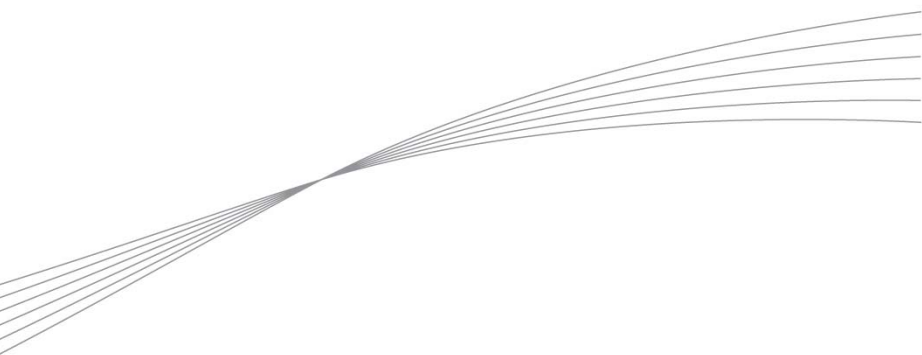
7.2.2.8 Potentially explosive atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. It is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly the marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is to be used.



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WAVECOM S.A. - 3 esplanade du Foncet - 92442 Issy-les-Moulineaux Cedex - France - Tel: +33(0)1 46 29 08 00 - Fax: +33(0)1 46 29 08 08
Wavecom, Inc. - 4810 Eastgate Mall - Second Floor - San Diego, CA 92121 - USA - Tel: +1 858 362 0101 - Fax: +1 858 558 5485
WAVECOM Asia Pacific Ltd. - Unit 201-207, 2nd Floor, Bio-Informatics Centre - No.2 Science Park West Avenue - Hong Kong Science Park, Shatin
- New Territories, Hong Kong

www.wavecom.com