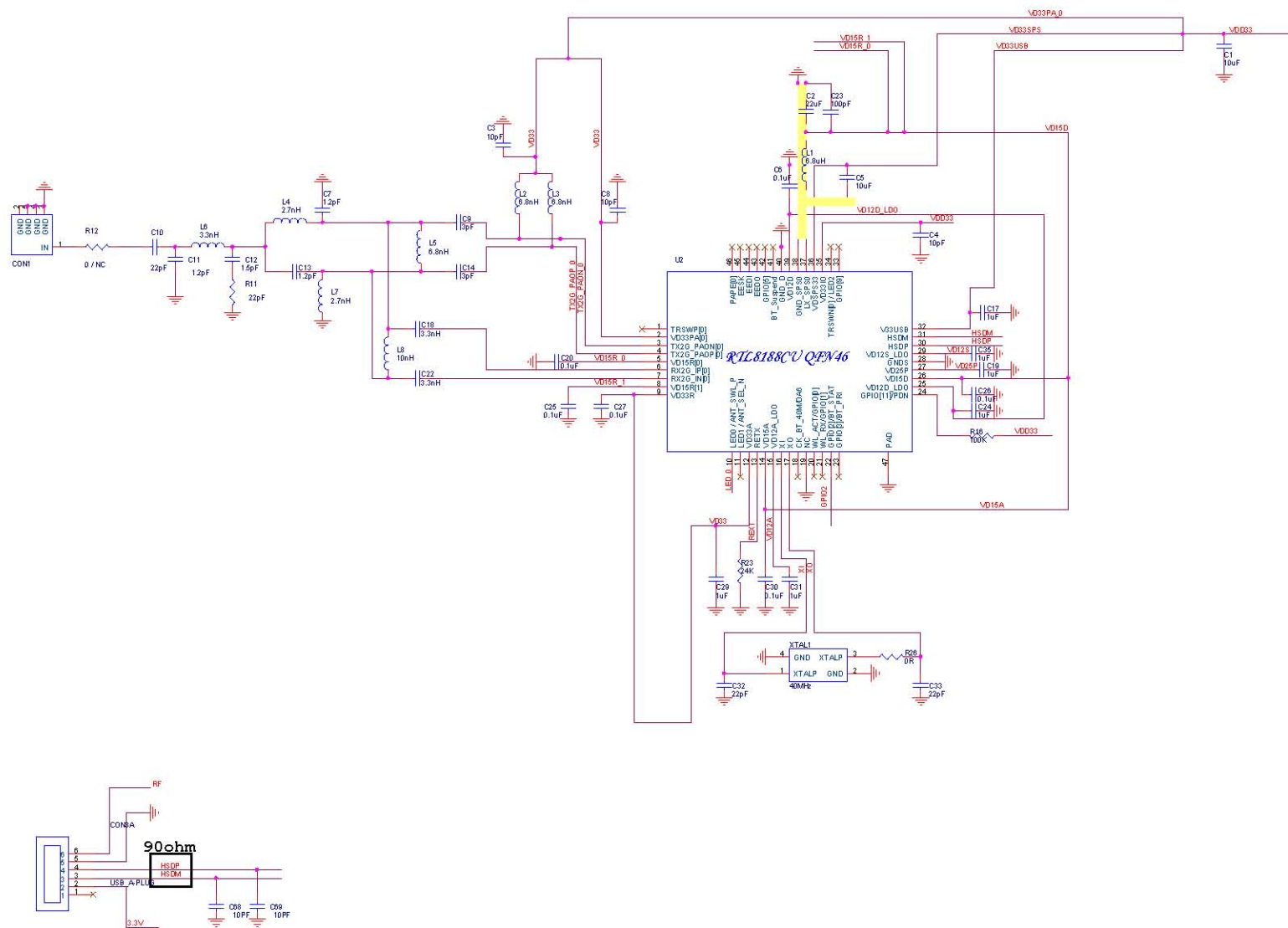
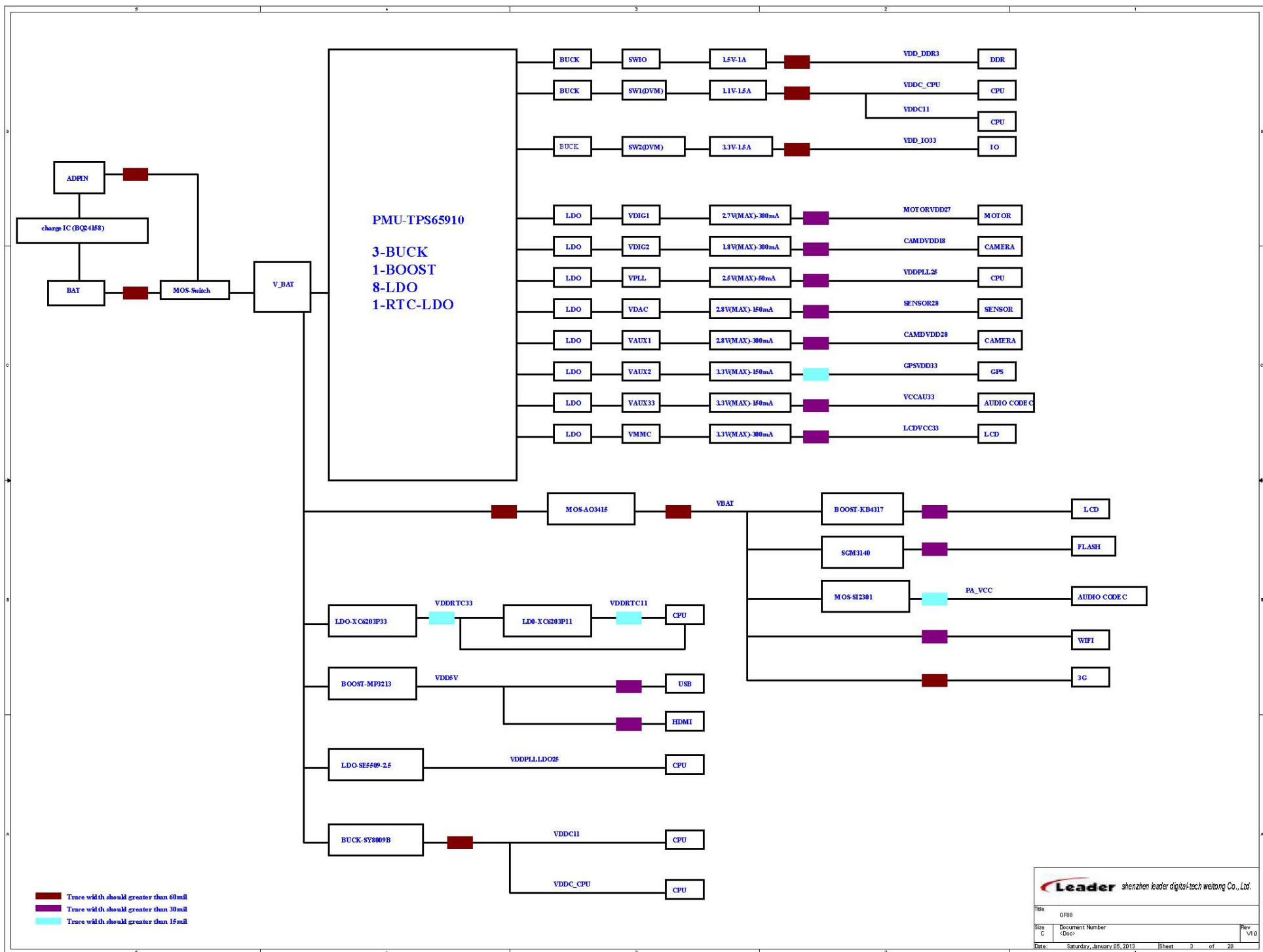
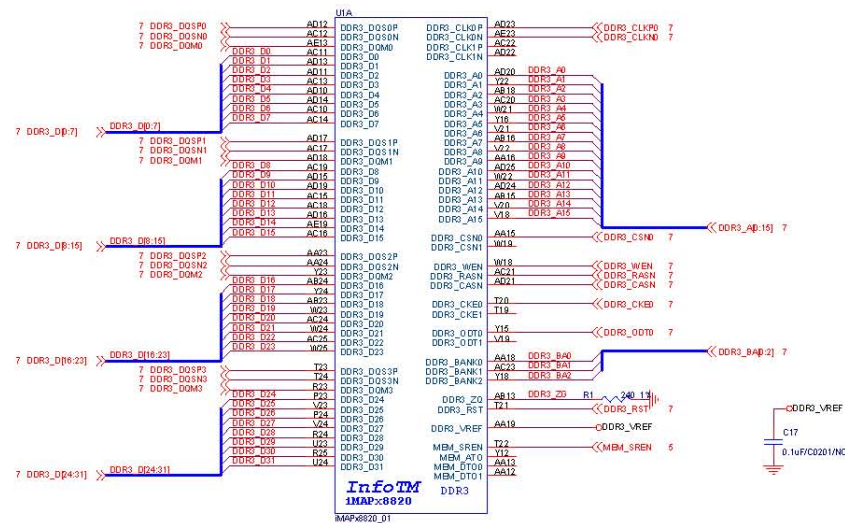


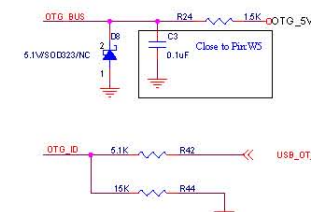
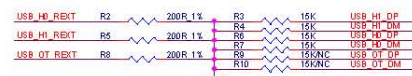
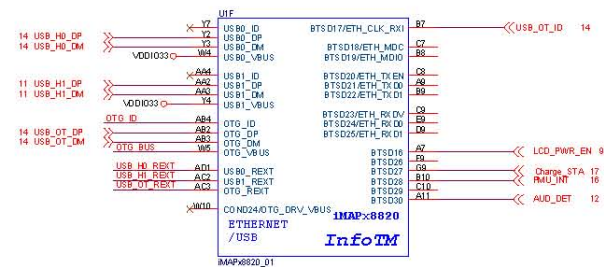




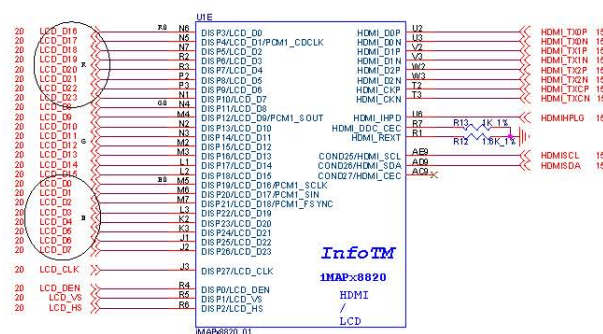
DDR3 Interface



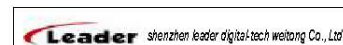
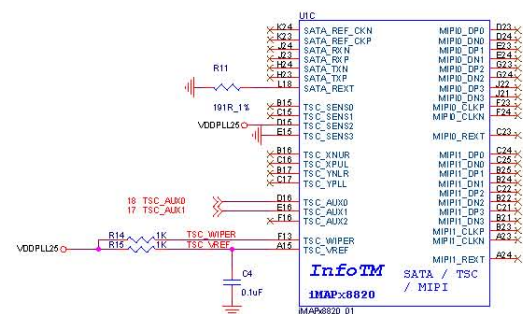
USB / Ethernet Interface



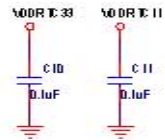
LCD / HDMI Interface



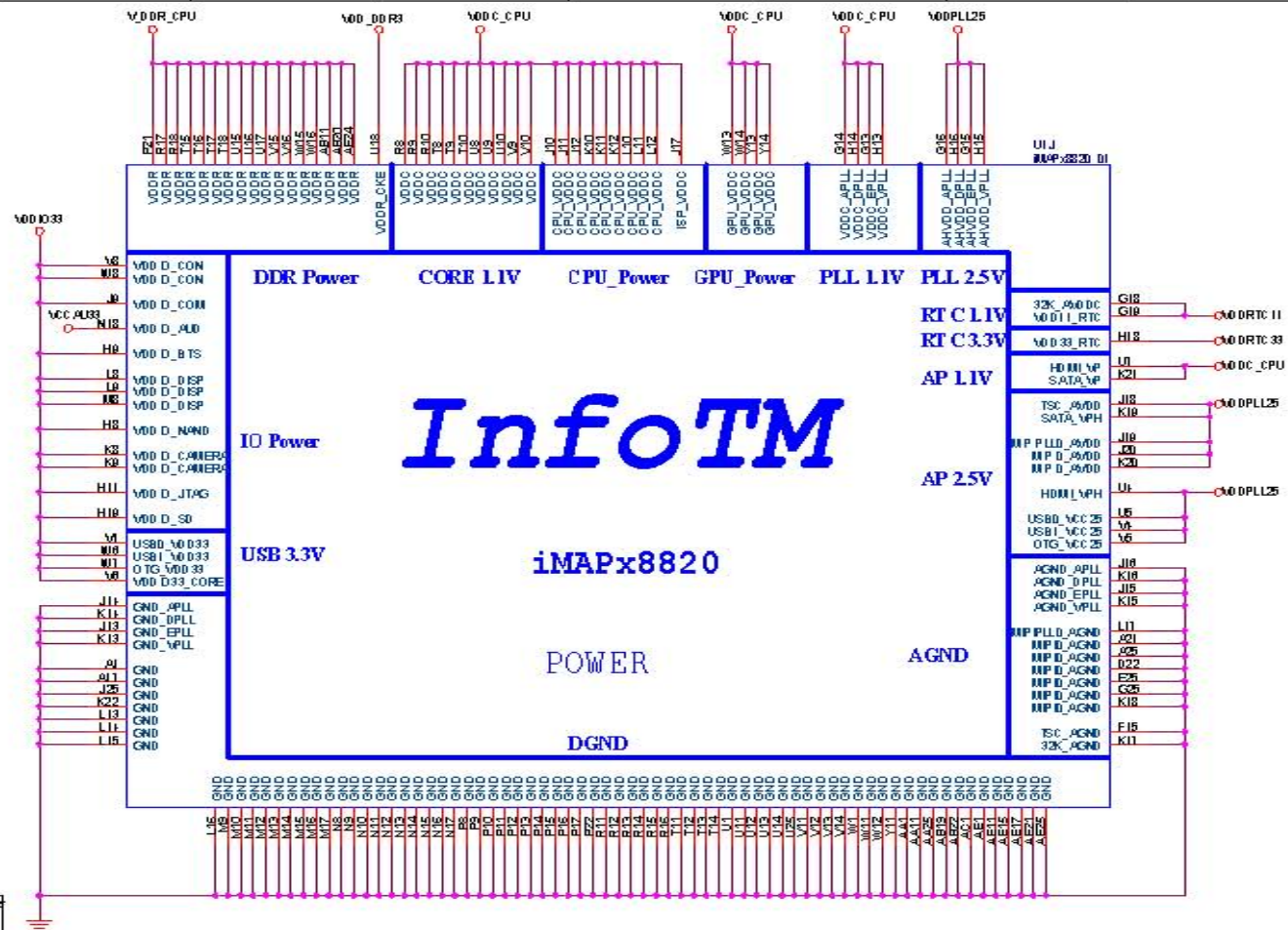
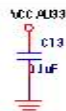
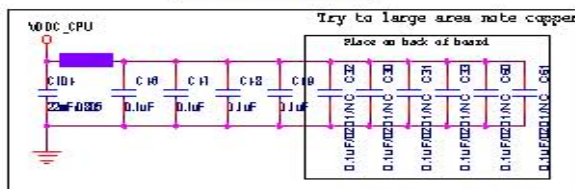
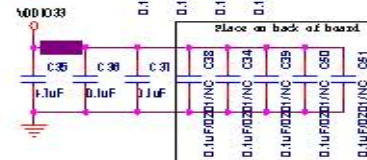
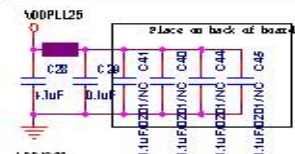
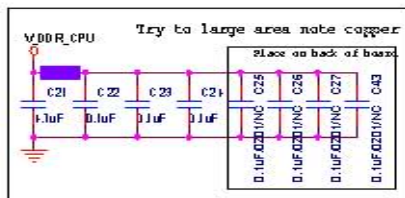
SATA / MIPI Interface



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Trace width should be greater than 60mil
Trace width should be greater than 30mil

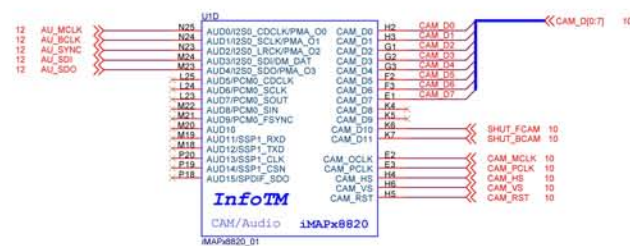


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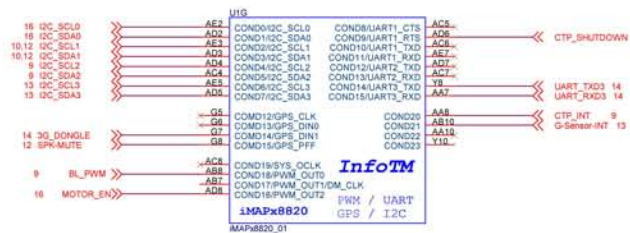
NAND / SD Interface



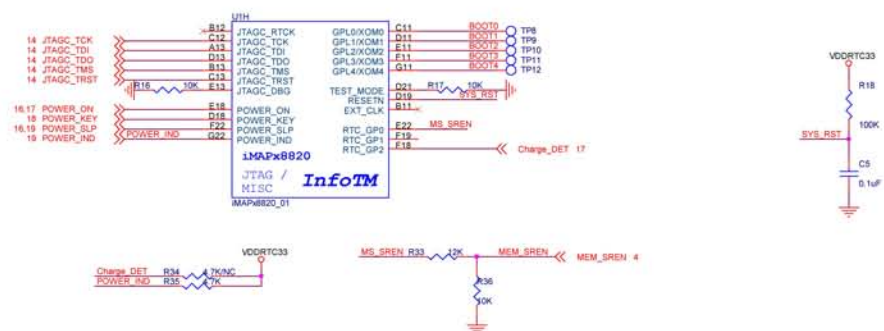
Audio / CAM Interface



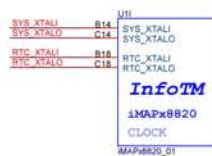
PWM / UART / GPS / I2C Interface



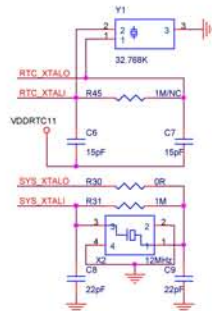
JTAG / Misc Interface



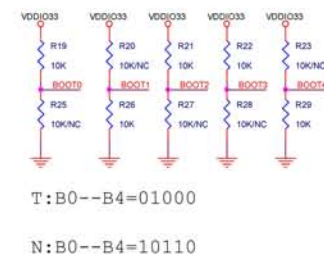
CLOCK Source



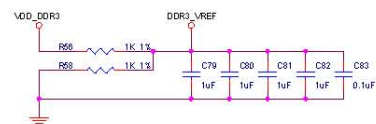
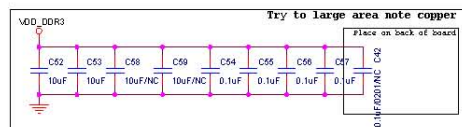
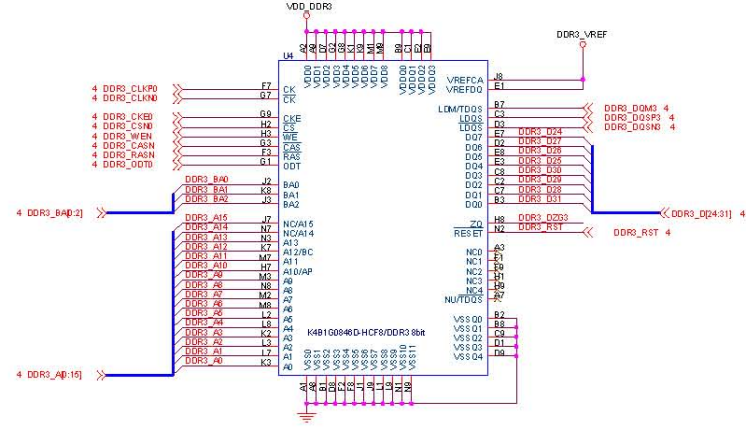
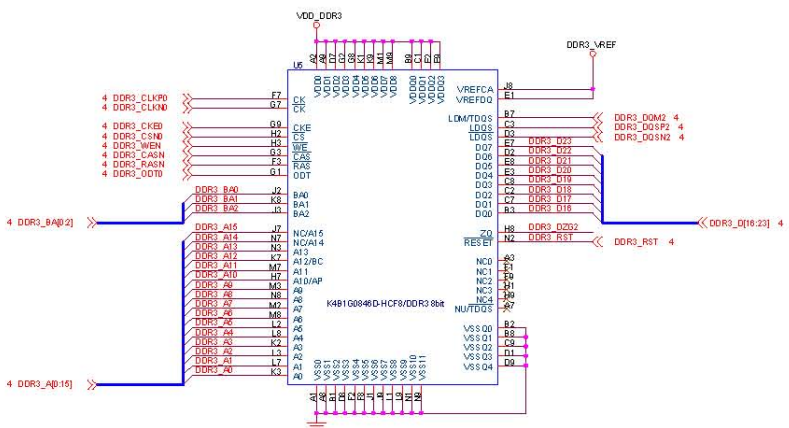
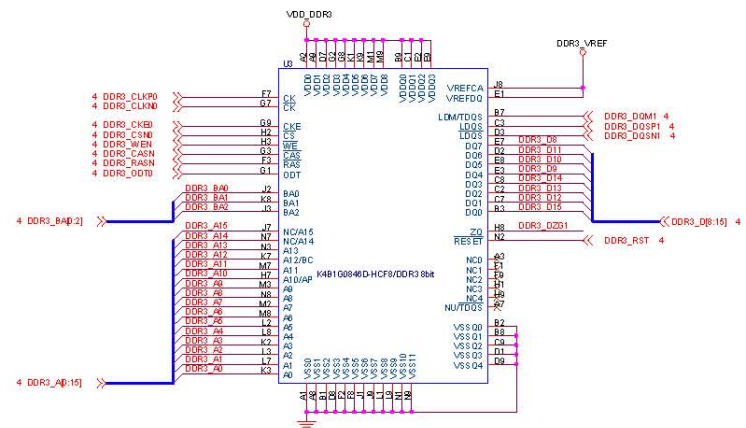
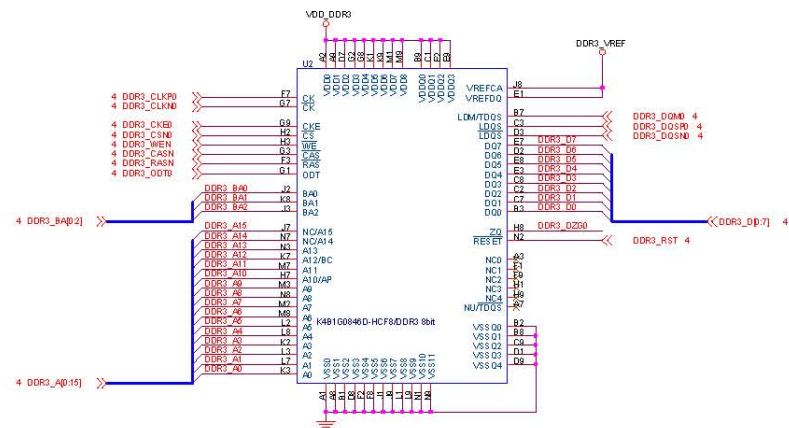
Crystal



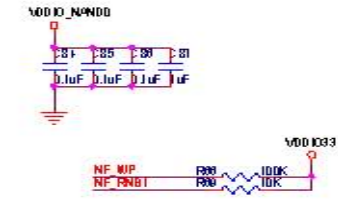
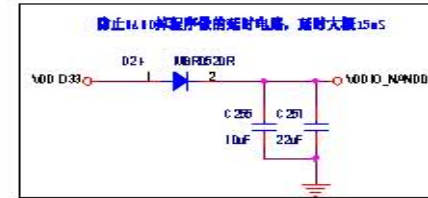
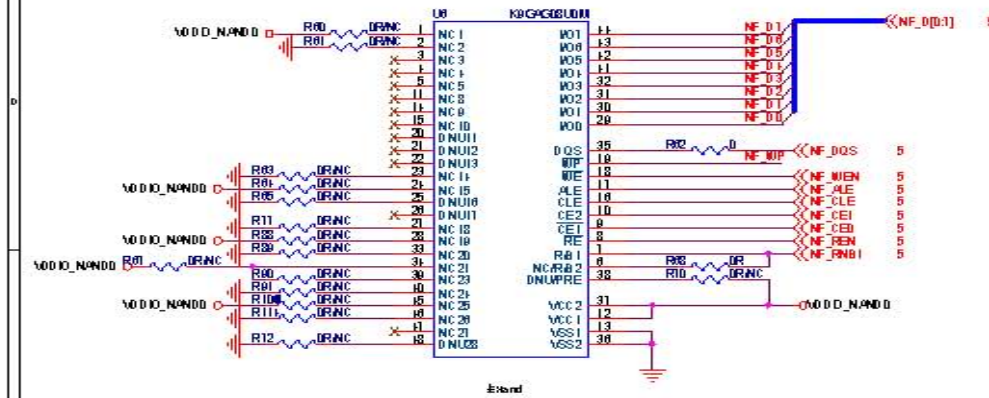
BOOT MODE



DDR3

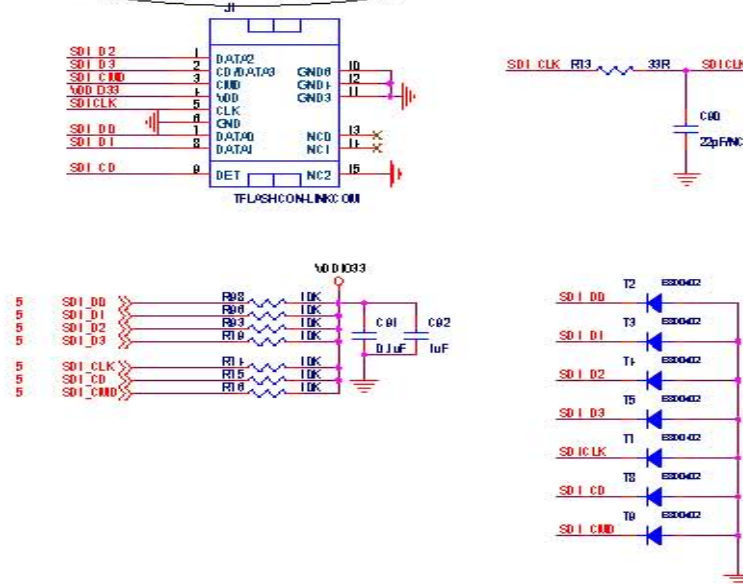


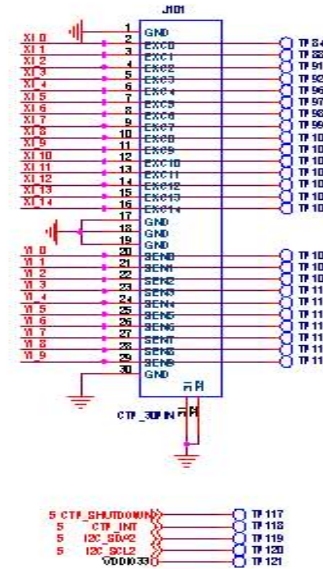
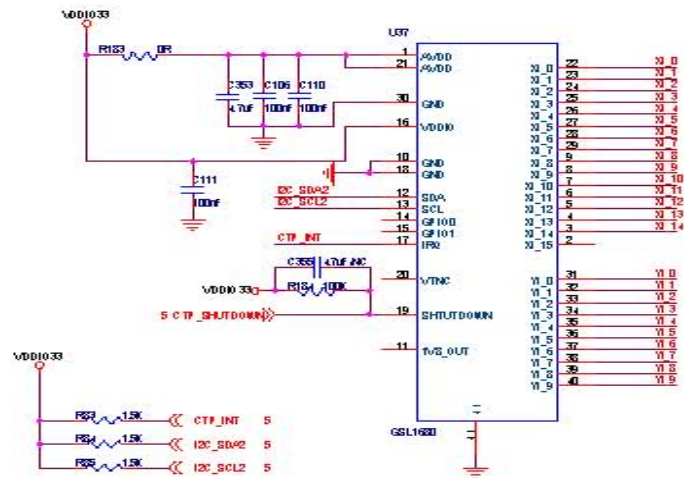
NAND



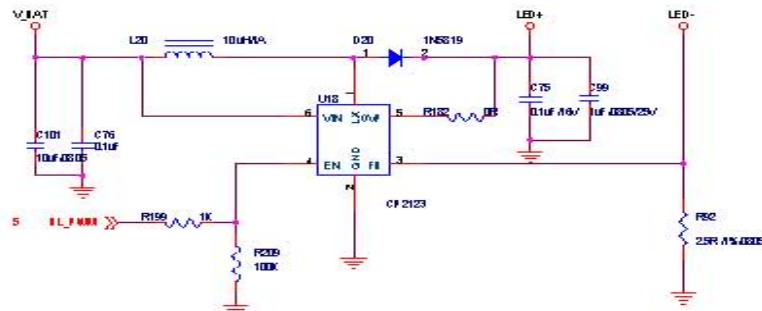
TF Card

For SD Card interface, all signals should keep the equal trace length with in 500m il.





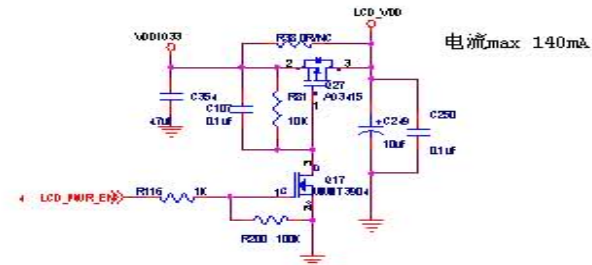
Back Light Circuit

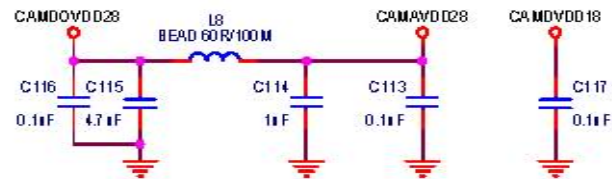
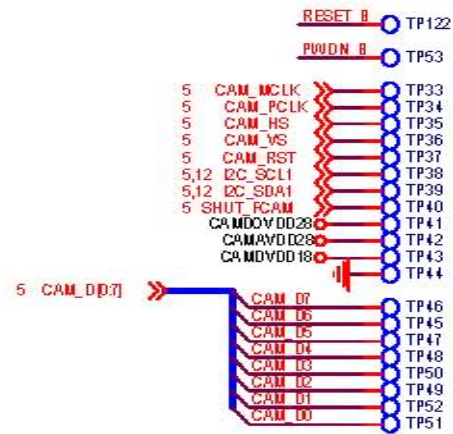
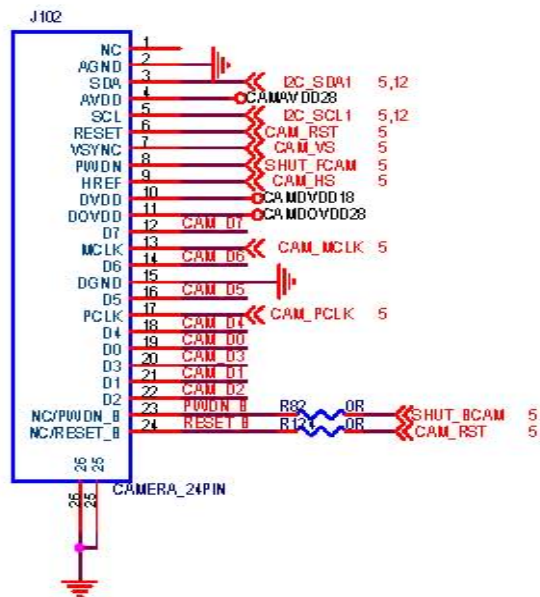


LED: 3X6

CP2123 SY7200A
FB=0.3V FB=0.2V

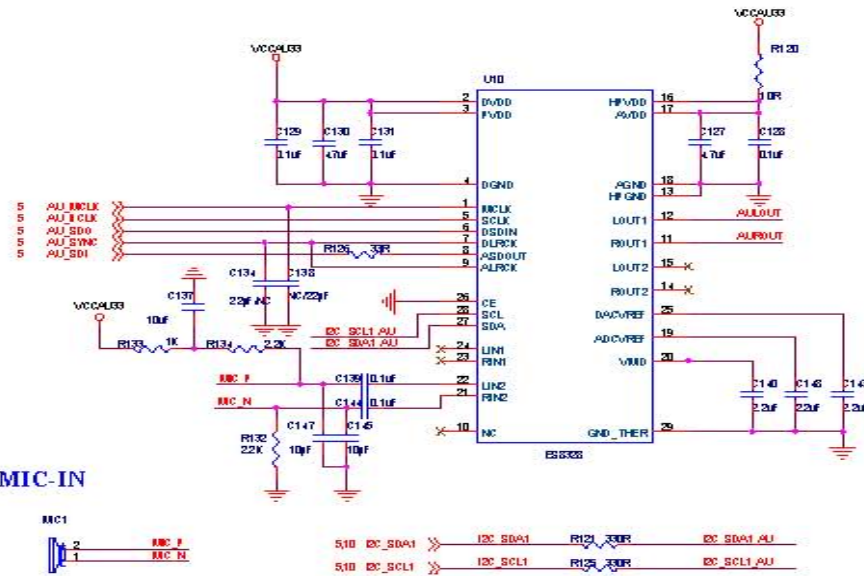
LCD Power



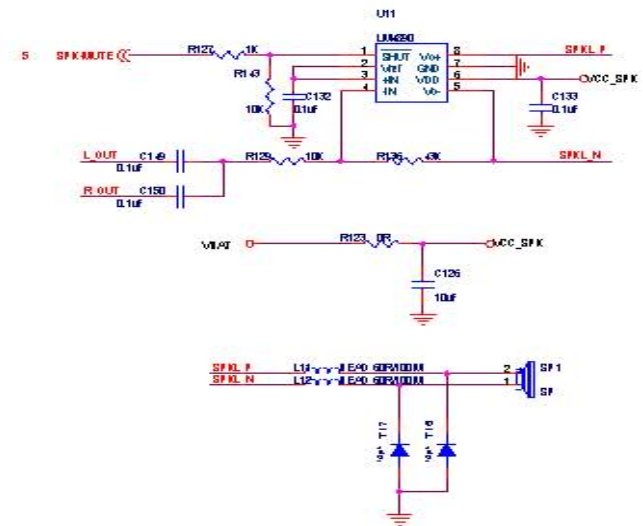


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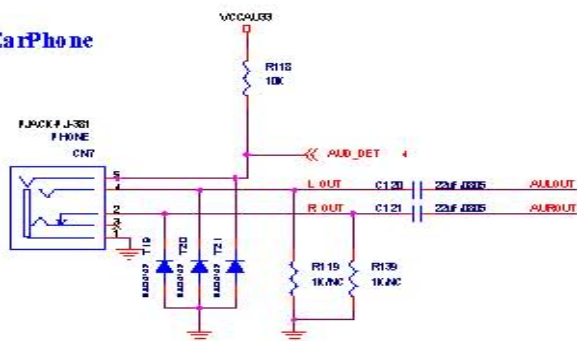
MIC-IN



Audio Codec 的地，在 layout 的时候不需要分离模拟地和虚拟地，但是 Codec 的地不要采用表面其他地方的地走 trace 过来，应该打 VIAL 到第二层相邻的地，一个地脚至少备 2 个 VIAL，这样可以极大的减少回流的干扰，减少电流声。音频功放的地也要这样接，直接打 VIAL 到相邻层的地，不需要周围的地方走 trace 相连。

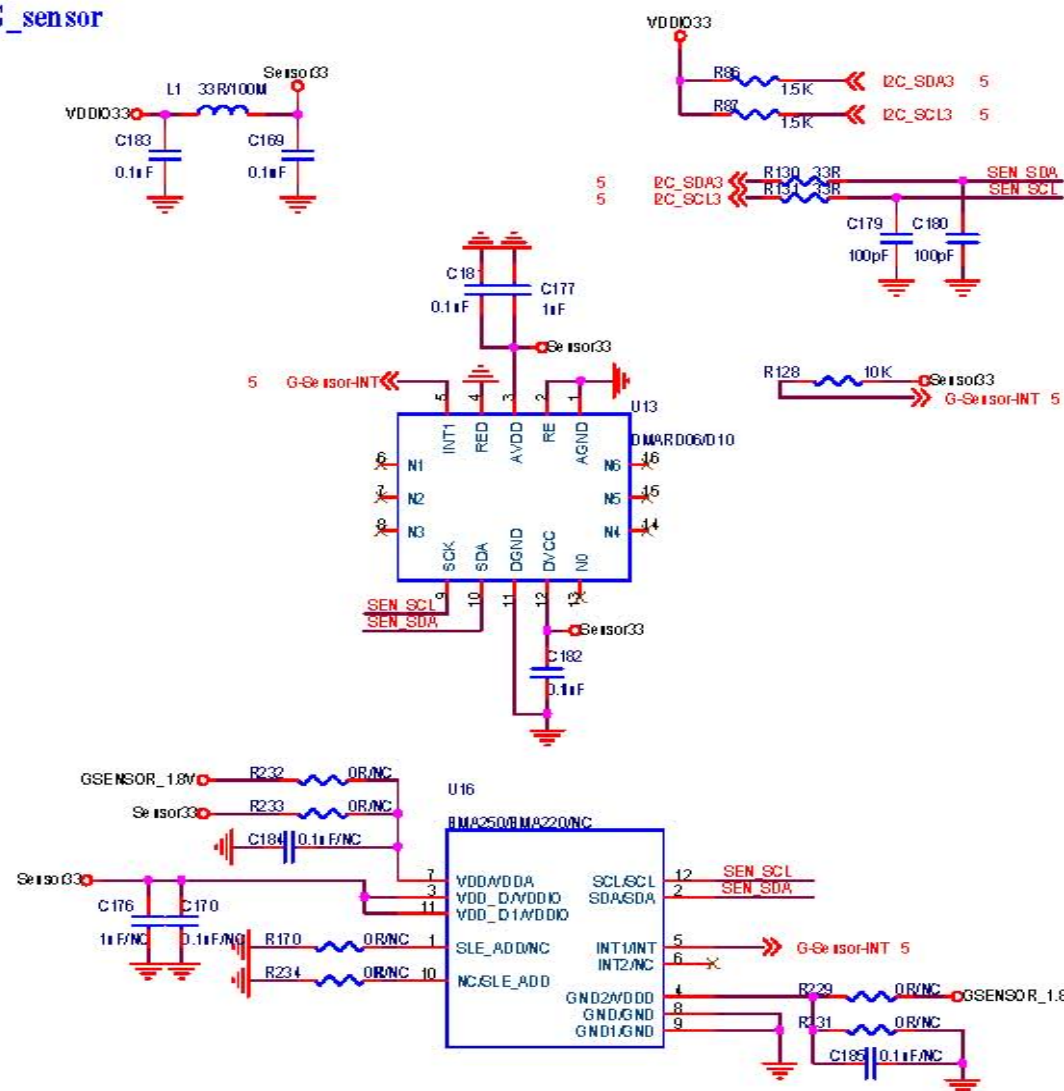


PJACK# J-361
 PHONE



Gryo-Sensor

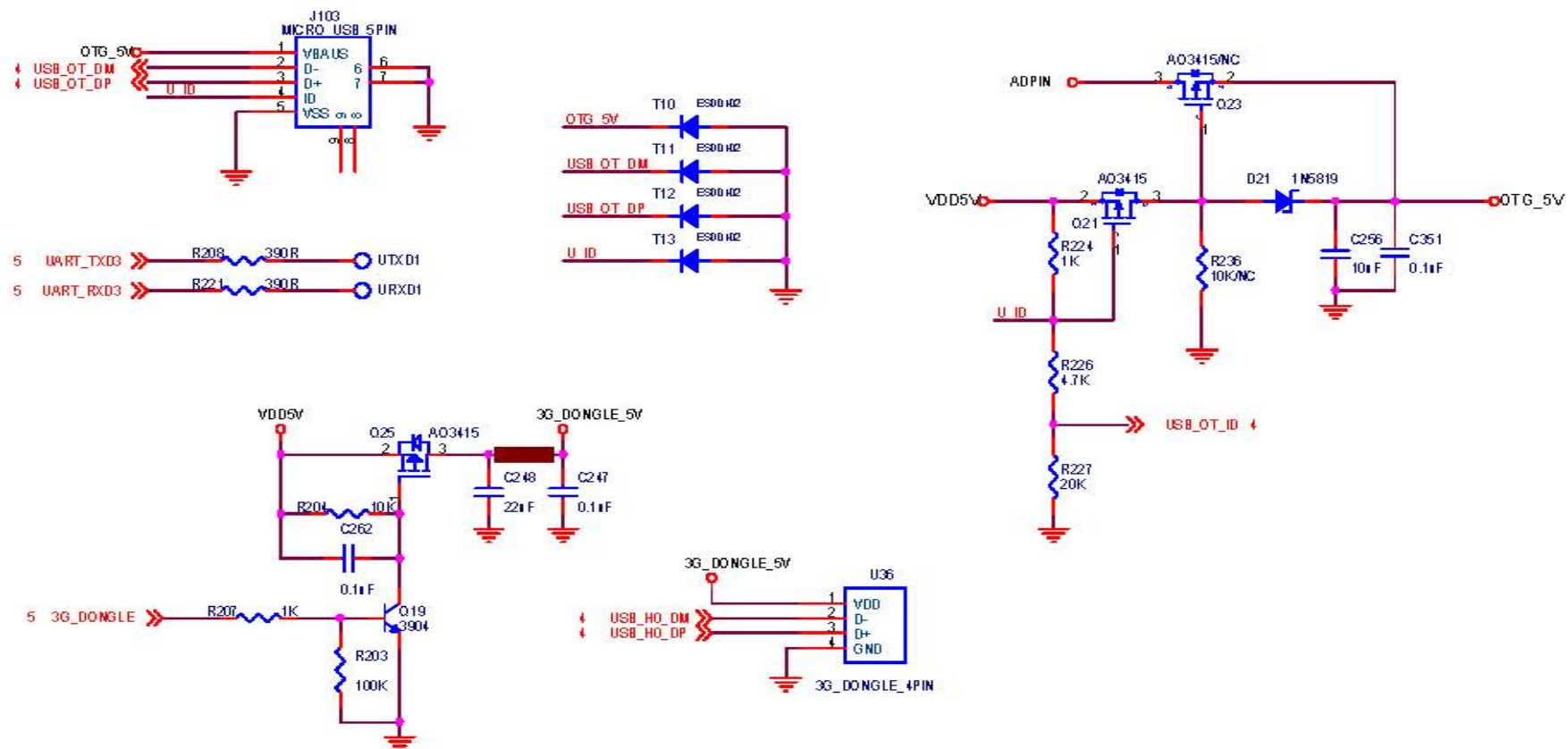
G_sensor



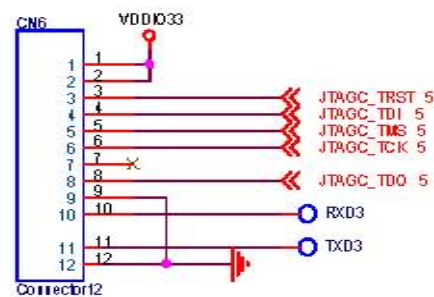
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OTG

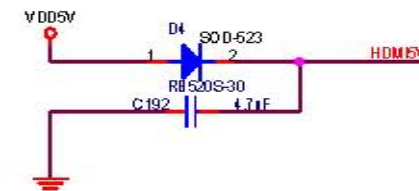
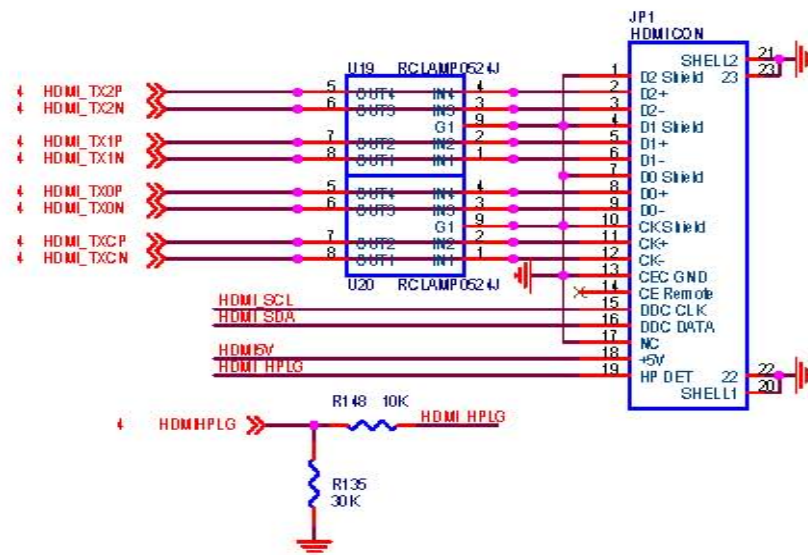


JTAG Connector

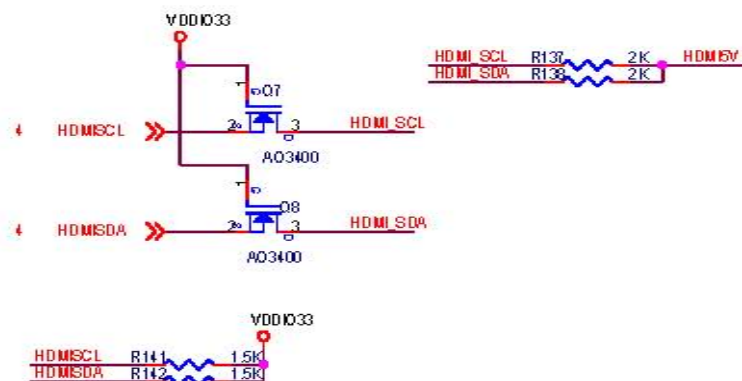


HDMI

HDMI ESD

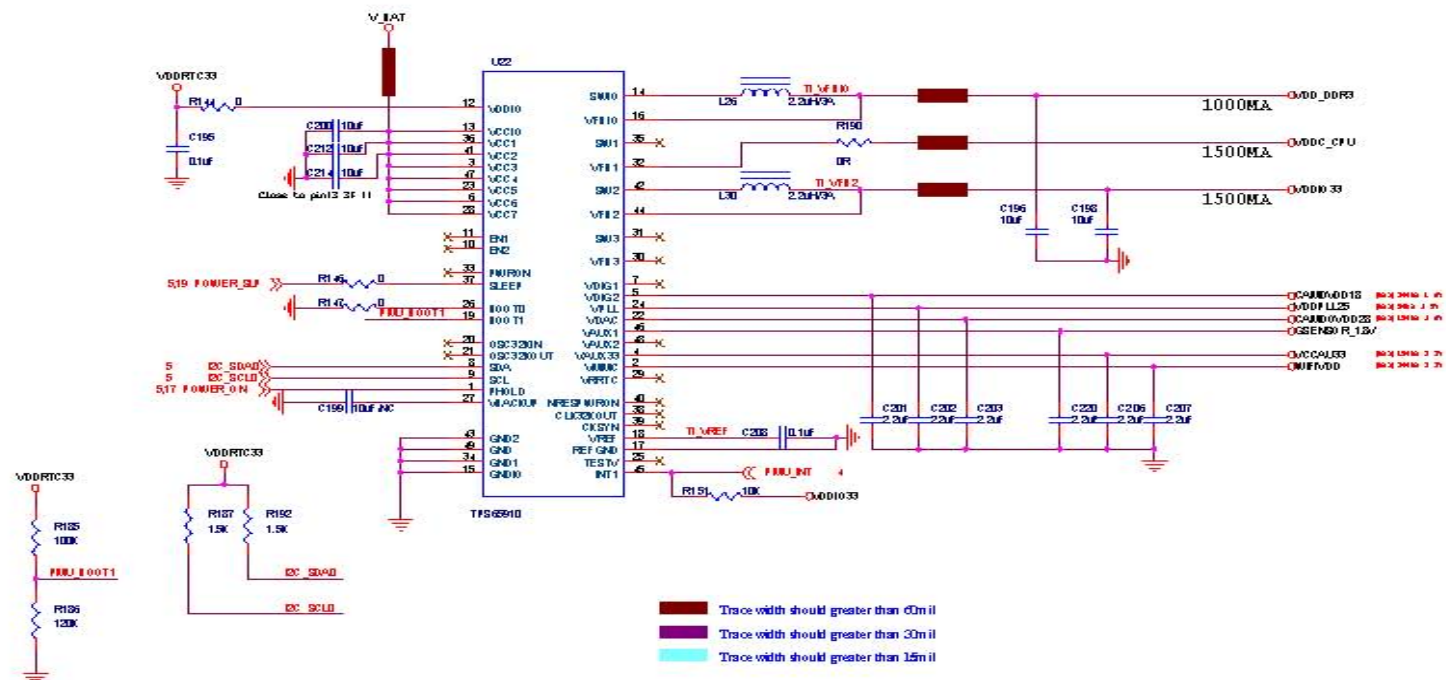


HDMI LEVEL SHIFT

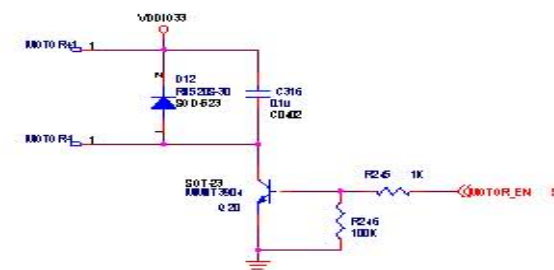


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TI PMU TPS65910



RESOURCE	TYPE	VOLTAGES	POWER
VIO	SMPS	1.5 V / 1.8 V / 2.5 V / 3.3 V	1000 mA
VDD1	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD2	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD3	SMPS	5 V	100 mA
VDIG1	LDO	1.2 V, 1.5 V, 1.8 V, 2.7 V	300 mA
VDIG2	LDO	1 V, 1.1 V, 1.2 V, 1.8 V	300 mA
VPLL	LDO	1.0 V, 1.1 V, 1.8 V, 2.5 V	60 mA
VDAC	LDO	1.8 V, 2.6 V, 2.8 V, 2.85 V	150 mA
VAUX1	LDO	1.8 V, 2.5 V, 2.8 V, 2.85 V	300 mA
VAUX2	LDO	1.8 V, 2.8 V, 2.9 V, 3.3 V	150 mA
VAUX3	LDO	1.8 V, 2.0 V, 2.8 V, 3.3 V	150 mA
VMMC	LDO	1.8 V, 2.8 V, 3.0 V, 3.3 V	300 mA



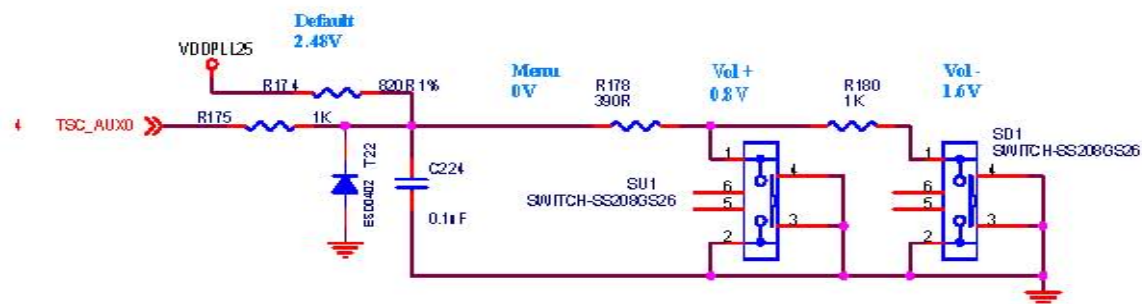
[illegible]

Battery Charger

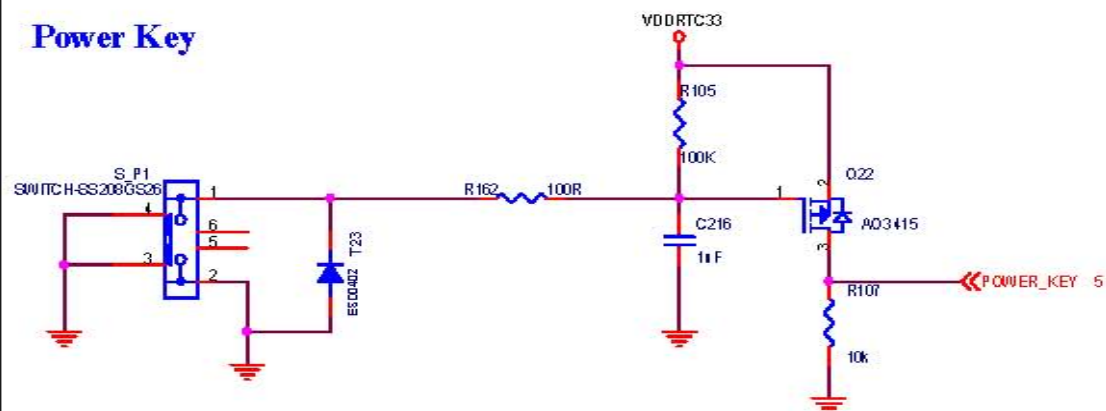
The diagram shows a battery charger circuit. It features a USB input (VIN) connected to a 4.7k resistor (R32) and a 100nF capacitor (C21). The USB input is also connected to a 100k resistor (R32) and a 100nF capacitor (C21). The USB input is connected to the VIN pin of the IC. The IC has pins for CHARGE, DONE, and BAT. The CHARGE pin is connected to a 100k resistor (R32) and a 100nF capacitor (C21). The DONE pin is connected to a 100k resistor (R32) and a 100nF capacitor (C21). The BAT pin is connected to a 100k resistor (R32) and a 100nF capacitor (C21). The IC is powered by a 5V regulator (U1) with a 100k resistor (R32) and a 100nF capacitor (C21). The output of the regulator is connected to the BAT pin of the IC. The IC is also connected to a 100k resistor (R32) and a 100nF capacitor (C21). The output of the IC is connected to a 100k resistor (R32) and a 100nF capacitor (C21). The output of the IC is connected to a 100k resistor (R32) and a 100nF capacitor (C21).

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Function Keys



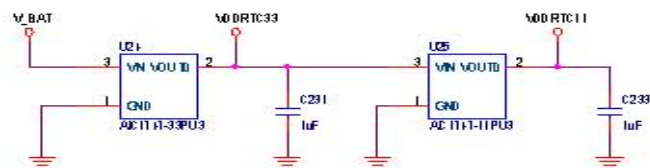
Power Key



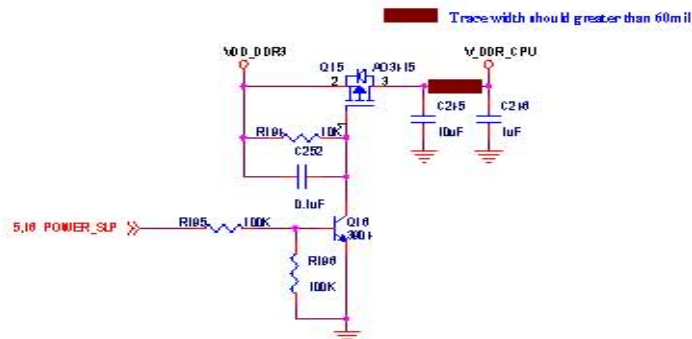
Home Key

Back Key

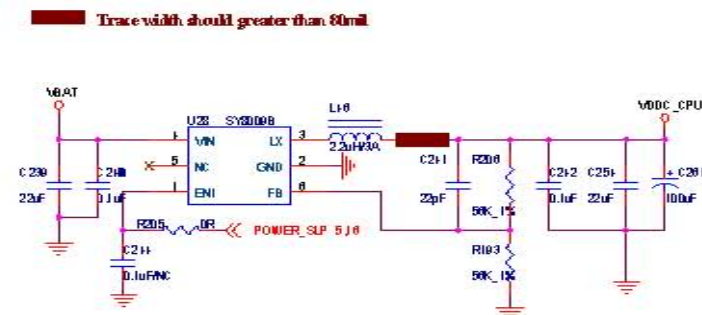
RTC Power



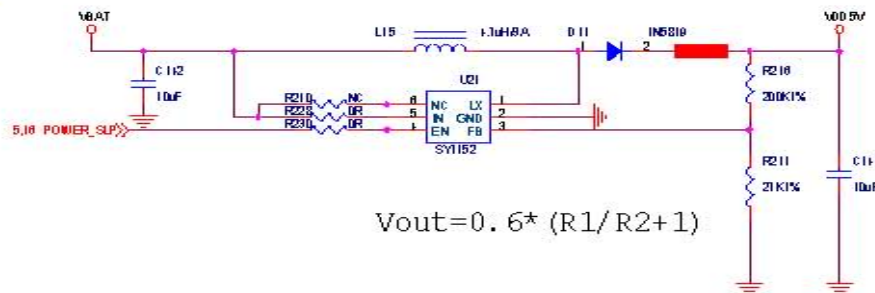
V_DDR_CPU



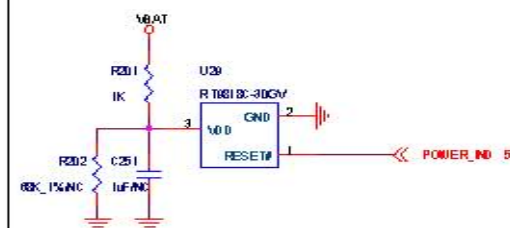
VDDC



Boost 5V



Power-ON and Low-Bat Protector!



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