

P4097 Specification

Read/Write analog front end IC with serial μ C interface for usage in 125kHz RFID Basestation applications

TeraTron GmbH

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1. Features

- Integrated PLL system to achieve self adaptive carrier frequency to antenna resonant frequency
- Chip can be forced to run with external clock, division ratio 32
- 100kHz to 150kHz carrier frequency range
- Direct antenna driving using bridge driver
- Data transmission by OOK (100% Amplitude Modulation)
- Multiple transponder protocol compatibility, (i. Ex.: H400X, V4050, V4X50, V4070, V4X70, P4069, P4077, ...)
- Two sampling points for demodulation, allowing extended system tolerances
- Serial μ C interface for diagnosis and status control
- Very low sleep mode current consumption of 1 μ A typically
- USB compatible power supply range
- -40 to +85°C automotive temperature range
- Small outline plastic package SO16

2. Description

The P4097 chip is a CMOS integrated transceiver circuit intended for use in an RFID basestation to perform the following functions:

- Antenna driving with carrier frequency to transfer energy to the transponder
- Data transfer to writable transponder by amplitude modulation (ASK) of the field (100% modulation ratio, called OOK, "on"- "off" keying)
- Data transfer from transponder by amplitude- or phase demodulation (ASK or PSK)
- μ C Interface to communicate with a microprocessor

3. Applications

- Car immobiliser in intelligent- or active coil configuration
- Hand held reader
- Low cost reader

4. Pin assignment

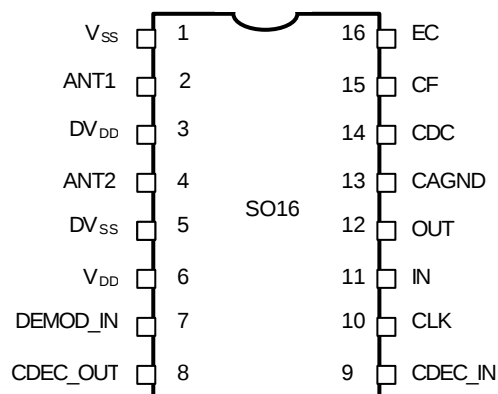


Figure 1. Pinning diagram

5. Absolute Maximum Ratings

Parameter	Symbol	Condition
Storage temperature	T_{Store}	-55°C to +125°C
Maximum voltage at V_{DD}	V_{DDmax}	$V_{SS} + 6V$
Minimum voltage at V_{DD}	V_{DDmin}	$V_{SS} - 0.3V$
Maximum voltage at other pins	V_{max}	$V_{DD} + 0.3V$
Minimum voltage at other pins	V_{min}	$V_{SS} - 0.3V$
Maximum junction temperature	T_{Jmax}	+125°C
Electrostatic discharge according to MIL-STD-883C method 3015 (pins ANT1 and ANT2), 100pF with 1.5kΩ series resistance referenced to V_{SS}	V_{ESD_Ant}	10kV
Electrostatic discharge according to MIL-STD-883C method 3015 (other pins), 100pF with 1.5kΩ series resistance referenced to V_{SS}	V_{ESD}	4kV
Maximum Input/Output current for each pin except V_{DD} , V_{SS} , DV_{DD} , DV_{SS} , ANT1, ANT2	$I_{Imax/Omax}$	10mA
Maximum AC peak current for ANT1 and ANT2 pins @ 100 kHz, 50% duty cycle	I_{ANTmax}	400mA _p
Static Latch-up current, maximum power supply voltage	I_{Latch_S}	±30mA
Dynamic Latch up voltage, 220pF with 50Ω series resistance referenced to V_{SS} , maximum power supply voltage	V_{Latch_D}	±50V

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

6. Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

7. Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating junction temperature	T_J	-40		+110	°C
Supply voltage	V_{DD}	4.1	5	5.5	V
Antenna circuit resonance frequency	F_{Res}	100	125	150	kHz
Q of antenna circuit			10		
Current through ANT1 and ANT2 pins, continuous wave	I_{Ant}			250	mA _p
C_F (not needed if external clock is used)	Note 1, 3 Note 2		10 100		nF
C_{DEC}	Note 1		100		nF
C_{DC}	Note 1		10		nF

C_{AGND}		100		220	nF
Thermal resistance of SO16, soldered on 1.5mm FR4 board with 35µm copper, standard footprint	R_{thJA} Note 4	69	70	71	°K/W
Thermal capacitance of SO16, soldered on 1.5mm FR4 board with 35µm copper, standard footprint	C_{thJA} Note 4		TBD		mWs/°K

Note 1: ±10% tolerance capacitors should be used

Note 2: Phase demodulation with PLL is used (see Bit#1 of serial interface register)

Note 3: Phase demodulation with PLL is not used (Bit#1 should be set to "0")

Note 4: Due to the antenna driver losses the internal junction temperature is higher than the ambient temperature. Please calculate the allowed ambient temperature range by using the maximum antenna current and the maximum package thermal resistance. For transient operation the value of the thermal capacitance may help to calculate the junction temperature at the end of each pulsed operation. In any case it is the user's responsibility to guarantee that T_j remains always below 110°C.

8. System principle

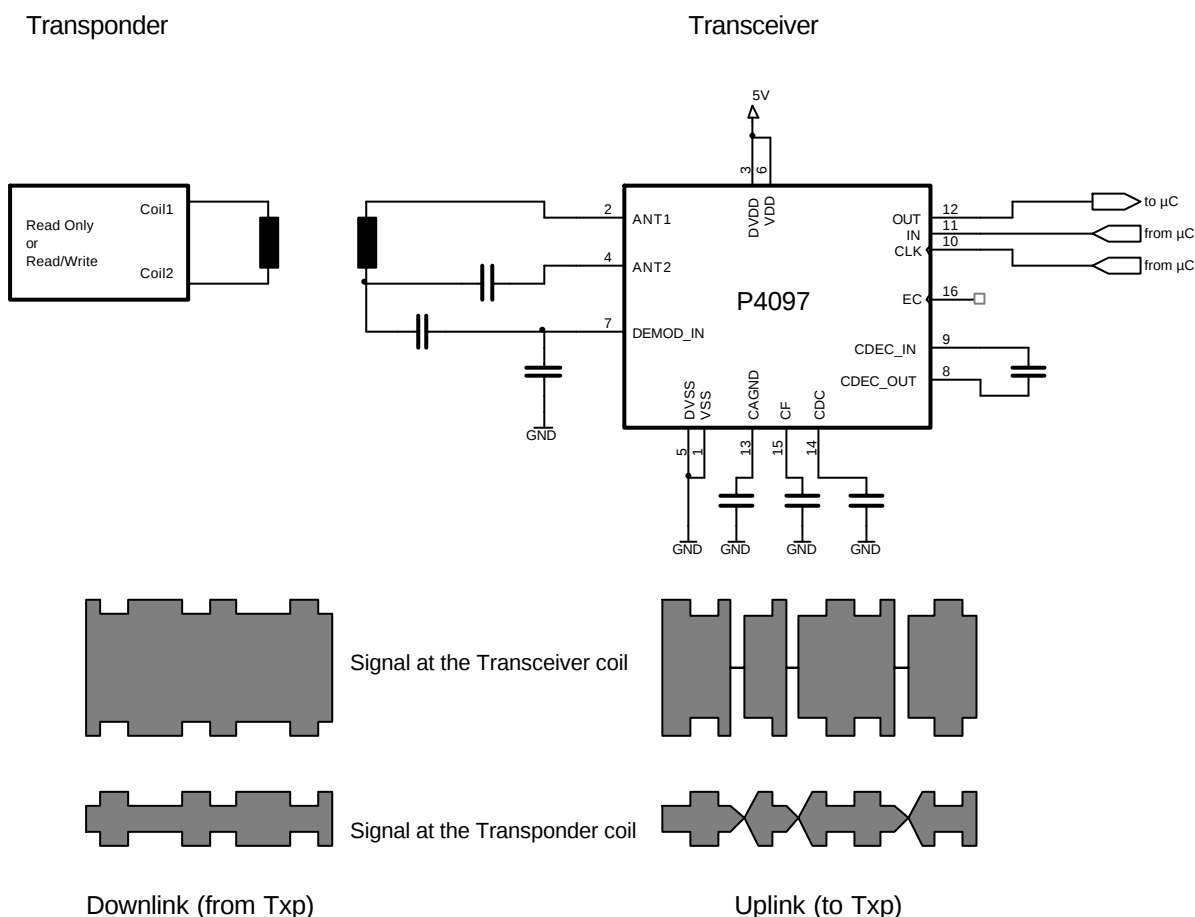


Figure 2. System principle

9. Electrical and Switching Characteristics:

Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page.

$V_{SS} = DV_{SS} = 0V$, $V_{DD} = DV_{DD} = 5V$, $T_J = -40^{\circ}C$ to $+110^{\circ}C$; unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units		
Supply current in power down mode	I _{DDsleep}	Note 1		1	5	μA	T	
Supply current excluding antenna current	I _{DDon}		5	10	mA	T		
CAGND level	V _{CAGND}		2.35	2.5	2.65	V	T	
Logic signals								
Input logic high	V _{IH}	I _{SOURCE} = 1mA I _{SINK} = 1mA	0.7V _{DD}		0.3V _{DD}	V	T	
Input logic low	V _{IL}				0.3V _{DD}	V	T	
Output logic high	V _{OH}		0.9V _{DD}			V	T	
Output logic low	V _{OL}				0.1V _{DD}	V	T	
IN, CLK, EC pull down resistor	R _{PD}	0.3V _{DD}	25	50	75	kΩ	T	
Input leakage current			-1		+1	μA	T	
PLL								
Antenna capture frequency range	F _{ANT_C}		100		150	kHz	T	
Antenna locking frequency range	F _{ANT_L}		100	125	150	kHz	Q T	
Antenna driver								
ANT driver output resistance, full path	R _{AD}	I _{Ant} = 10mA, T _J = 25 °C I _{Ant} = 100mA		8	13	Ω	T	
R _{AD} = R _{ADL} + R _{ADH}	R _{AD}			8	15	Ω	Q	
Diagnostic ANT driver threshold “high”	V _{diagOutH}			0.5V _{DD}		V	Q	
Diagnostic ANT driver threshold “low”	V _{diagOutL}			0.5V _{DD}		V	Q	
Current threshold for protective shut down	I _{sh}			600		mA		
AM demodulation								
DEMOD_IN common mode range	V _{CM}	Note 2	V _{SS} + 0.5		V _{DD} - 0.5	V		
DEMOD_IN input sensitivity, at gain = 480	V _{sense}				0.8 2	1.4	mV _{pp}	Q T
Diagnostic DEMOD_IN threshold	V _{diagIn}			1.0		1.5	V _{pp}	T

General Note: The minimal and maximal values are guaranteed within the complete temperature range. Nevertheless the test of these parameters (T) is done at room temperature. Parameters marked with (Q) are not tested but qualified.

Note 1: AGND is a P4097 internal reference point. Any external connection except specified capacitor to V_{SS} may lead to device malfunction.

Note 2: Modulating signal 2kHz square wave on 125kHz carrier, within boundaries of V_{CM} .

10. Timing Characteristics:

Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page.

$V_{SS} = DV_{SS} = 0V$, $V_{DD} = DV_{DD} = 5V$, $T_J = -40^{\circ}C$ to $+110^{\circ}C$; unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Set-up time after a sleep period (fast start-up)	T_{setF}	Modulating signal 2kHz square wave $10mV_{pp}$ at $f_{Res} = 125kHz$ Note 1		25	35	ms	T
Set-up time after a mode change (slow start-up)	T_{setS}			100	140	ms	Q
AM demodulation: Delay time from input to output	T_{pd}			40	100	μs	T
Recovery time of reception after antenna modulation	T_{rec}				550	μs	Q
External clock frequency range	f_{ext}		3.2	4.0	4.8	MHz	Q
External clock duty cycle			40		60	%	Q
External clock input capacitance	C_{EC}			5		pF	Q
Maximum clock frequency	f_{max}				1	MHz	Q
Minimum pulse width (CLK) "high"	$t_{W(H)}$		400			ns	Q
Minimum pulse width (CLK) "low"	$t_{W(L)}$		400			ns	Q
Minimum setup time	t_s		50			ns	Q
Minimum hold time	t_h		5			ns	Q
Minimum reset time	t_{res}		200			ns	Q

General Note: The minimal and maximal values are guaranteed within the complete temperature range. Nevertheless the test of these parameters (T) is done at room temperature. Parameters marked with (Q) are not tested but qualified.

Note 1: The condition is of course that the amplitude on antenna has already reached its steady state by that time (this depends on Q of antenna). See also Application Notes.

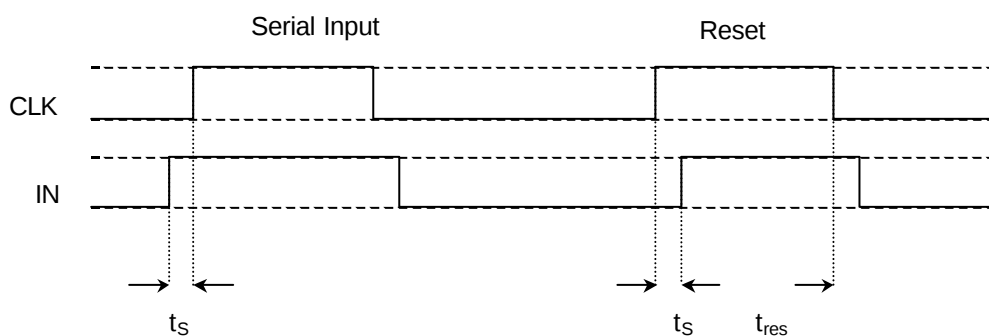


Figure 3. Reset and Setup times

11. Block diagram and Pin Description

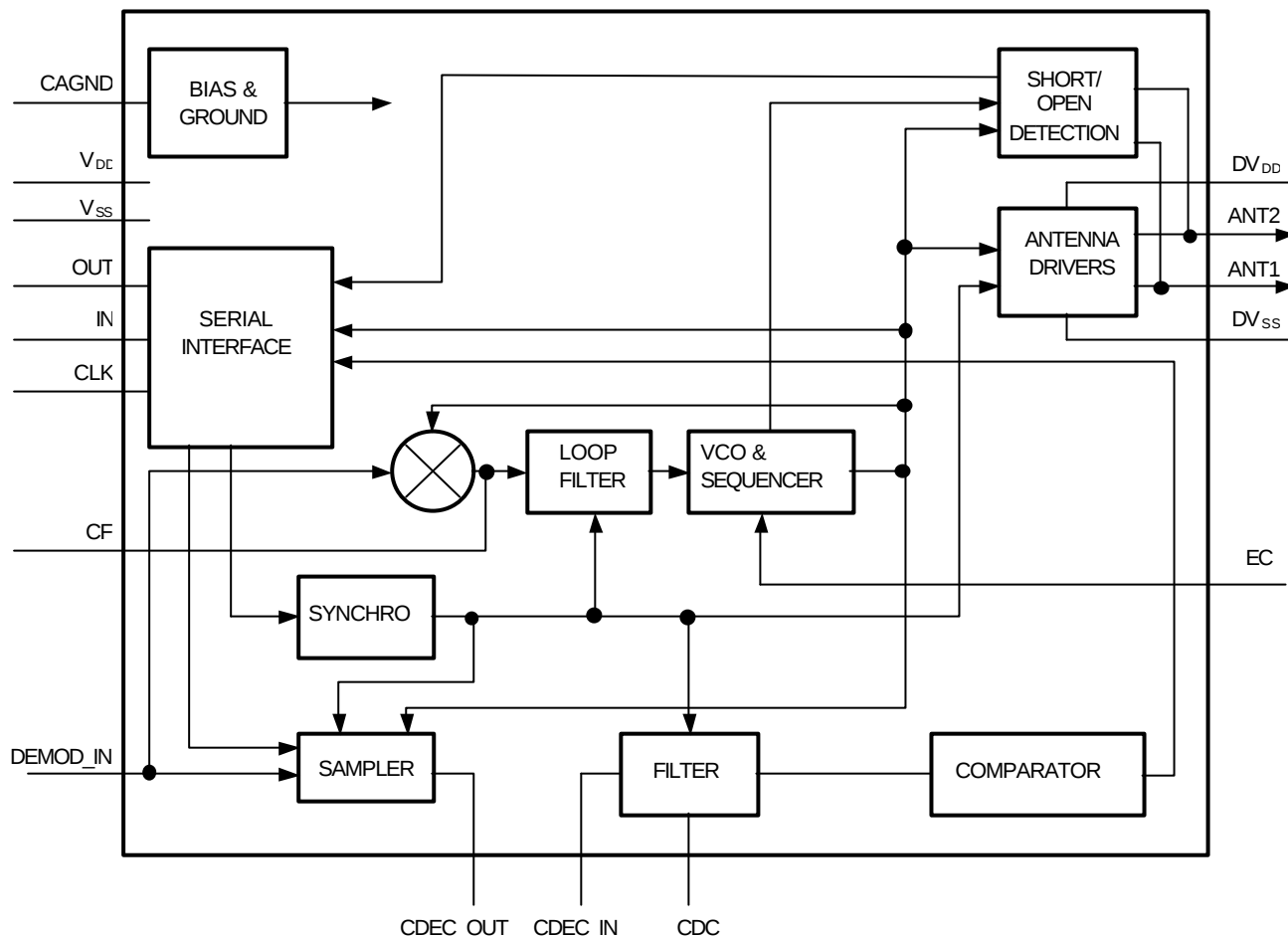


Figure 4. Block diagram

Pin	Symbol	Description	Type
1	V _{SS}	negative supply voltage	power supply
2	ANT1	antenna driver output	output
3	DV _{DD}	positive supply voltage for antenna driver	power supply
4	ANT2	antenna output	output
5	DV _{SS}	negative supply voltage for antenna driver	power supply
6	V _{DD}	positive supply voltage	power supply
7	DEMOD_IN	receiver input	analog input
8	CDEC_OUT	DC blocking capacitor connection "out"	analog signal
9	CDEC_IN	DC blocking capacitor connection "in"	analog signal
10	CLK	μC interface, serial clock input	input (pull down)
11	IN	μC interface, serial data input, modulation pin	input (pull down)
12	OUT	μC interface, serial data output, clock reference	output
13	CAGND	Analog ground	analog signal
14	CDC	DC decoupling capacitor	analog signal
15	CF	PLL loop filter capacitor	analog signal
16	EC	external clock	input (pull down)

12. Functional Description

12.1 General

The P4097 is intended to be used either with an attached antenna circuit and a μ controller or in an active but non-intelligent antenna configuration. Few external components are needed to achieve DC and RF filtering and power supply decoupling.

A stabilized power supply with sufficient current rating to supply the coil driver has to be provided. Any ripple on V_{SS} causes a modulation of the antenna voltage and therefore a modulation of the received signal at DEMOD_IN. Please note that operating configurations in this document present only elements, which are essential for P4097 operation. Additional power supply filtering capacitors, which are necessary to filter power supply are not shown.

12.2 Serial Interface

Device operation is controlled by 8 bit Configuration Register. This register is written via serial interface. The functionality is as follows:

Serial Interface is controlled by signal CLK. When power supply is applied (Power on Reset) Serial Interface is set in Initial State (beginning of timing on figure 5). The CLK signal has to be low. First pulse on CLK will transition Serial Interface in Command State. In Command State the functionality of the IN and OUT pins changes: IN pin is used to enter 8 bit data, OUT pin is used as diagnostic output. During clock cycles 2 to 9 the Serial Interface receives 8 bit information. The 8 bits are shifted in 8 bit shift register on rising edge of CLK. On the falling edge of pulse 9 the 8 bit information is loaded in Configuration Register. During cycles 10 to 12 the μ Controller gets status information back from the device. The status bits are put on pin OUT after rising edge on signal CLK. With the 13th clock pulse Serial Interface transition in Active State, pins IN and OUT resume their normal function. Additional pulses on pin CLK do not have any influence on P4097 operation. An Interface Reset is needed to transition Serial Interface back in Initial State.

Interface Reset: A high Signal at the CLK pin and a rising edge at the IN pin causes transition of Serial Interface in Initial State. Interface Reset is accepted in all states of Serial Interface.

Change of P4097 Configuration register and thus operation of device is done by performing Interface Reset and shifting in new 8 configuration bits.

Every serial communication has to start with an interface reset. Clock cycles without a leading interface reset are meaningless.

Power on Reset: After the power is switched on the internal POR circuitry set Serial Interface in Initial State. Power Down bit of Configuration Register is set to 0 (power down mode). P4097 is thus in inactive sleep mode with low current consumption.

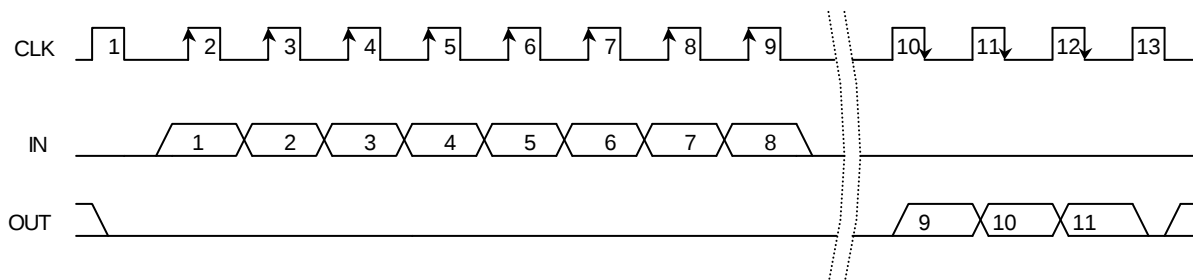


Figure 5. I/O Timing

As explained above the Configuration Register changes its state with the falling edge of clock 9 in the Command Mode. Changing the Power Down bit, changing the gain, the demodulation phase or the clock source causes a delay of about 100ms until the operating points of analog blocks are settled. This time can be reduced to about 25ms if the fast analog start-up has been set. In order to receive a correct diagnostic output an appropriate pause has to be inserted between CLK pulses 9 and 10. Anyway the chip can be forced to return an answer immediately after sending the 8 configuration bits but the diagnostic data like PLL-Status may be incorrect since the analog operating points are not set yet. See also figure 6, which present possible states of Serial Interface and conditions for transitions between them.

Bit #	Description	Reset	if Bit is set to "0"	if Bit is set to "1"
1	Sample Point	0	Amplitude demodulation	Phase demodulation
2	Power Down	0	Power Down	Active
3	EC=1 Bit#4=0	0	Data from Txp at OUT-pin IN pin has no function	Data to Txp with IN-pin OUT pin pulled to VSS
	EC=0 Bit#4=0		Txp-Data at OUT-pin	Clock at OUT-pin
	EC=X Bit#4=1		Txp-Data at OUT-pin	Clock at OUT-pin
4	Clock source	0	Internal PLL	External clock
5	Analog start-up	0	no change	fast start-up
6	Gain setting	0	see below	
7	Gain setting	0	see below	
8	Test mode	0	Normal mode	Test mode
9	Antenna Status	0	Correct load	Short circuit
10	Input Status	0	Correct signal	No input signal
11	PLL-Status	0	Locked	Not locked

Bit #1: The relative demodulation phase can be changed with this bit allowing higher tolerances in the transponder to antenna matching.

Bit #2: This bit determines whether the chip is in sleep mode with low power consumption or active. Active mode means the chip is using the current contents Configuration register for operation. Note that there is no answer from the chip after sending the power down bit. This means that on falling edge of bit 9 Serial Interface transition in Initial State if Power Down bit is set to 0.

Bit #3: The meaning of this bit is controlled by the EC pin and bit #4.

If EC is pulled to V_{DD} and bit #4 is 0, the direction of data is switched with this bit, pins IN and OUT are not used at the same time. Depending on the Data Direction bit either the OUT pin is outputting the data sent by the Transponder or the IN pin is modulating the Antenna Driver. When OUT pin is used, IN pin has no influence on antenna drivers (they are always ON independent of IN pin). When IN pin is used OUT pin is always driven to VSS. Such set up allows to connect OUT and IN pin together to achieve a two wire connection in an active antenna configuration (see also figure 9. Typical operating configuration as Active Antenna).

If the EC pin is pulled to V_{SS} or left open and bit #4 is 0, the meaning of Bit #3 is different. Now it switches either the Data Comparator (output of the demodulation chain) or the Clock Reference (signal driving the antenna) divided by 32 to the OUT pin.

In case the "External clock" mode is selected with Bit #4, the EC pin is used for different purpose and the meaning of Bit #3 is independent of this pin. The bit is used for the Data/Clock selection in this case.

The state of this bit does not affect the behavior of the serial interface; in any case the serial register can be written and read by the IN and OUT pins.

Bit #4: The clock for driving the antenna and demodulating the received signal can be generated by an internal PLL if this bit is set to "0" or by an external source connected to the pin EC if Bit #4 is set to "1". In case the EC-pin is not used it should be left open or connected to VSS.

Bit #5: This decides whether the analog circuitry is doing a fast start-up or not. The settling time can be reduced from about 100ms to about 25ms if parameters like sample point or gain setting have been changed. If fast analog start-up is set it is active from falling edge of pulse 9 to the rising edge of pulse 10 on pin CLK.

Bit #6 & Bit#7: These bits control the gain of the amplifier. By combining both bits the gain can be set in four steps of 6dB. Note that Bit #6 is decreasing the gain by 50% whereas Bit #7 is increasing the gain by 100%. The default state is a gain of 480.

Bit #6, Gain setting	Bit #7, Gain setting	Gain
0	1	960
0	0	480
1	1	240
1	0	120

Bit #8: This bit switches into a test mode when set. The test mode will be left after clock pulse 13 on pin CLK. Therefore the test mode is volatile even if it has been selected by accident. Note that the functionality and pin assignment in this mode is different. It should be avoided in the application.

Bit #9 – Bit#11: These bits are the diagnostic output of the P4097. The detectable faults are an unlocked PLL (due to antenna mistuning for example), a short circuited connection to the antenna or a signal below a certain threshold. The short circuit detection is done by a voltage level comparison of the antenna driver. If the driver can not pull the output close enough to V_{SS} or V_{DD} , a short circuit is detected and the driver is switched off immediately. This state is steady until the next command is sent. In the case bit #4 is 1 (external clock) the PLL is not used, PLL-status bit is set to 0.

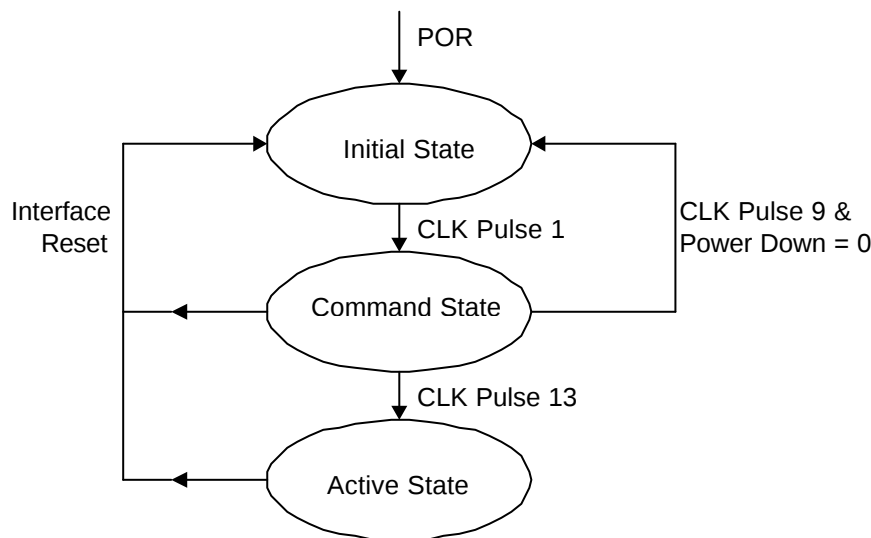


Figure 6. Serial Interface state transition diagram

Pins IN and OUT in Initial and Active state of Serial Interface:

The signal at the IN pin is modulating the antenna signal. A "high" signal switches the antenna driver on, whereas a "low" signal is forcing the antenna driver into tri-state mode to achieve a fast de-energizing of the coil.

Output OUT is behaving according to the setting in Bit #3.

12.3 Analog Blocks

The circuit performs the two functions of an RFID basestation, namely: transmission and reception. Transmission involves antenna driving and AM modulation of the RF field. The antenna driver delivers a current into the external antenna to generate the magnetic field.

Reception involves the ASK or PSK demodulation of the antenna signal which is modulated by the transponder. This is achieved by sensing the absorption modulation applied by the transponder.

Transmission

Referring to the block diagram, transmission is achieved by a Phase Locked Loop (PLL) and the antenna driver.

Driver

The antenna driver supplies the reader basestation antenna with the appropriate energy. It delivers current at the resonant frequency which is typically 125 kHz. The current delivered by the driver depends on the Q of the external resonance circuit.

To archive the maximum lifetime of the chip it is recommended that the design of the antenna circuit is done in a way that the maximum peak current of 250mA_p is not exceeded for a continuous wave application (see Application Note for antenna current calculation). If a certain pulse length is not exceeded the peak current can reach up to 400 mA_p. When such large currents are necessary in the application a thermal simulation is recommended. A limiting factor for the antenna current is the limited amount of thermal energy which could be dissipated by the package by radiation and convection. The maximum peak current should be designed in a way that the internal junction temperature does not exceed the maximum junction temperature at allowed maximum ambient temperature. 100% modulation (OOK) is done by switching off the drivers. The antenna driver is protected against antenna DC short circuit to the power supplies. If a short circuit of the antenna or from the driver to ground or supply is detected, the status "Short Circuit" (Bit #9) is set to "1".

Phase locked loop / External Clock

The clock for the antenna driver is either generated using the integrated PLL or it is connected from outside through the EC pin (External Clock Input) as 4 MHz square wave. The EC clock is divided by 32.

The PLL is composed of the loop filter, the voltage controlled oscillator (VCO) and the phase comparator blocks. By using an external capacitive divider, pin DEMOD_IN gets a divided antenna signal.

The phase of this signal is compared with the signal which is driving the antenna driver. Therefore the PLL is able to lock the carrier frequency to the resonant frequency of the antenna. Depending on the antenna type the resonant frequency of the system can be anywhere in the range from 100kHz to 150kHz. Wherever the resonant frequency is in this range it will be maintained by the phase lock loop.

Reception

The demodulation input signal for the reception block is the voltage sensed at the antenna. The DEMOD_IN pin is used as input to the reception chain. The signal level on the DEMOD_IN input must be lower than V_{DD} - 0.5V and higher than V_{SS} + 0.5V. The input level is adjusted by the use of an external capacitive divider. The additional capacitance of the divider must be compensated by an accordingly smaller resonance capacitor. The AM/PM demodulation scheme is based on the "AM Synchronous Demodulation" technique.

The reception chain is composed of a sample and hold circuit, a DC offset cancellation, a bandpass filter and a comparator. The DC voltage of the signal on DEMOD_IN is set to the AGND voltage by an internal resistor. The AM signal is sampled, synchronized with the VCO. Any DC component is removed from this signal by the CDEC capacitor. Further filtering to remove the remaining carrier

signal, as well as high- and low frequency noise, is made by a second order high pass filter and CDC. The amplified and filtered demodulated signal is fed to an asynchronous comparator. By the Sample-Point command the kind of demodulation can be chosen. The phase shift between VCO and sample frequency for both kinds of demodulations is fixed in a way that pure amplitude- and pure phase demodulation is possible. With this technique the P4097 could demodulate also the phase shift which occurs in certain tuning conditions between the transponder and the antenna circuit.

TXP-Modulation / Reference-CLK

In Active Status either the Transponder modulation information or the Reference-CLK signal is transmitted through the OUT-Pin, but only if the Modulation Bit is not set. The Reference-CLK is the Clock for the ANT1 and ANT2 Clock signal divided by 32, so that the controller can calculate the actual clock signal frequency.

13. Typical operating configuration

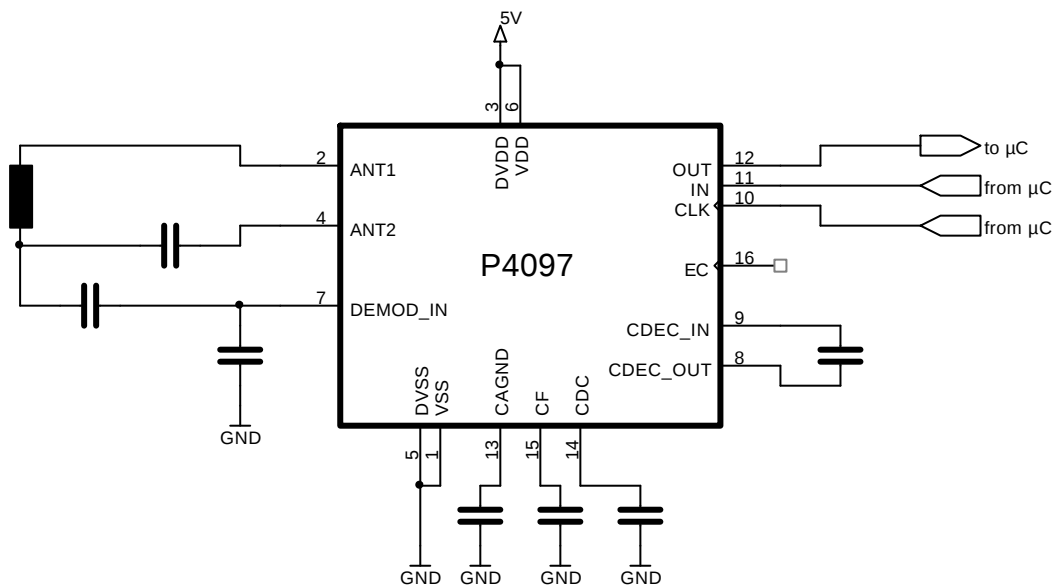


Figure 7. Typical operating configuration, with direct μC interface

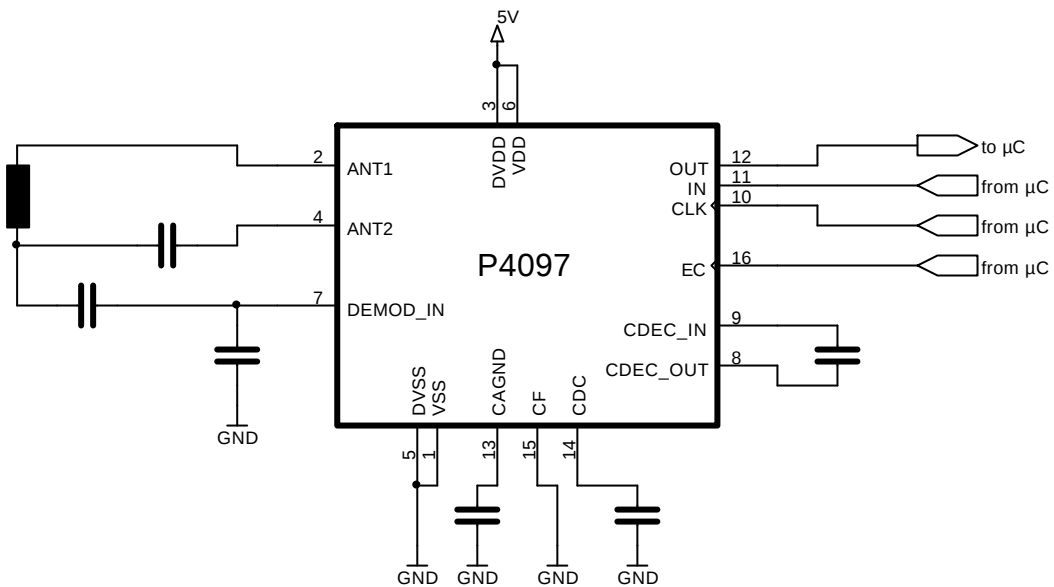


Figure 8. Typical operating configuration, with external clock

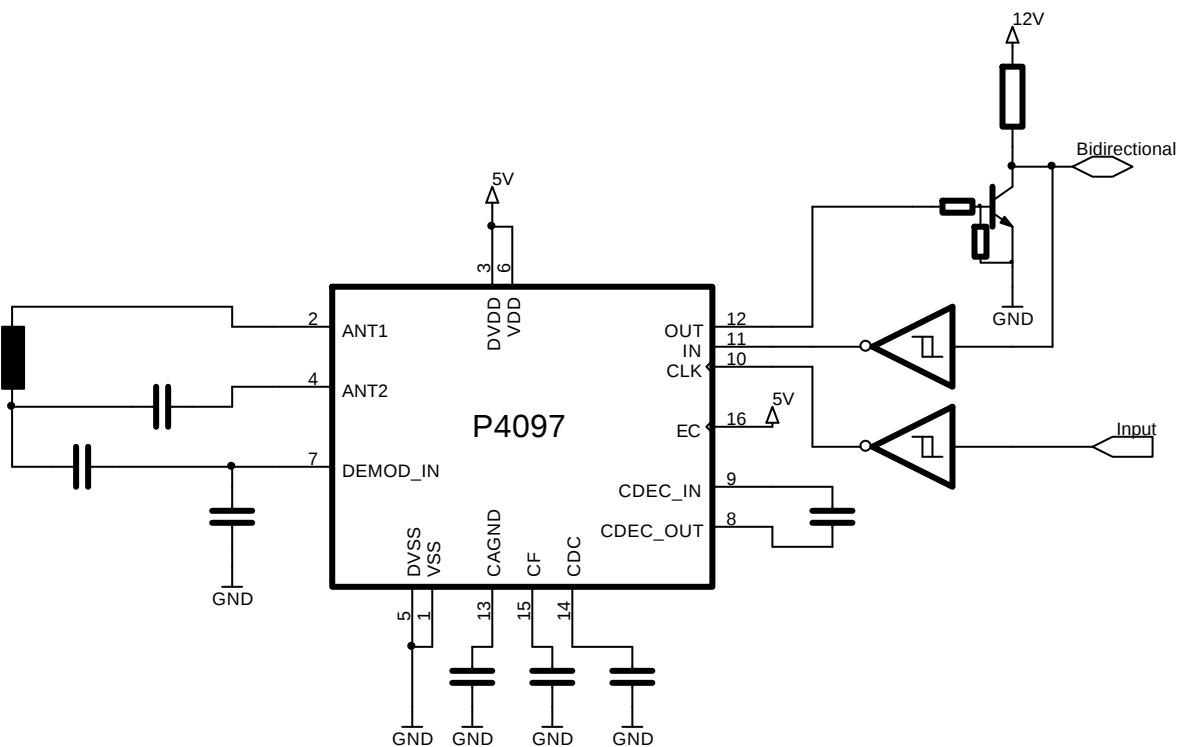
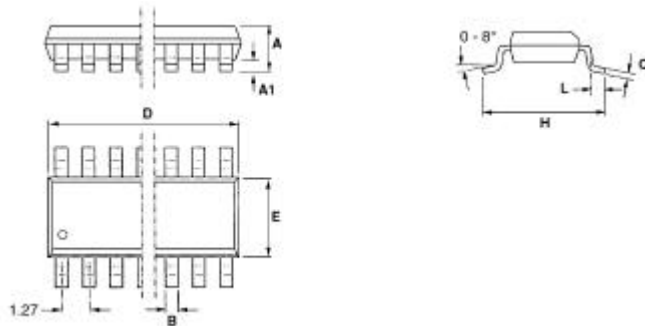


Figure 9. Typical operating configuration, as Active Antenna

14. Package and Ordering Information



Symbol	Dimensions in millimeters		
	Min.	Nom.	Max.
A	1.55	1.63	1.73
A1	0.13	0.15	0.25
B	0.35	0.41	0.49
C	0.19	0.20	0.25
D	9.80	9.93	9.98
E	3.81	3.94	3.99
H	5.84	5.99	6.20
L	0.41	0.64	0.89

Figure 10. Dimensions of SO16 Package

Ordering Information

The P4097 is available in the following package:

Part Number	Package	Description
P4097/16S	SO16	plastic small outline package; 16 leads

Life Support Applications

This product is not designed for use in life support appliances, devices, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and are fully responsible for any damages resulting from such improper use or sale.

15. Quality and Reliability Information

Wafer Sort

Each die is electrically tested at ambient temperature (25°C) to guarantee commercial DC/AC parameters and functionality.

Chip visual inspection

Visual inspection of described die is performed at high power magnification.

Visual QC gate

AQL 0.4% cumulative I.L. II.

Conventional Packages

All devices are marked with complete information for full traceability (product type, lot identification, assembly designation and date code).

Final Electrical Test

Static, functional and dynamic parameters are assessed on all devices. The assessed parameters are defined in the electrical specifications.

Package Visual Inspection

Visual inspection for bent leads, chip cracks, and finish are assessed to MIL Std. 883C Method 2009.4.

Static Protections

Inputs and outputs are protected against electrostatic discharges. The device is designed to withstand the following test:

Condition: 4kV pulse from 100pF capacitor, 1.5k Ω series resistance with reference to V_{SS} . No degradation of pad characteristic or device performance is permitted. This test is an intrinsic part of the qualification procedure.

Exception: 10kV pulse on ANT1 and ANT2.

Latch-up Protections

Inputs and outputs are protected against Latch-up. The device is designed to withstand the following test at $T_a = 25^\circ\text{C}$ ambient temperature:

Static latch-up: No latch-up triggered with $\pm 30\text{mA}$ @ maximum power supply voltage.

Dynamic latch-up: No latch-up triggered with $\pm 50\text{V}$ pulse from 220pF, 50 Ω series resistance at maximum power supply voltage, with reference to V_{SS} . These tests are part an intrinsic part of the qualification procedure.