P4097 Application Note

Designing a RFID Reader/Exciter using the P4097 integrated circuit

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Contents

1. Introduction

This application note should give supplementary information about the integrated reader/exciter circuit P4097.
The P4097 serves as interface between a transponder and a µController. The interface operates bi-directional. The transponder is supplied with energy and data by on-off keying (OOK) of the carrier signal and the transponder sends data back by modulating its quality factor (ASK/PSK).
The described circuit is a highly integrated solution for communicating with a transponder which is not limited to a specific communication protocol and can read or write all kinds of transponder as long as they use amplitude modulation. The amount of necessary external components is minimized.

Due to an integrated PLL there is no need for an external clock, the antenna circuit oscillates always on its series resonance frequency. This, and the possibility to demodulate ASK and PSK signals coming from the transponder, eliminate the "zero modulation" problem which occurs if the resonance frequency of the transponder, the reader antenna and the driving frequency are mistuned by component tolerances.
Furthermore the chip has been designed to support both, active and intelligent antenna. The difference is the proximity of the controlling µC, either it sits close to the P4097 on the same PCB or it is connected via a wiring harness where the number of wires is important and should be minimized.

Controlled by a serial interface the chip incorporates a power down mode as well as diagnostic capabilities.

2. Function Principle

The interface between the transponder and the reader/exciter works like a transformer with very large air gap and therefore a low coupling factor. The coupling factor can be visualized as ratio of the received magnetic field by the transponder to the generated magnetic field by the reader/exciter. In common applications this ratio is in the range of 0.5% to 5%.
The transponder is energized by the received magnetic field and consumes little power which is simulated by the resistor R_{txp}. When sending data the transponder switches a voltage clipping element in its resonant circuit which can be seen on the reader/exciter side as a small change of the voltage at the antenna "tab" point (the voltage between the inductor L_{ant} and the capacitor C_{ant} referenced to ground).

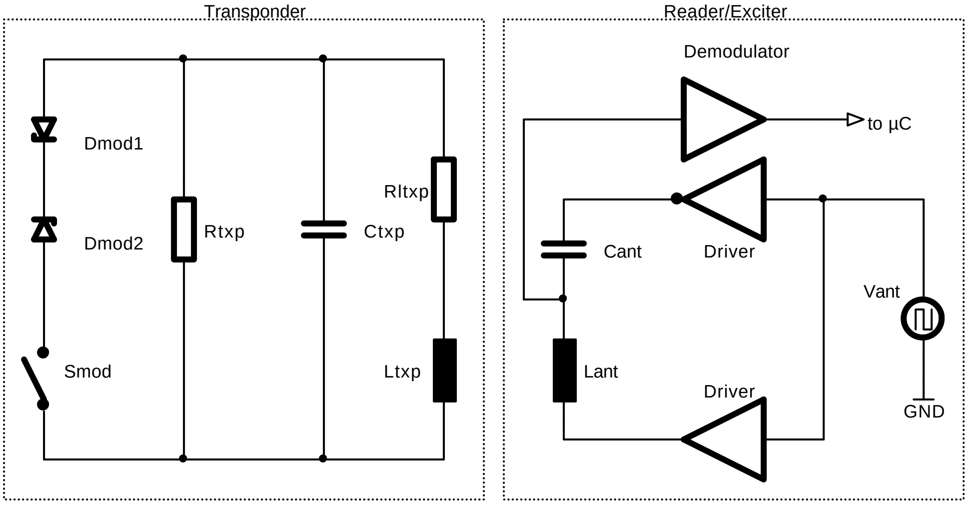


Figure 1.: Transponder Interface equivalent circuit

L_{txp} and L_{ant} form the transformer, they are coupled by a mutual inductor which is not drawn. The quality factor of both resonance circuits is determined by the resistors R_{txp}, R_{ltxp} and R_{ant} which represent the copper resistances, the eddy current losses and supply current of the transponder circuit.
To achieve a large current in the antenna with a given supply voltage and a limited quality factor a bridge configuration for the driver is chosen.

The transponder incorporates a parallel resonance circuit because a high voltage at low supply currents is needed, whereas the reader/exciter is realized using a series resonance circuit because a low supply voltage should cause a high antenna current. The series resonance circuit has a low impedance at the resonance frequency and allows high driving currents (and therefore strong magnetic fields) using a low driving voltage, the opposite is true for the parallel resonance circuit.

The voltage change at the reader/exciter antenna can be demodulated as it is modulated by the different damping of the transponder circuit (as long as the coupling factor is not too small).

If the resonance frequency of the transponder and the resonance frequency of the antenna are different the coupling factor between both coils becomes complex. This means that the modulated signal is phase shifted against the carrier signal. If this phase shift reaches 90° the signal can not be demodulated with a simple peak detector any more as the carrier is being pure phase modulated without any amplitude modulation.
To avoid this so called “zero modulation problem” and therefore increase the allowed tolerances of components the P4097 is able to detect amplitude- and phase modulation. The demodulation is done by a sampling principle where the sampling phase can be switched between 0° and 90° relative to the antenna driving voltage.

3. Hardware Design

3.1 Thermal considerations

Due to resistive losses in the antenna driver circuit and the supply current for the integrated analog circuitry the chip is generating heat during operation which is increasing the junction temperature. As mentioned in the data sheet this junction temperature shall not exceed 110°C to guarantee the electrical characteristics of the chip and therefore the functionality of the whole circuit.
The following simplified schematic is useful for calculating the junction temperature during operation.

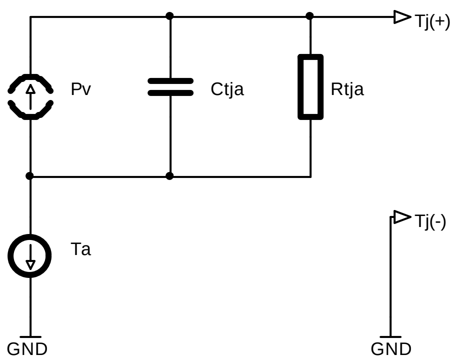


Figure 2.: Equivalent schematic for thermal calculations

In this circuit Ta is the ambient temperature, T_j is the junction temperature (to be calculated) and C_{tja} and R_{tja} are the thermal capacitance and resistance as given in the datasheet for the chip soldered on a 2 layer 1.5mm FR4 board with 35µm copper using a standard SO-16 footprint.
The current source P_v represents the power which has to be dissipated. It is calculated as follows:

$$P_V = V_{DD} \cdot I_{DDon} + \left(\frac{\hat{I}_{Ant}}{\sqrt{2}} \right)^2 \cdot R_{AD}, \text{ with } V_{SS} = 0V$$

with the antenna current determined by:

$$\hat{I}_{Ant} = \frac{4}{\Pi} \cdot \frac{V_{DD}}{R_{loop}}$$

and the loop resistance given with:

$$R_{loop} = R_{Ant} + R_{AD}$$

Putting all above into an electric circuit simulation (or using the appropriate formulas) the junction temperature even for pulsed operation at the antenna driver current limit can be calculated. The surrounding circuit, ambient temperature and the duty cycle should be chosen that by no means a junction temperature of 110°C is exceeded.

3.2 Power Supply

The circuit has to be supplied with a regulated voltage in the range given in the datasheet. The consumed current in active mode can be calculated with:

$$I_{Sup} = \frac{2}{\Pi} \cdot \hat{I}_{Ant} + I_{DDon}$$

The power supply should be able to supply this current without voltage fluctuations and ripple. This ripple on V_{DD} will be seen as modulation on the DEMOD_IN pin and can especially in the frequency range of transponder communication not be distinguished from data send by the transponder. To get a feeling for the supply voltage rejection of the circuit, as there will be always a certain amount of ripple because of non perfect components, for a typical configuration the drop of the DEMOD_IN peak voltage is 50mV if the V_{DD} is decreased by 62.5mV. The transponder itself is modulating by a few tens of mV. It can be seen that an insufficient power supply can easily cause malfunction or at least a reduction in functionally and read/write range.

As a good design practice the power supply capacitor should be split and a 10µF capacitor with a low ESR together with a ceramic 100nF capacitor are being placed in direct vicinity of the chip. A ripple voltage smaller than $5mV_{SS}$ in the frequency range between 100Hz up to 10kHz should be achieved for best results. For higher or lower frequencies the susceptibility is reduced due to the receive band pass filter.

The 10µF is needed to suppress the sourcing of antenna current into V_{DD} in case the antenna driver is being modulated. Too little capacitance together with a low power circuit will result in a lifted V_{DD} in the moment when the antenna is switched off as the voltage regulator can usually not sink current.
The 100nF ceramic capacitor supplies the output stage with the short current peaks which are drawn by the pre-driver stage when the output level changes between V_{SS} and V_{DD}. The output transistors

themselves are equipped with a “break-before-make” circuitry and do not draw a cross current. The capacitor is needed to suppress EMI.

The antenna is deenergized by diodes connected to V_{SS} and V_{DD}, the push-pull antenna drivers are in tri-state if switched off. Therefore the voltage shortly after the driver has being switched off reaches about V_{DD} + 1V and V_{SS} – 1V for a few 125kHz cycles depending on the quality factor of the antenna.

Take care that the OUT pin, connected buffers or similar, must not switch high currents. Together with a weak power supply this can form a resonant loop. The switched current modulates the supply voltage which can be seen as amplitude modulation on the DEMOD_IN which is demodulated through the chip to the OUT signal.

3.3 Filter design

The internal demodulation chain of the chip is shown below. The schematic is simplified but contains all stages of interest.

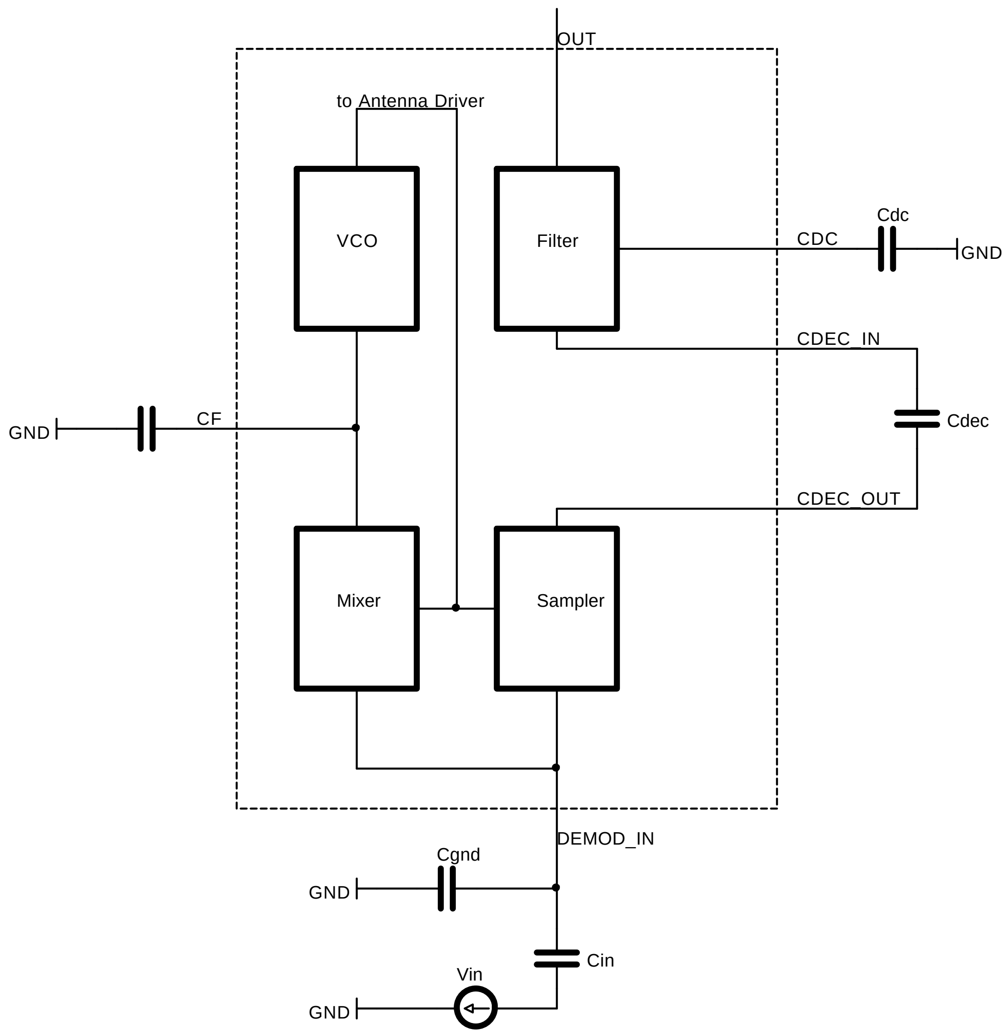


Figure 3.: Simplified internal filter configuration

The capacitive voltage divider coming from the antenna tab point to the DEMOD_IN pin should be dimensioned so that the voltage level never exceeds V_{SS} + 0.5V or V_{DD} – 0.5V. Above or below these thresholds the signal will be clipped and the modulation of this signal is lost. On the other hand the signal should not be smaller than necessary because the absolute level of modulation should be as large as possible to achieve a maximum system performance.
When choosing the values and the tolerance class for this voltage divider (C_{in} and C_{gnd} in the drawing) all component tolerances and the variation of antenna quality and resonance frequency over temperature and part variations should be regarded.

The low pass and high pass filter frequency of the band pass filter following the sampler can be chosen by the external capacitors connected to CDEC and CDC. They should match with the data rate and the modulation spectrum of the used transponder. Recommended values are given in the datasheet.

The low pass filter frequency of the mixer which controls the VCO can be chosen by the external capacitor connected to CF. The smaller the value is, the faster the settle time is to find the series resonance of the antenna circuit after starting the antenna driver.
When the capacitance value is selected too small the VCO follows the phase modulation which is generated by a transponder with a detuned resonance frequency (zero modulation effect). This affects the phase demodulation and is only recommended if the sample point of the demodulator is always set on amplitude demodulation (bit#1 set to "0").
Recommended capacitor values for ASK and ASK/PSK are given in the datasheet.
When the external clock mode is used this capacitor is not needed and the CF pin should be connected to ground.

The gain of the involved amplifiers can be selected by using bit#6 and bit#7 of the serial shift register. The influence of different gains should be tested by qualification. In general the sensitivity is increased with higher gains but the chance of signal clipping and therefore the loss of functionality is also increased. To easy the gain selection the voltage levels at CEDEC_OUT, CEDEC_IN and CDC can be monitored. Clipping may occur above V_{DD} – 0.5V or below V_{SS} + 0.5V and shall be avoided considering all tolerances and drifts.

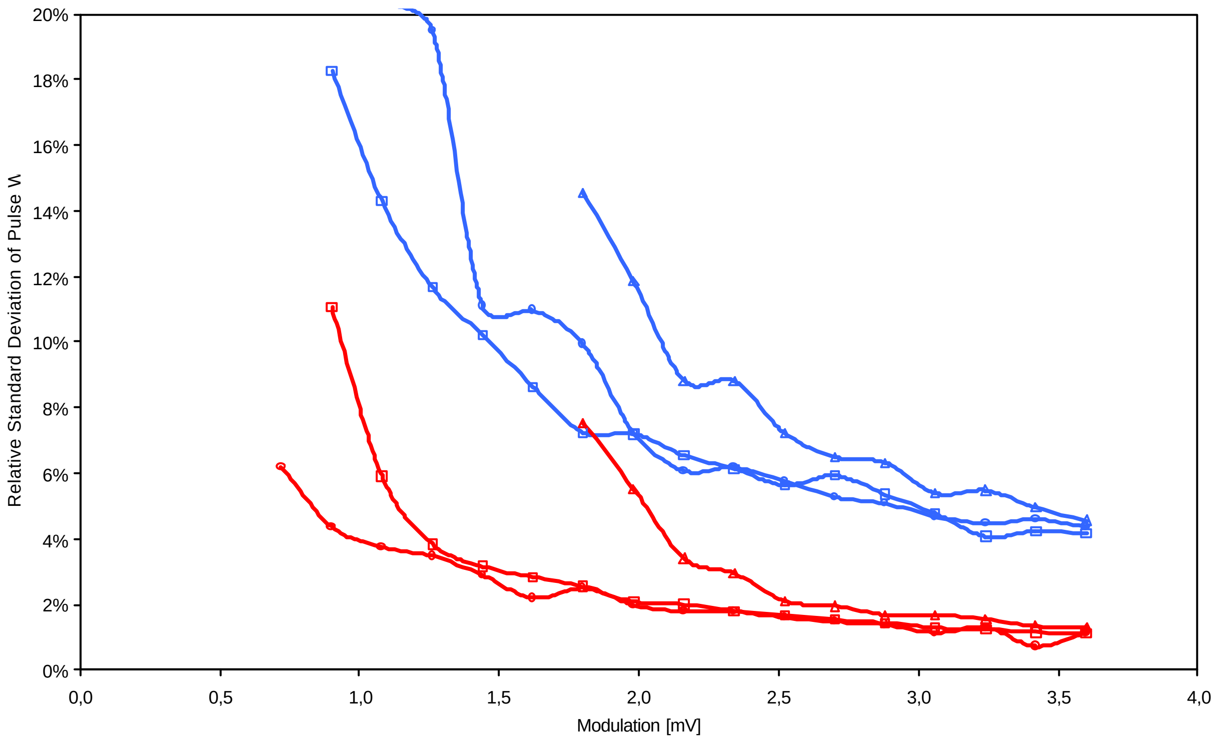
The comparator threshold and its hysteresis can not be modified externally. They are derived from the internal reference voltage which shall be buffered properly. Voltage ripple on the ground pin of the connected capacitor relative to the V_{SS} pin affects the system performance seriously.

If the internal PLL is used for clock generation the ASK and PSK channel are different in their sensitivity if a certain bit failure rate is used to determine whether the received signal is valid or not. The reason for that is the phase jitter of the PLL which generates noise when the phase of the signal is demodulated. This noise causes a jitter on the pulse length of the digital output.

In general the communication range for the PSK channel is slightly reduced in comparison with the ASK channel when using the PLL. On the other hand the PSK channel is needed in PLL mode only when very large tolerances of transponder- and antenna resonance frequencies have to be covered.

When a low jitter external clock is used the performance of the ASK channel and the PSK channel is the same.

The jitter of the demodulated signal as function of signal strength with the gain as parameter for the ASK and PSK channel can be seen on the figure below.



Red trace:	Amplitude demodulation	Circle:	Gain 960
Blue trace:	Phase demodulation	Square:	Gain 480
		Triangle:	Gain 240

Figure 4.: Jitter as function of modulation depth

The diagram shows that the sensitivity is typically about 0.5mV, 1mV and 2mV for a gain of 960, 480 and 240. If the jitter is regarded a gain of 480 achieves the best result for both, the phase and the amplitude demodulation.

3.4 Phase Lock Loop

With the help of the PLL the antenna is driven with it's series resonance frequency. The input signal for this PLL is the signal at the DEMOD_IN pin, the same signal which is demodulated.
Therefore the phase of this signal relative to the antenna driver signal is important as the PLL will not lock correctly with shifted signals. This is the reason for choosing a capacitive voltage divider for the DEMOD_IN pin as the phase shift is not affected by parasitic capacitance caused by the PCB tracks or the pin to pin spacing.
For the same reason the polarity of the ANT1 and ANT2 antenna driver pins is important. The PLL locks only if the ANT2 pin is connected to the DEMOD_IN pin via the series resonance capacitor, not the via the coil. Swapping ANT2 and ANT1 or the capacitor and the inductor causes a 180° phase shift and the PLL is not able to lock which means the antenna is driven on the wrong frequency.

The lock frequency of the PLL is preserved as analog voltage in the external capacitor during the modulation of the antenna driver. When the antenna is switched on again this hold mode is switched off after a few 50µs. The antenna voltage has reached a steady state then and the PLL can continue working with the same voltage level as before the modulation. If the antenna is continuously modulated with a frequency of more than 2.5kHz the chip is not able to leave this hold mode. Therefore the frequency of the PLL will drift away as the capacitors are discharged by leakage currents. This is a process with a time constant at room temperature of minutes.

3.5 µC Interface

The inputs of the P4097 are IN, CLK and EC. All three pins are pulled down by a resistor with a typical value of 50kΩ. The switching threshold is typical 50% of V_{DD}. However, when using the worst case values the connected µController should be able to source at least 140µA at V_{DD} = 5V to achieve a proper logic high level. This requires a R_{DSon} of the p-channel FET (or a pull up) in the µController with a value of less than 10.7kΩ.

The output OUT of the P4097 is a push-pull type with a worst case R_{DSon} of about 500Ω. A typical value at room temperature is between 150Ω and 200Ω.To achieve proper logic levels the load resistance should be above 4.9kΩ. Due to the limited sink or source current the output is short circuit protected against V_{SS} and V_{DD}.

Care should be taken when the chip is not interfaced directly to a µController. The slew rate of the clock signal should be high enough to achieve rise or fall times below 50ns. The chip is generating a current spike during the polarity change of the 125kHz carrier signal (as any CMOS output) which can crosstalk via ground into the clock signal. As the input does not incorporate any hysteresis only a sufficient rise time guarantees that a clock pulse is not counted twice. Connected directly to a µController the rise time should never cause a problem if a direct connection without additional filter capacitors is chosen.

3.6 Active antenna interface

When the IN and OUT pin are connected together to form with the CLK signal a two wire interface this configuration is called active antenna. It is advantageous if the antenna interface is a stand alone unit without a µController. The wiring harness is then reduced to two supply wires plus two wires for the digital interface.

Because the OUT signal would modulate via the IN pin the antenna driver, both signals must be decoupled via the data direction bit of the serial interface. This bit is enabled via the EC pin which is not used if the P4097 is running with its own PLL and without an external clock.

The data direction bit is switching the interface between input and output. If in input mode the OUT pin is pulled to ground. If in output mode the IN pin has no function but the antenna driver stays switched on. This mode is left by an interface reset.

A simple transistor stage can form the interface to the wiring harness as shown in the chapter “modes of operation” later in this application note.

3.7 Printed circuit board

To achieve the maximum communication range the following design rules for the printed circuit board should be regarded.
The V_{SS} pin is the reference level for all analog signals. The antenna driver current which is sourced out of the DV_{SS} pin shall not have a common path with these analog signals.

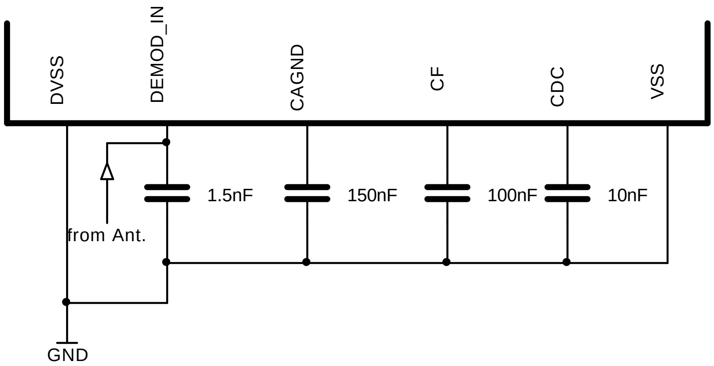


Figure 5.: Ground signal layout

The buffer capacitors should be located close between the DV_{DD} and DV_{SS} pins. Any voltage drop due to copper resistance or track inductance will be seen via the antenna on the DEMOD_IN pin and will be demodulated. This should be regarded for the larger electrolytic capacitor as well as for the ceramic capacitor. Using two sets of capacitors makes it easier to place and route them on the circuit board. One set is buffering the high current supply DV_{DD} and DV_{SS}, whereas the other capacitors (or just the ceramic one) buffers the analog supply V_{DD} and V_{SS}.

The signal DEMOD_IN is very susceptible against capacitive coupling of noisy tracks. The capacitive voltage divider should be located close to the input pin and connected to a proper analog ground. A ripple voltage or a voltage drop relative to V_{SS} is coupled into the DEMOD_IN pin due to the capacitor ratio much stronger than the useful signal coming from the antenna.

The CDEC capacitor which connects the sampler with the filter is susceptible against capacitive coupling of noise. The capacitor should be located close to the chip and the tracks should be short and not close to other traces with fast changing voltage levels.

The antenna connection, if an external antenna is used, should be bypassed with two small ceramic capacitors to ground close to the connector. This suppresses high frequency voltages to ground which are picked up by the wiring harness and reduces the radiation out of the circuit into the wiring harness. Other connector pins which are connected to a wiring harness should be treated similar. The ground plane to which these capacitors are connected should be routed carefully to achieve a low impedance for high frequencies.

Unused pins except the CF pin in external clock mode can be left open as the inputs are internally pulled to ground and outputs are push-pull types without tri-state mode and therfore defined voltage levels.

3.8 EMI Filter

In applications where the functionality even under the influence of strong electromagnetic fields is required, additional filter circuitry for connecting the antenna coil with the P4097 is recommended. The filter shown below suppresses high frequent voltages which could be picked up by the antenna cable or the antenna itself. Because of the –60dB level of the useful transponder signal in relation to the 125kHz carrier frequency the communication is by nature susceptible against electromagnetic interference.

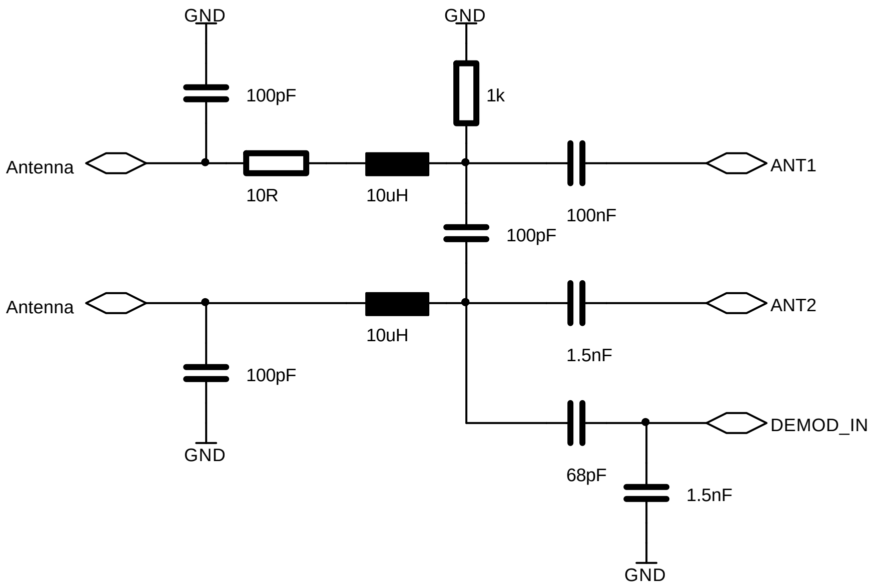


Figure 6.: EMI filter circuit

If the quality factor trimming resistor value is large enough it may be split equally on both antenna connections and may replace the 10µH inductors. The susceptibility against interference is increased compared to the inductor solution, especially for higher frequencies, but may be still sufficient for the given application.
The short circuit protection is done in this example with the capacitive decoupling of both antenna drivers. The smaller capacitor determines the resonance frequency together with the inductance of the coil. It is a low tolerant, low temperature drift, high voltage type. The larger capacitor should be in relation 10 to 100 times larger so that a low voltage and high tolerance type can be used. The larger the capacitance, the lower is the influence on the resonance frequency.

3.9 Antenna diagnosis

The P4097 contains three kinds of inspecting the antenna circuit.

Both output stages are tested internally for correct voltage levels. The driven voltage level and the actual voltage level at the output pin are compared each cycle and the output stage is switched into tri-state mode when the output does not reach the assumed voltage. This feature protects the P- and N-channel driver transistor against destruction by short circuit to V_{SS} or V_{DD}. The occurrence of these short circuits can be read back by the connected µController through the serial shift register.

A typical current threshold for switching off the output stage is 600mA. If the short circuit happens during normal operation it will be switched off after 4µs at the latest when running with 125kHz carrier frequency. If the circuit is powered up into a short circuit the current will be switched off as soon as the internal (PLL) or external (EC) clock is present. In case the chip is using its PLL the short circuit path is interrupted after about 300µs. If the circuit has to deal with such states the power supply has to be designed appropriate as the current can reach up to 1.5A. The power supply requirements are reduced by inserting the series capacitor as described in the chapter above.

The drivers stay switched off until they are activated at the next writing of the serial shift register.

The signal at the DEMOD_IN pin does reach a certain voltage level during normal operation. It is the antenna tab voltage decreased by an capacitive voltage divider. If this voltage is lower than a fixed limit shown in the datasheet the input status bit is set. This indicates a broken antenna or connection to the antenna, or in general a too low quality factor of the antenna.

The status of the phase lock loop is outputted in a third bit of the serial shift register. It shows the mistuning of the antenna loop, which means the PLL could not lock to a frequency in a certain range. This shows a broken or short circuited antenna connection or wrong values for inductance or capacitance of the antenna loop, or in general a wrong resonance frequency of the antenna.

All three bits are not logical connected with each other. A single failure can cause one or more failure flags to occur. The pattern has to be interpreted by the µController if necessary.

Failure mode	Antenna Status	Input Status	PLL-Status
Short circuit of ANT1 to V_{SS}	1	X	0
Short circuit of ANT1 to V_{DD}	1	X	0
Short circuit of ANT2 to V_{SS}	1	1	1
Short circuit of ANT2 to V_{DD}	1	1	1
Broken connection to ANT1	0	1	1
Broken connection to ANT2	0	1	1
Capacitor value too large	0	X	1
Capacitor value too small	0	X	1
Inductor value too large	0	X	1
Inductor value too small	0	X	1
Loop resistance value too large	0	0	0
Loop resistance value too small	X	1	0
Antenna voltage is being modulated (no failure)	0	1	0

The X's are showing an undefined status. Depending on the safety margin of the design, the bit could be read as “0” or “1”.

If the antenna driver is switched off during communication with the transponder, the PLL will loose is tuning state depending on the time constant determined by the external capacitor connected to the pin CF. If the driver is switched off for a long time the PLL-Status bit will show a “1”.

Testing of the antenna status bits should only be done if the antenna voltage is at its normal constant level. This means it shall not be tested in power down mode, during write pulses and in settling phases because the diagnostic information might be unclear.

A more precise antenna diagnosis can be done by using the OUT pin as clock output. By setting the data/clock bit in the serial shift register the actual PLL frequency divided by 32 can be seen at the OUT pin. The connected µController can measure with a pulse counting or gated timer the exact resonance frequency and compare it with given limits. These limits are usually much more narrow than the PLL locking range is.

4. Antenna Design

The reader/exciter antenna is a series resonance circuit which consists of an inductor, a capacitor and a resistor. The characterizing variables of this circuit are the resonance frequency f_{res} and the quality factor Q.

The resonance frequency is calculated with:

$$f_{res} = \frac{1}{2 \cdot \Pi \cdot \sqrt{L \cdot C}}$$

The quality factor is given with:

$$Q = \frac{2 \cdot \Pi \cdot f_{res} \cdot L}{R}$$

The resistor R should be measured at the resonance frequency for the case that magnetic or electric conductive material is located in the vicinity of the coil. R is then the sum of resistive, eddy current and hysteresis losses. Furthermore the resistive losses are the sum of the copper resistance of the antenna, possibly the parasitic resistance of EMC coils and the resistance of the antenna driver, given in the datasheet as R_{AD}.
For measuring the value of Q the voltage over the inductor or the capacitor can be used. The formula is given as:

$$\hat{V}_L = Q \cdot \frac{4}{\Pi} \cdot V_{DD}$$

Not only the voltage over C and L are linear dependant from Q, also the current through the series resonance circuit depends from Q.

$$\hat{I}_{Ant} = \frac{4}{\Pi} \cdot \frac{V_{DD}}{R}$$

This current should be chosen with regard to the datasheet, there are three limits to pay attention to, one for continuous operation, the other for pulsed operation and the third is the resulting power dissipation affecting the chip temperature. Violating these limits will affect the performance or the lifetime of the chip.

To get a feeling for the antenna parameters the current as function of Q for different quality factors is drawn in the figure below.

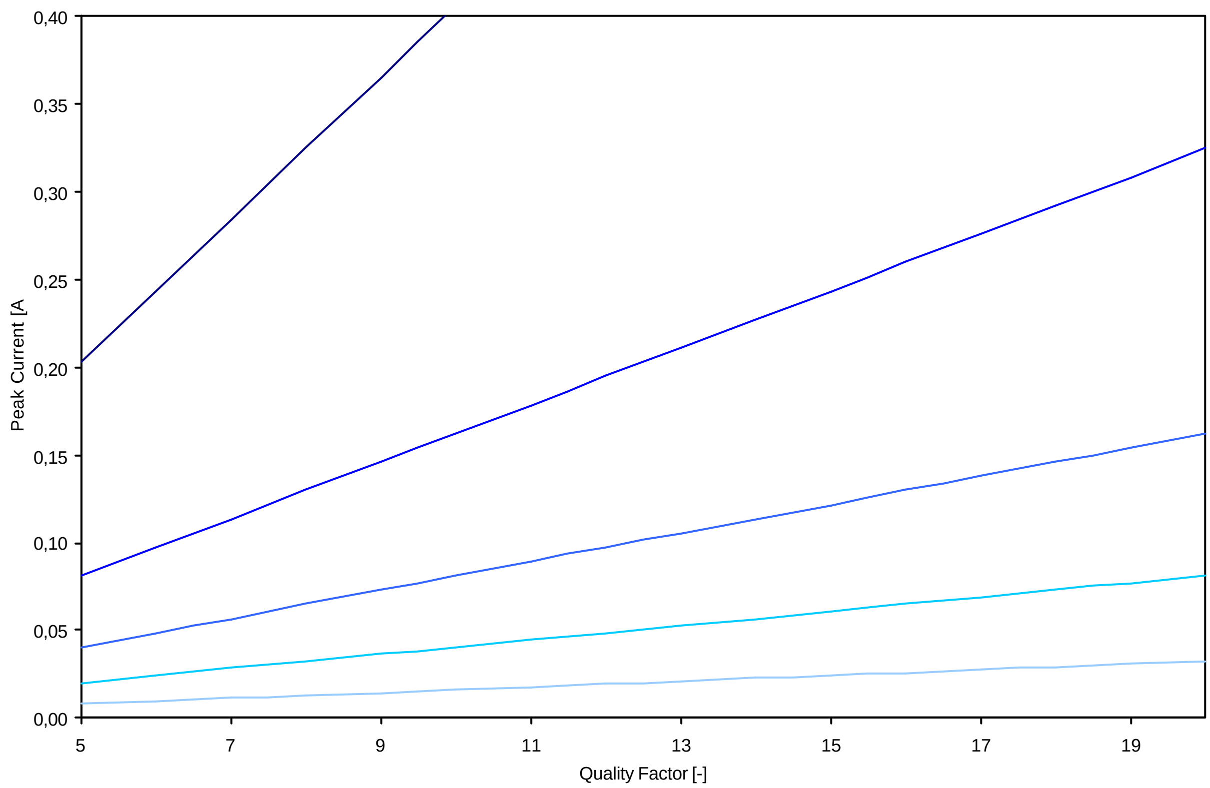


Figure 7.: Antenna peak current as function of quality factor with L as parameter

The goal is to achieve a maximum of magnetic flux to gain a large reading range. The flux is proportional to the current and proportional to the number of windings, but the number of windings are proportional to root of the inductivity.
To optimize the reading range the antenna current should be therefore maximized. With a given quality factor the necessary inductivity can be found in the diagram. The inductivity as parameter is 200µH, 500µH, 1mH, 2mH and 5mH from top to bottom.

The quality factor should be as high as possible but is limited by the susceptibility against component value deviations and the necessary bandwidth for the communication. Usually quality factors are in the range of 10 to 15.

To maximize the current instead of maximizing the inductivity has the other advantage of avoiding excessive high antenna voltages. This makes it easier and less expensive to find the appropriate electronic components and results in a smaller division factor for the DEMOD_IN voltage. Therefore the modulation ratio is kept larger.

To achieve the lowest cost for the antenna the needed resistance for the desired quality factor could be integrated as copper resistance in the antenna. However the copper resistance has a large temperature dependency and a large absolute tolerance. If the system qualification shows that this tolerance in the quality factor can not be tolerated the antenna wire size has to be increased and an external low tolerant resistor has to be used. The usage of magnetic conductive but electrical insulating material, like ferrite, is another method to reduce the quality factor at a given geometry.

If the antenna coil is not located on the same PCB as the reader chip, it is recommended to use a cable to the antenna which is not longer than 50cm. If a longer connection is necessary a shielded cable may be required or the system performance will be reduced.

With the length of the connection the susceptibility against EMI is increased. Also the electrical parameters of the cable and their tolerances or drift over temperature are becoming important with increasing length.
For architectures where 50cm are by far exceeded the use of an active antenna is recommended. The digital signals can be carried over a large distance as susceptibility against injected noise is reduced.

5. Software Design

5.1 Timing considerations

When writing software to interface with the P4097 which is running in PLL mode without an external clock it is important to have in mind that the antenna frequency which is the clock for the transponder, is generated by a PLL and the frequency therefore depends on the component values and their deviation over temperature and manufacturing tolerances.

If the resonance frequency can shift more than about 2% over tolerances and temperature it is strongly recommended to achieve a reliable reader design to measure the actual resonance frequency by software and do the complete read and write timing with the transponder relative to the measured frequency.
For that reason the serial interface can be programmed with bit#3 of the command register to output the PLL frequency divided by 32. For some transponders this is already the bit length.

The exact value for the allowed tolerance in resonance frequency depends on the used transponder. The more stringent it’s timing requirements is or the more bits are transferred without synchronization the lower the allowed tolerances are.

Errors due to desynchronization are hard to find and are often dependent on the data value which is sent or received. The effect could be that some fix code transponders could not be read, depending on their serial number, or crypt code transponders do not work with certain random numbers. Such a “random” behaviour is not easy to debug.

To avoid such errors and to be able to use less expensive and higher tolerance components it is a good design practice to derive all timings from the transponder clock which is the antenna frequency.

5.2 Interface requirements

As described in the datasheet the signals CLK and IN are used to enter data into the serial interface and do the interface reset. Because of this combined functionality it is important to control the rising edges of both signals.

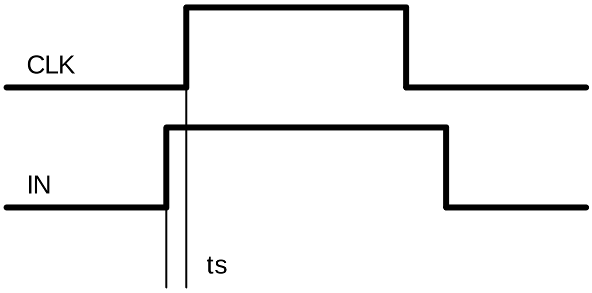


Figure 8.: Entering data into the serial interface

The figure above shows how to enter the value “1” into the serial interface. IN has to be high at least t_S before the rising edge of CLK. The value for t_S is given in the datasheet. If this time is chosen to small or even negative (CLK before IN) the data might not be accepted or the serial interface reset could be activated. The relative position of the falling edges is uncritical.

The interface reset with which every serial communication starts is done as defined in the specification when a rising edge on IN happens while CLK is high.

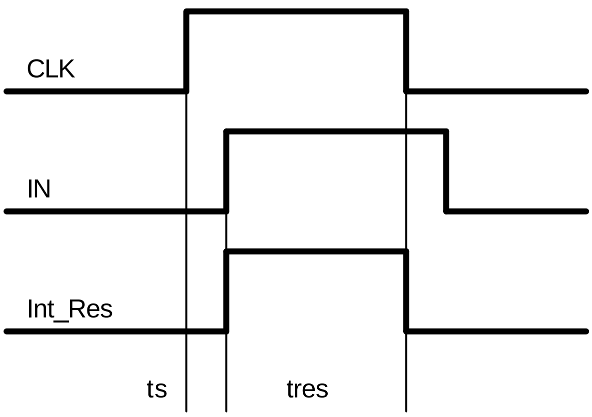


Figure 9.: Interface reset

It is recommended that the rising edge on IN appears at least a settle time of t_s after the rising edge of CLK. The internal reset is active as long as both signal are high. This time should exceed the minimum t_{res} given in the datasheet. The falling edges of both signals are uncritical, it can have any order.

It is necessary to start each writing to the serial shift register with a interface reset. By mistake the P4097 shift register and the connected µController could not be in phase due to EMI or ESD influence. In this case the written or read information would be wrong and it is difficult for the µController to figure this out. For that reason the P4097 is designed to be synchronized at each serial transmission with the interface reset.

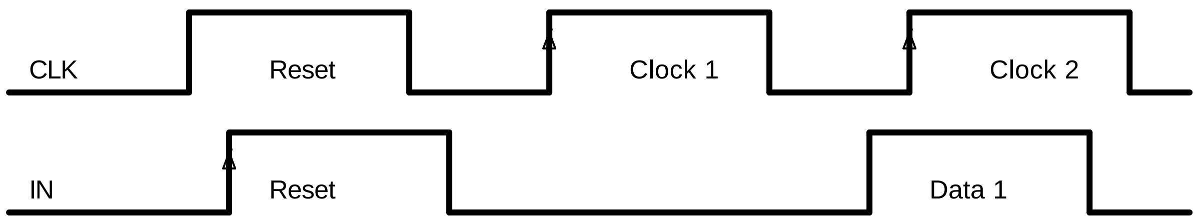
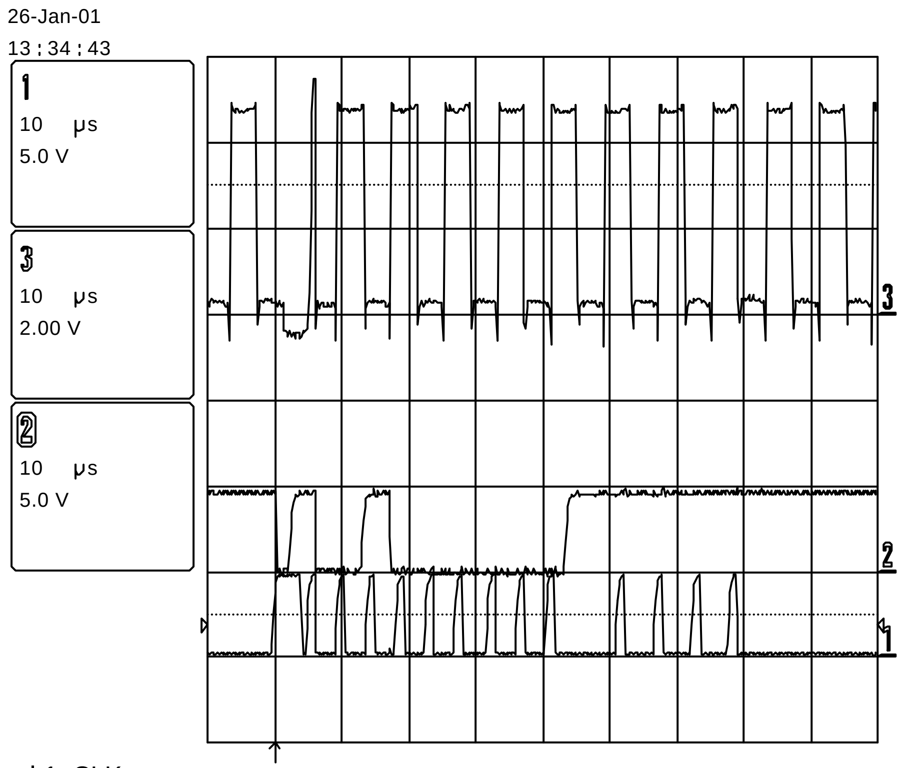


Figure 10.: Start of communication

A valid serial command to power up the chip is shown below. It starts with a interface reset to bring the IC in the command state. Because the IN pin has to be low to achieve this a momentary modulation of the antenna driver can not be avoided.
The In pin should be pulled high between the 9th and the 12th clock pulse to avoid modulation at the end of data transmission.

The pause between the first 8 bits which are input for the chip and the last 3 bits which are the output should be made longer as shown as due to the analog settle time the outputted data might be wrong.

The recommended pause length depends on the written data and is described in the specification of the P4097. Violating this pause may cause wrong status bit information. Writing the same data in the shift register after the recommended pause duration again without a delay between the 9^{th} and 10^{th} clock cycle results in a correct status output.



Channel 1: CLK
Channel 2: IN
Channel 3: ANT2

Figure 11.: Serial command sequence

5.3 Modes of operation

The P4097 is able to be used in three different system architectures or modes.

		Clock source	
		Internal PLL	External clock
µController location	Direct Interface	yes	yes
	Active Antenna	yes	no

The clock for the antenna can be internally generated by a PLL. The frequency is then determined by the resonance frequency of the antenna series resonance circuit. The other possibility is to connect an external clock to the EC pin and drive the antenna with a fixed frequency. In this case the EC pin can not be used to switch the meaning of bit#3 of the serial shift register. Therefore the combination of external clock (the EC pin is used) and active antenna (data direction of bit#3 must be used) is not feasible.

The interface to the µController can be a three wire or a two wire connection. The two wire interface should reduce the number of wires if the P4097 is connected via a wiring harness to the µController. This configuration is called active antenna. The configuration with the µController on board is called intelligent antenna.

One of the three possible architectures is the direct µController interface. This requires a µController close to the P4097 which is connected via a three wire interface to the chip.

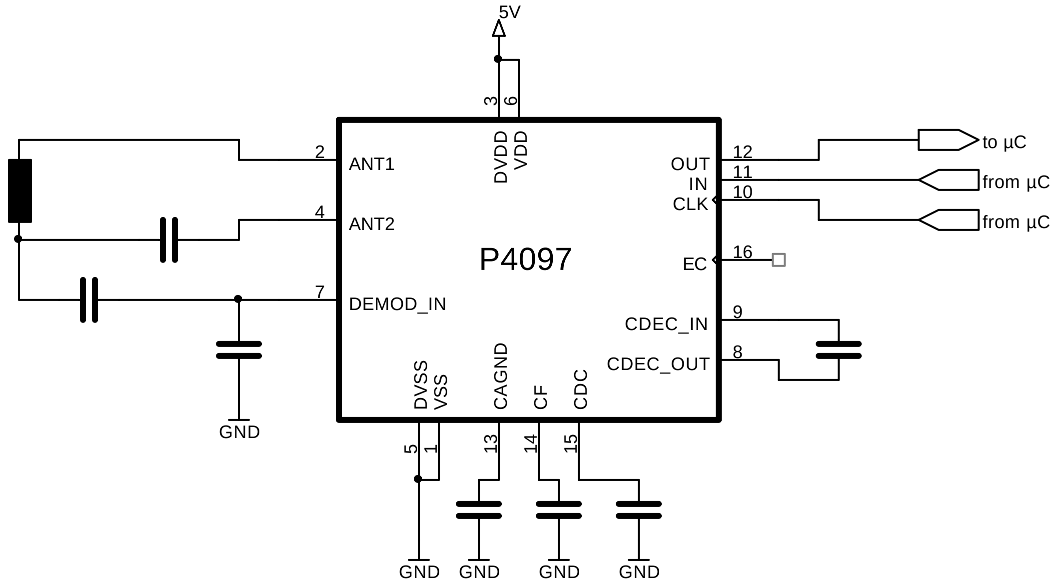


Figure 12.: Direct µController interface

The communication to the chip (writing into the serial shift register) is done synchronously by using the CLK signal. Diagnosis information is transmitted at the second half of writing into the serial shift register to the µController by using the CLK signal as well.
Data from the transponder through the chip are transmitted asynchronously, without using the CLK signal, depending on the used transponder, for example Manchester coded. In this configuration the EC pin can be left unconnected as it is pulled internally to V_{SS}. This configuration uses the PLL for the antenna clock generation.

The second architecture is the direct µController interface with external clock. The difference is the usage of a fixed antenna frequency which does not depend on the series resonance.

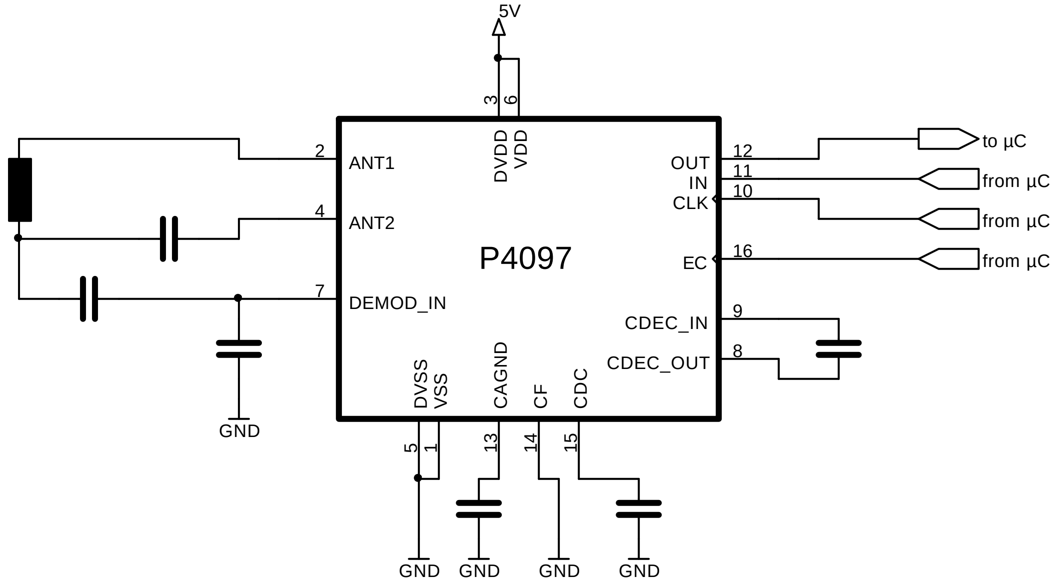


Figure 13.: External clock

The division factor between EC pin and antenna driver is 32 and fixed. Therefore the external clock has to have a 4MHz frequency when using a 125kHz transponder. 125kHz is then the carrier frequency for the data and energy transmission. Care should be taken when routing this high frequency signal from the source to the chip. To avoid electromagnetic emission the clock source should be located close to the P4097. The slew rate should not be higher than necessary.

If a crystal is shared between the µController and the P4097, the additional capacitance of the trace and the input should not be disregarded to achieve a stable start up. The input capacitace is given in the datasheet. Capacitive coupling in of high frequency signals must be avoided.
Any jitter on this signal reduces the system performance, µController using a PLL for clock generation have to be checked carefully on their clock signal stability.
The CF pin is connected to ground as the internal VCO is not needed.

The third possible architecture is called active antenna. The µController is connected via a wiring harness with the P4097. For that reason the IN and OUT pins are connected together and share one wire. For a proper communication the EC pin must be connected to V_{SS} and the bit#4 shall be set to “0”. The internal PLL has to be used and the IN and OUT have to be suppressed mutually using the bit#3.

A clock buffer has to be used to achieve the desired switching thresholds and rise times and to suppress noise on the line by using a input hysteresis.

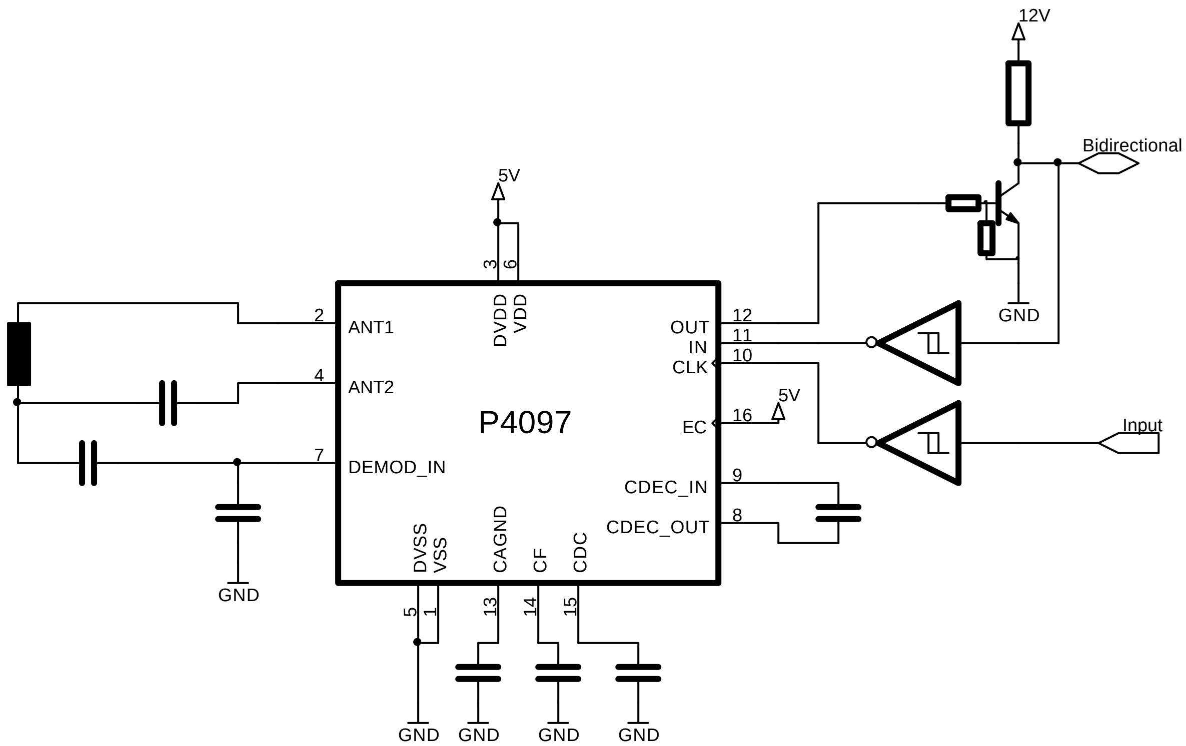


Figure 14.: Active antenna

Because the OUT pin can not be switched to tri-state a wired "or" connection must be used. A logic low signal at the OUT pin should not influence the voltage level on the bi-directional communication line. If the OUT pin is switched to low the line is used as input.

5.4 Typical Schematic

A typical circuit for interfacing a transponder may look like shown below.

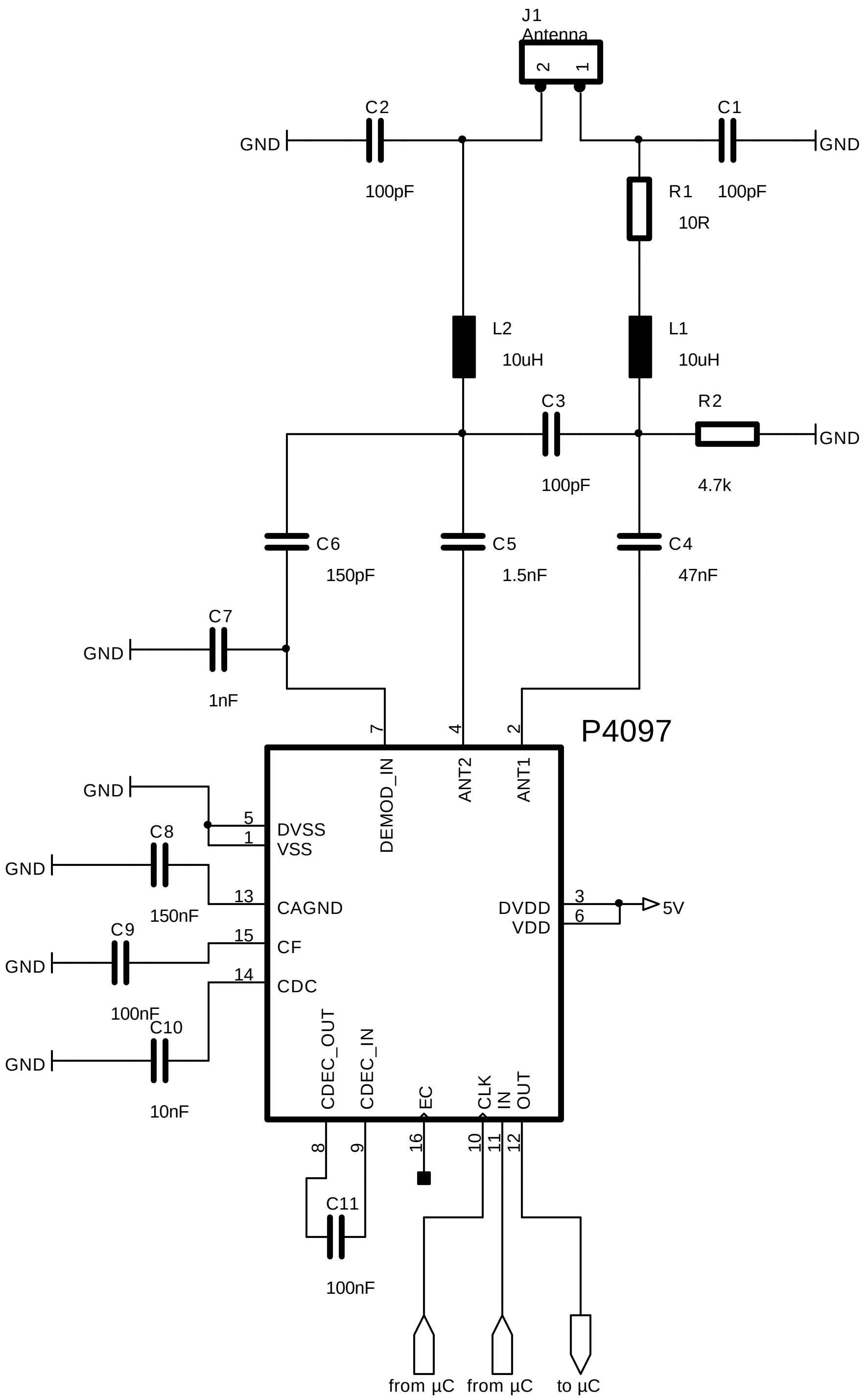


Figure 15.: Typical application schematic

The data of the connected antenna coil are L=1070µH and R=65Ω at 125kHz. This includes the cable and the eddy current losses of the lock cylinder.