Wireless Headset System
Base Unit, Model: RDA444-UNLEASH
Technical Description

reason
PRODUCTS

Wireless Headset System
Base Unit Model: RDA444-UNLEASH

The Unleash wireless headset system is a fully integrated time division duplexed (TDD) digital communication system designed for use as wireless short range audio link for mobile phones or similar devices. The system transmits a gaussian minimum shift keyed (GMSK) magnetic field between the base station and headset station . The headset uses a single magnetic coil for both transmit and receive. Spatial diversity is achieved through three orthogonal magnetic coils in the base, allowing the system to select the antenna axis that results in the optimum signal to noise ratio (lowest ber) for the link. Near-field magnetic transmission allows a lower cost system that makes more efficient use of power and space compared to conventional RF approaches.

The system is able to operate on the two channels and utilize the "listen-before-talk" algorithm to choose one of them with less interference.

The system based on the LibertyLink single chip full duplex wireless transceiver consisting of a receiver, transmitter, codec, frequency synthesizer, microprocessor and memory. This same chip is used for the base and headset implementations with only minor circuit and firmware changes. The LibertyLink is fully integrated and only a handful of low-cost and readily available external components are needed to make a complete system. The versatile microprocessor firmware can be programmed to suit many specialized applications.

1. Base Unit

The base unit connects to the mobile phone and serves as the master for the headset application. It uses the same LibertyLink chip as the headset unit in a slightly different configuration. The major off-chip components are identical to the headset, however, to provide spatial diversity for the system, the base front-end employs three antenna coils. The base unit has two volume buttons, one for volume up and one for volume down.

Most of the off-chip function blocks for the base unit are identical to the headset. The two main differences are the front-end transmitter/receiver and the host device interface.

2. LibertyLink ASIC Tranceiver

The LibertyLink chip is supports full duplex transmission of audio and data. For discussion purposes, the system is broken down into five sections; the receiver, the transmitter, synthesizer timing block, microcontroller and the off-chip front-end. The LibertyLink block-diagram is shown on the Fig.1

The receiver chain is made up of an off-chip antenna block, a low noise amplifier, the IF strip, down converters, the detector, the CVSD decoder and audio output stage. Each of these are discussed in detail in the next section.

The transmitter chain consists of the following blocks; audio input stage, CVSD encoder, GMSK modulator, coil driver, and off-chip antenna block. Each functional block is described in more detail below.

The transmitter chain can convert line level audio into a GMSK modulated signal that is applied to the transmit/receive coils. The digitally encoded audio signal is not transmitted continuously over time, rather, each end of the system alternates between transmit and receive in 1.4 millisecond bursts or frames. This allows a single antenna for both transmit and receive modes and eliminates the possibility of the transmitter crosstalk into the receiver.

The synthesizer/timing block, based on a low cost crystal, provides local oscillator and reference clocks for the RF and baseband sections.

The microprocessor/control section and specialized functional blocks control almost every aspect of the system's operation. It is composed of a microprocessor core, MMU controller, DMA unit, link controller, a UART, an audio randomizer and derandomizer, watchdog timer, a timer/counter, a power manager, a user interface controller, and a system control block.

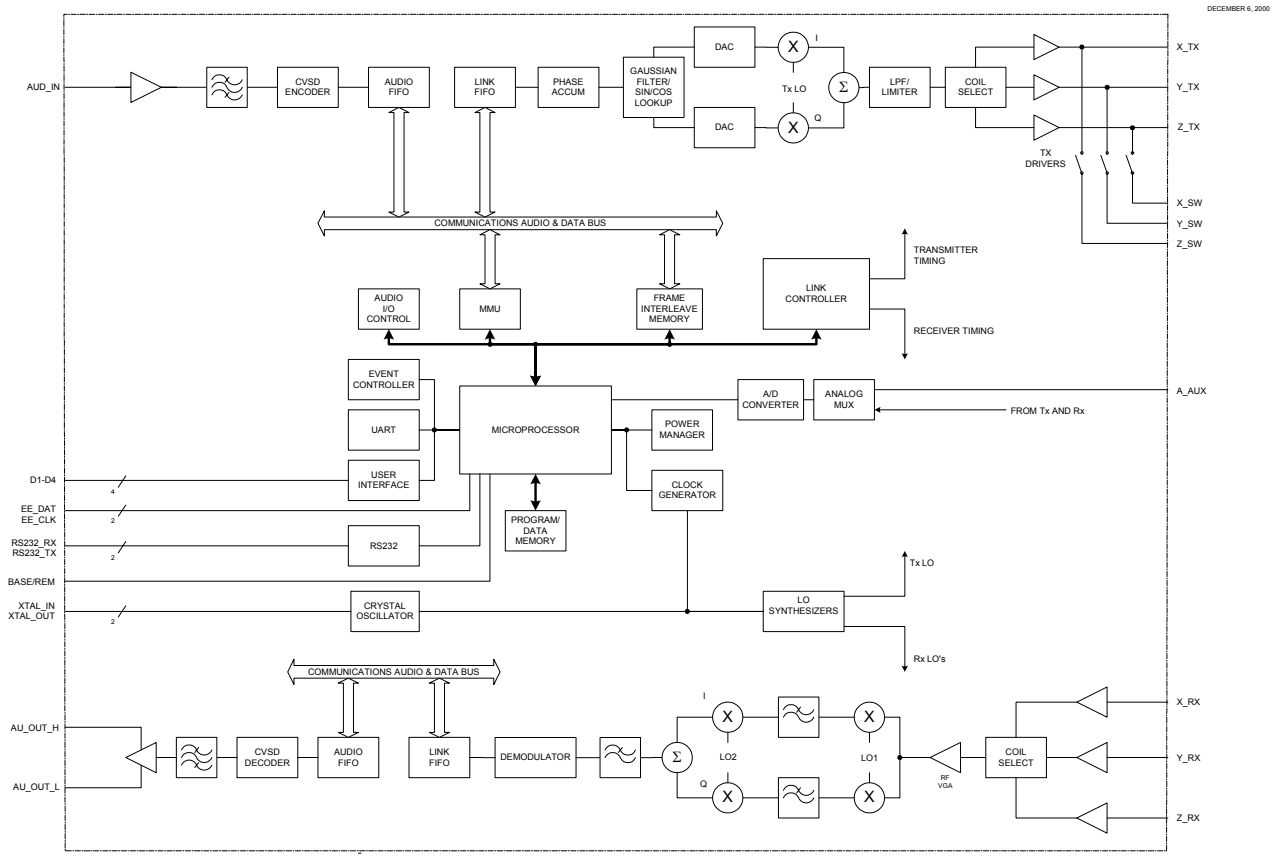

Fig. 1. The LibertyLink block-diagram

2.1. Receiver

The base antennas act as a receiving coils during the appropriate time slot and feed the signal through a tuning network and into the X_RX, Y_RX and Z_RX pins on the chip. The Q of the receiving coils in conjunction with the chain of image-reject mixers and active filters reduces adjacent channel interference. The receiver amplifies the raw signal delivered by the antenna front-end, and provides adjacent channel filtering while downconverting to IF and baseband in a two stage conversion chain. The resulting baseband FM signal is demodulated to provide the audio data stream to the decoder.

The receiver consists of a Low Noise Amplifier (LNA), an RF Variable Gain Amplifier (RF VGA), two mixing stages, two filter stages, and a demodulator/detector stage. A block-diagram of the receiver is shown below in Fig. 2., followed by the receiver specification table and the sample of the frequency plan for Channel 1 (Fig.3.).

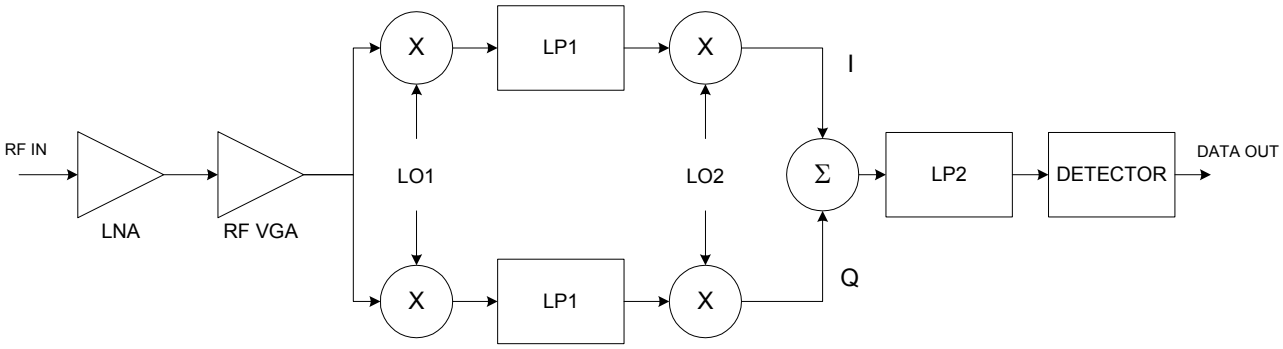

Fig. 2. LibertyLink Receiver Block Diagram

Receiver Specifications

Receiver		Min.	Nominal	Max.	Units
Carrier Frequencies			Ch1: 13.56, Ch2: 13..96		MHz
Modulation	GMSK				
Channel Spacing			400		KHz
Channel Bandwidth			215		KHz
Dynamic Range			80		dB
Baseband Data Rate			204.8		kbps
Total Operating Current			1000		uA
Antenna Interface					
Input Referred Noise			5.5		nV/root-Hz
IF					
IF Frequency			IF_{Ch1}: 508.47 IF_{ch2} : 491.52		KHz
IF Filter Type	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			500		KHz
IF Coupling Filter Type	Passive HPF				
Order			2		
Frequency Cutoff (3dB)			50		KHz
Baseband					
Baseband Bandwidth			300		KHz
Baseband Channel Filter	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			300		KHz
Baseband Coupling Filter Type	Passive HPF				
Order			1		
Frequency Cutoff (3dB)			25		KHz

The sample how receiver operates according to the following frequency plan when the input signal appears at 13.56 MHz.

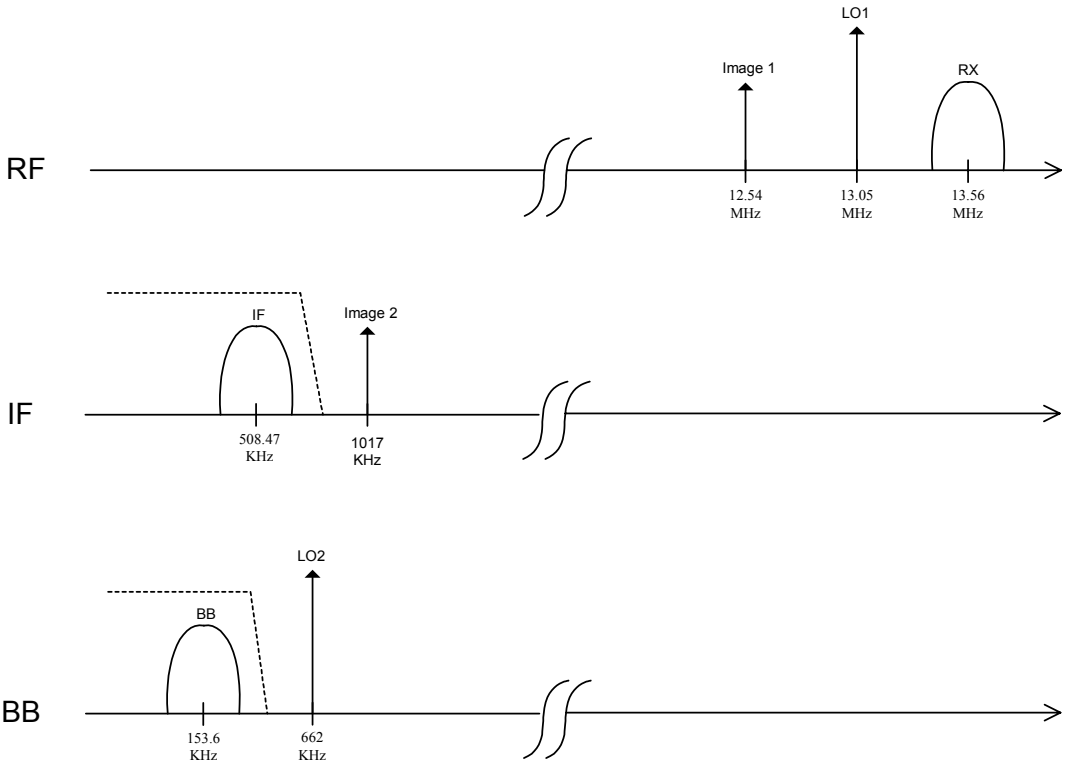

Fig. 3. LibertyLink Receiver Frequency Plan

2.1.1 LNA/RF VGA

Two gain stages, the Low Noise Amplifier (LNA) and the RF Variable Gain Amplifier (VGA), precede the image reject mixer. Both feature variable gain capabilities in order to address the 80dB dynamic range requirement. For small signals, the LNA provides 14dB of gain at 13.56 MHz. Due to the high signal levels experienced when system separation is small, the LNA incorporates signal attenuation circuitry. Since the maximum signal levels exceed the 1dB compression point of the LNA, attenuation is achieved by changing the input resistance of the receiver, resulting in a reduction in antenna Q. Two attenuation steps are possible, for a total of three effective LNA gain states of 14dB, 8dB, and -7dB. The RF VGA addresses further internal dynamic range issues. A maximum gain of 15dB can be reduced to -9dB in 10 steps.

2.1.2 IF strip

The IF strip consists of in-phase and quadrature (I&Q) conversion and filter chains that are summed and filtered.

As can be seen in the frequency plan (Fig. 2.), significant selectivity can be achieved through the use of a relatively low intermediate frequency and high-order low pass filters. Removal of all signal components at or below the LO1 frequency occurs after the subtraction of the second mixer quadrature products. At this point, further selectivity is achieved with additional low pass filtering at baseband (LP2).

2.1.3 Demodulator/Detector

The demodulator and detector scheme will be discussed later.

2.1.4. CVSD Decoder

Although not generally considered part of the receiver, the CVSD decoder is the final stage of the receive chain. The decoder, shown in Fig. 4, receives a 1-bit 64Kbps digital signal that indicates the direction and values for two "leaky" digital integrators. The direction and values for the integrators are determined by the incoming bit value. The detection of four (4) consecutive 1's or 0's represents a condition called "slope-over/under load". It signals to the decoder that the estimate no longer has the same slope as the incoming signal and therefore, the integrators value (step-size) needs to be changed. The Syllabic integrator changes its step size up to a maximum value based on the sampling rate and the time constant. This bit also represents as direction (+ or -), based on the bit value of 1 or 0 respectively, of the Syllabic value as it is applied to the Principle integrator. The output of the Principle integrator feeds a 13-bit Digital-to-Analog Converter and a low-pass filter with an f_C of 4 kHz. The DAC output is a reconstructed version of the original baseband audio signal.

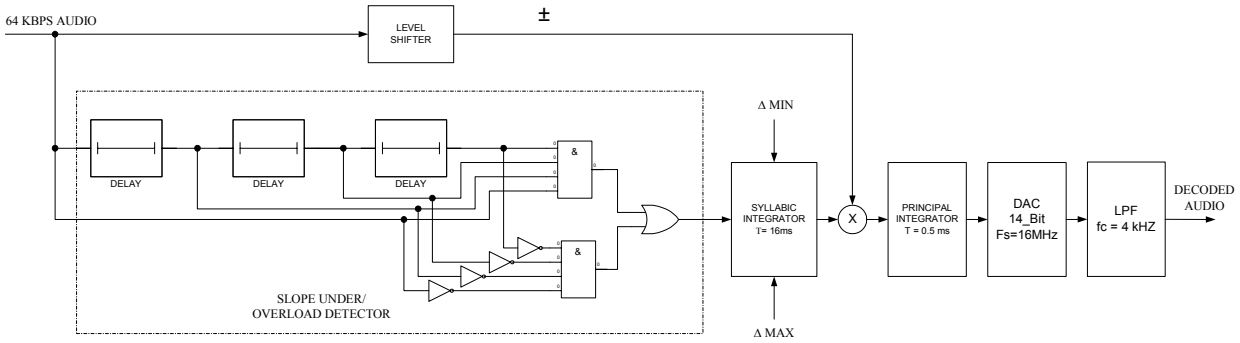

Fig. 3. CVSD Decoder.

CVSD Decoder Specifications

CVSD Decoder		Min.	Nominal	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits
Principal Integrator Time Constant					msec
Frequency Cutoff (3dB)		3.0		6.0	KHz

2.1.5. Audio Output Stage

The final stage of the receiver chain is the Audio Output stage. The audio output stage shown on Fig. 5 conditions the CVSD decoder's analog output so that it may be applied to a line level audio input. Reconstructed baseband audio from the CVSD decoder is fed into a programmable frequency response shaping block. This signal is then summed with a tone generator. These tones can be used to signal the user that a low battery condition exists or other useful information. A user or microprocessor controlled variable gain amplifier follows for volume control. A speaker driver for low impedance loads can be switched into the signal path depending on whether the chip is being used as a base or a headset.

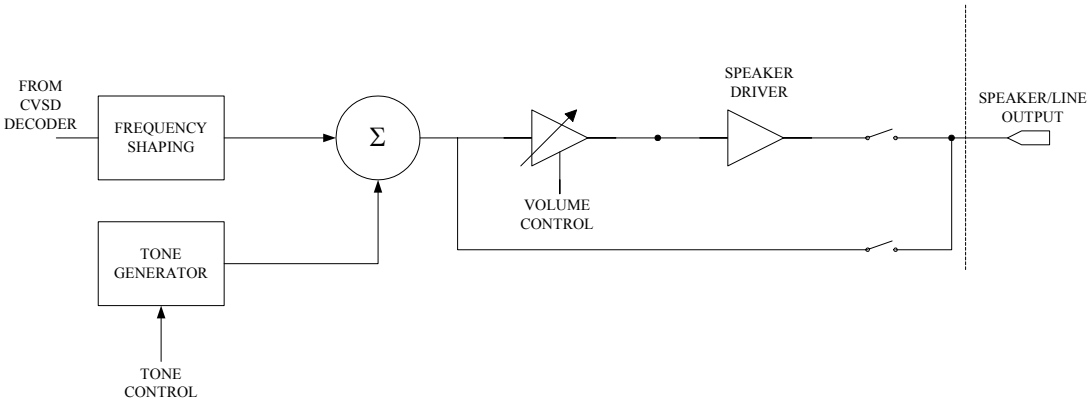

Fig. 5. Audio Output Stage Block Diagram.

2.2. Transmitter (GMSK modulator)

The transmitter system consists of the audio input stage, CVSD encoder, a data register, Gaussian Sine/Cosine lookup ROM's , I-Q 8-bit DAC's, low pass filter stages, Gilbert cell upconversion mixers, anti-alias/squaring circuitry, and the Tx driver.

Transmitter activity begins when a signal is presented at the AUD_IN pin. The signal is gained up, filtered, presented to a 13-bit ADC and input to the CVSD encoder. The driver of the system is the GMSK transmitter shown in block diagram form in Figure 5. It takes the CVSD Encoder's 64 kbps data stream as well as other data and combines them into a 204.8 kbps GMSK square wave at the carrier frequency. The input data to the GMSK transmitter is buffered and 8X oversampled. This bit stream is applied to SIN and COS Gaussian lookup tables stored in ROM. It is here that the Gaussian prefiltering with a B_t of 0.5 is performed. The lookup table values for Sine and Cos are then converted to an analog signal by the switched capacitor 8-bit DAC's. Once filtered, the Sine and Cosine signals are filtered and upconverted to become 13.56 MHz I and Q signals. The I and Q signals are then summed, filtered, and squared through a comparator. This signal is then applied to the Tx Driver and fed to the transmitter front end. Below is the block diagram, specification table and a more detailed discussion of the individual blocks.

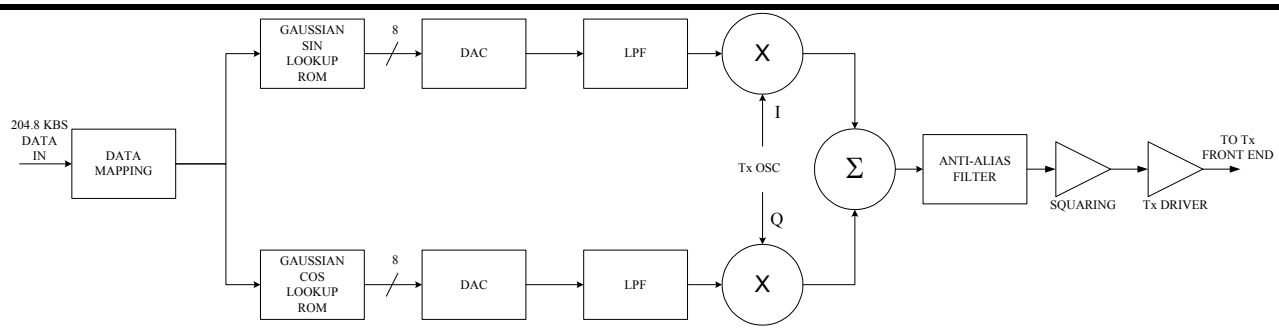

Fig. 6. GMSK Transmitter Block Diagram

Transmitter (GMSK Modulator) Specifications

Transmitter		Min.	Nominal	Max.	Units
Carrier Frequency			Ch1: 13.56 Ch2: 13.96		MHz
Modulation Type	GMSK				
Gaussian Filter Constant (BT)			0.5		
Channel Bandwidth			215		kbps
Input Data Rate			204.8		kbps
Encoding	Differential				
Data Oversampling Factor			8		samples / bit
Clock Frequency			1.6384		MHz
Baseband I-Q Filter Type	Butterworth LPF				
Order			4		
Frequency Cutoff (3dB)		165	175	185	KHz

2.2.1 Audio Input Stage

The audio input stage shown in Fig. 7 allows audio line level signal to be used as a source for the wireless system. A preamplifier for use with low-level microphones can be switched in and out of the signal path. The level and frequency response of the audio input can be adjusted under the control of the microprocessor to suit specific applications and operating conditions.

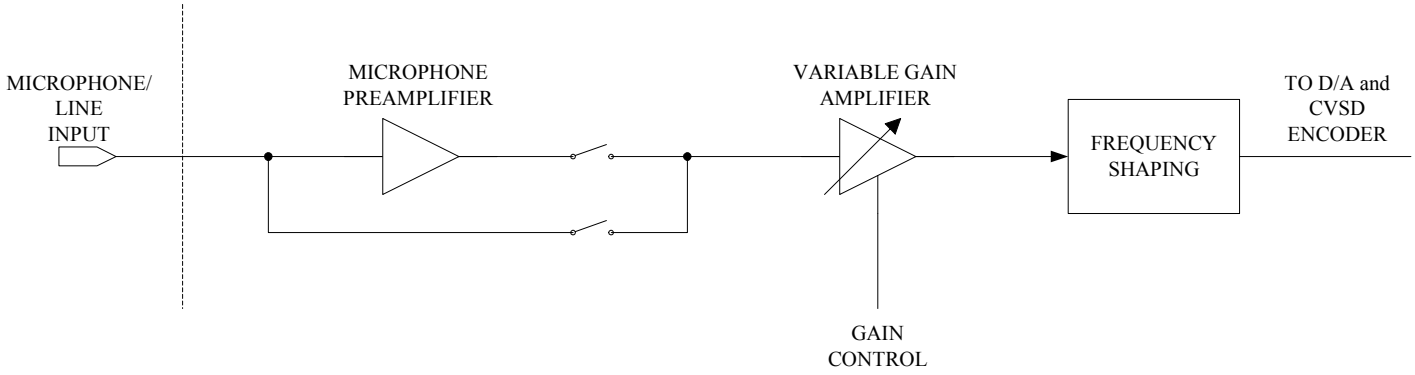

Fig. 7. Audio Input Stage Block Diagram.

Audio input specifications

Microphone/Line Input		Min.	Nominal	Max.	Units
Microphone Preamplifier Gain			24		dB
Variable Gain Amplifier Gain Range		-10		+20	dB
High Frequency Cutoff (3dB)			4		KHz
Low Frequency Cutoff (3dB)			200		Hz

2.1.2. CVSD Encoder

To encode the baseband audio signal, the signal from the audio input is fed to a continuously variable slope delta modulator (CVSD), as shown in Fig. 8. This type of digital encoder is used so that an optimal quantization resolution is achieved for a given amplitude of the signal to be encoded. By doing this, quantization noise at low signal levels can be reduced while keeping the data rate low even when large amplitude signals are encoded.

In the encoder, the audio signal is bandwidth limited by a low pass filter with an f_C of 4kHz. This signal is then compared to an estimated signal generated by the same type of CVSD decoder that is used at the receiving end of the wireless link. Thus the audio information is represented by a serial bitstream that represents the error between the actual audio signal and its estimated digital representation.

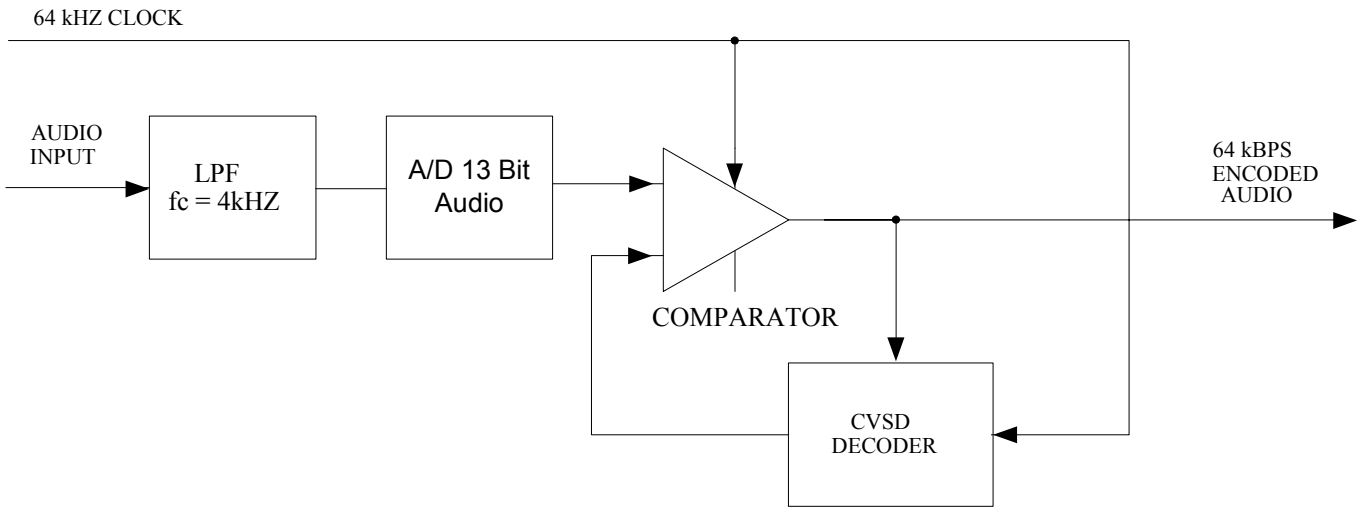

Fig. 8. CVSD Encoder.

CVSD Encoder Specifications

CVSD Decoder		Min.	Nominal	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits

Principal Integrator Time Constant					msec
Frequency Cutoff (3dB)		3.0		6.0	KHz

2.2.3. Data Mapping

This block maps the 64kbps encoded audio data along with other digital data into the I-Q plane based on three samples worth of input data. Mapping into the I-Q plane creates an address for the ROM lookup table. The two most significant bits (MSB) indicate which quadrant of the IQ plane the data is coded in. The three middle bits indicate last, current, and next data samples. The three LSB's describe the phase angle within each quadrant. Thus each LSB represents 11.25 degrees. This information is used in the ROM table to define the trajectory between constellation points.

2.2.4. Gaussian SIN/COS Lookup ROM

The function of this block is to filter the oversampled digital data using a Gaussian (B_T=0.5) response. Gaussian filtering allows spectrally efficient transitions between IQ constellation points as the data are transmitted.

The output of each table is an 8-bit word. The MSB represents the sign of the signal and the lower seven bits represent the magnitude.

2.2.5. DAC/LPF

Once the data has been Gaussian filtered and Sine/Cosine looked-up, the two 8-bit outputs are converted back into an analog signal. The DAC performs this function using the 3 MSB for the resistor ladder and the lower 5 bits in a switched capacitor array configuration. A low pass filter smoothes and bandwidth limits the DAC output before transmission. This filter is a 4-pole passive network with a 3dB bandwidth of 175kHz.

2.2.6. Upconversion

Once the baseband data has been modulated, it is mixed with the I-Q carrier clocks. In the LibertyLink, 2 programmable carrier frequencies are 13.56 MHz and 13.96 MHz.

The in-phase (I) signal chain is mixed with the Tx-I oscillator. The Tx-I oscillator is a square wave of the appropriate carrier frequency. Similarly, the quadrature (Q) signal path is mixed with the 90 degree shifted Tx-Q oscillator. The outputs of the I and Q mixers are then summed. The result is a GMSK signal centered at the Tx oscillator carrier frequency.

The mixers themselves are of the linearized Gilbert cell configuration and the output current of the I and Q mixers are summed on a resistor.

2.2.7. Smoothing Filter

The smoothing filter is a pseudo 2-pole, low pass, passive filter with a 15MHz cutoff. It serves to remove unwanted frequency components from the upconverted signal.

2.2.8. Squaring

The squaring circuit is a high-bandwidth comparator which converts the GMSK modulated sine wave output of the smoothing filter into a 50% duty cycle, GMSK modulated square wave.

2.2.9. TX Driver

The TX driver is a low output impedance buffer used to amplify the power of the transmitted signal before it is applied to the transmitter front end. The driver is also part of the resonant transmitter coil circuit. During receiver operation the output of the driver is switched into a high output impedance state. Power control to the front end is achieved by switching parallel drivers of different channel resistances in and out of the circuit.

2.3. Synthesizer/Timing

The Synthesizer/Timing subsystem generates frequencies that represent 4X the in-phase and quadrature TX-LO, RX-LO1, and RX-LO2. These signals are divided down locally in the transmit and receive sections for the I & Q clocks. Fig. 9. shows a block-diagram of the basic synthesizer. Individual synthesizers are required for each local oscillator.

The synthesizer uses the classical phase locked loop (PLL) topology. A 4 MHz crystal oscillator is the stable frequency reference for each loop. A frequency divider of value N divides the clock and is fed into one input of a digital phase detector. The output of the phase detector is a charge pump and represents the frequency error of the loop. So that the loop is stable under all operating conditions, a simple on-chip capacitor filter network with a stability compensation resistor is used to condition the error charge before it is applied to the VCO. Note that the Tx and LO1 loops have a different VCO scale factor than the lower frequency LO2 loop. The digital output of the VCO is then divided down in frequency by a factor M and fed into the other input of the phase detector. Since a PLL is a closed loop system, the output frequency of the VCO is the frequency of the crystal reference multiplied by M/N.

A wide range of Tx and LO frequencies are programmable using the 12-bit resolution of the frequency scaling factors M and N. The output of the VCO is actually a factor of four higher than the desired frequency. This allows the I/Q logic section to create 50% duty I and Q signal at the appropriate frequency.

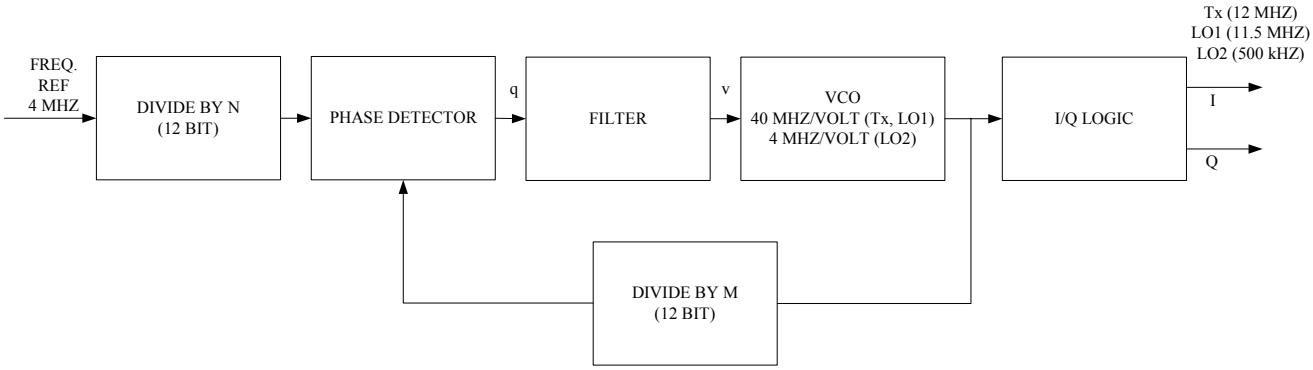

Fig. 9. Synthesizer Block Diagram.

The synthesizer/timing block, based on a low cost crystal, provides local oscillator and reference clocks for the RF and baseband sections.

The microprocessor/control section and specialized functional blocks control almost every aspect of the system's operation. It is composed of a microprocessor core, MMU controller, DMA unit, link controller, a UART, an audio randomizer and derandomizer, watchdog timer, a timer/counter, a power manager, a user interface controller, and a system control block.

3. Off-chip functions

There are several off-chip functions that were added to create an operating system. These functions, when taken with the LibertyLink chip, represent an entire working headset wireless system product. These sections, each discussed below,

include the antenna front-end, audio input stage, crystal reference, audio output stage, EEPROM, regulator and battery charging circuit.

3.1 Off-chip functions: front-end

The front-end is made up of two primary blocks, the tuning circuit and the coil antennas. In order for the system to function properly, the base unit needs to employ 'antenna diversity'. This ensures that the base will receive the optimal signal regardless of the orientation of the headset. To do this, three ferrite coils are mounted orthogonally and designated the X, Y and Z channel. On the base unit we use these coils to drive the X_RX/X_TX, Y_RX/Y_TX, and Z_RX/Z_TX. The signals present on these three coils are constantly monitored and the optimal coil is selected for use. The circuit networks for each X, Y and Z channels are the same and are identical to the circuit configuration used in the headset. Each of the three TX circuits needs to be tuned in manufacturing to the correct impedance.

It is important that extra care is taken when mounting the three antennas. In addition to being mounted at 90˚ to each other, ideally the antennas should be on a single centerline and the minimum spacing (12mm center to center for the 4 x 10mm antennas) must be observed

The transmit portion of the front-end converts the frequency modulated square wave output into a sine wave current in the antenna coil . This current through the antenna creates a modulated magnetic signal at the air interface. For receiver operation, the front-end must also convert the incident magnetic field from the base unit into a signal that can be amplified and demodulated.

The tuning circuit ensures that the proper impedance is present at the frequency of use. This is necessary due to variations in the coil impedance. Variable capacitors are used on the front-end to adjust the impedance. This is achieved by monitoring the transmit signal, using one of several methods, and adjusting the capacitor. Tuning of the receiver is accomplished automatically using a firmware driven capacitor table containing 7 programmable capacitors with 24 pF of range. This capacitor table loads into memory when the base is turned on.

Since LibertyLink is a TDD system, the front end must be configured to alternately transmit and receive in synch with the headset unit. During a transmit frame, the t/r switch is open and the transmitter driver applies a 50% duty GMSK modulated square wave to the transmitter tuning network. This front-end network, the antenna coils, and some impedance scaling capacitors form a series tuned band pass filter that is centered at the first channel frequency 13.56 MHz. It should be noted, that when second channel frequency 13.956 MHz in use, the transmitter front-end network is still tuned to 13.56 MHz resonance frequency but receiver front-end is tuned to 13.956 MHz only. The result is a GMSK modulated sine wave coil current.

During receive mode, the low impedance of the transmitter driver must be removed from the circuit. This is accomplished by setting the drivers to a high output impedance state. The t/r switch is closed and the receiver tuning network switches in the on-chip capacitor that gives the largest receiver signal. In this mode, the series tuned band pass response of the transmitter path has been converted into a purely parallel band pass response.

3.2. Off-chip functions: host device interface

The 2.5mm configured base/phone interface circuit contains lines for ground, audio input and audio output. Below is a table detailing the pin interface to the phone. Details of the pin configuration is shown in the table below.

Pin	Input/Output	Voltage
Universal 2.5mm jack Product		
AUD_IN	In to LibertyLink	500mVpp
AUD_OUT_L	Out to Phone	1.7Vpp
GND	Common ground	Ground

3.3. Off-chip functions: crystal reference

The 9.8304 MHz crystal oscillator is the stable frequency reference for the system. An on-chip, low gain inverter is used as the oscillator amplifier. A high gain buffer squares the oscillator output and distributes it throughout the chip.

3.4. Off-chip functions: EEPROM
The LibertyLink chip contains only a boot ROM and relies on an off-chip 16 kbit EEPROM for operating instructions. At power up, program code and data is automatically uploaded into LibertyLink's 5k pagable RAM. This firmware can be burned into the EEPROM using a EEPROM writer. It is also possible to reprogram the EEPROM after installation by using RS-232 port and appropriate fixture .

3.5. Off-chip function: boost converter

The boost DC-DC converter converts the 1.5 V from an AA disposable battery to 3.3 V dc. The converter is based on fixed frequency, current mode, pulse-width-modulation controller. It uses built-in synchronous rectifier therefore no external Schottky diode is required. A low EMI mode is implemented to reduce interference and radiated electromagnetic energy when converter enters the discontinue conduction mode.
3.6 Off-chip functions: regulator circuit

The regulator circuit is a simple linear regulator. As the voltage from boost converter drops from 3.3V down to 2.1V, the regulator puts out a constant 2.0 V.

3.7 Off-chip functions: headset battery charging circuit

The base charges the headset's batteries when it is docked to the base unit. The charging time is around 5 hours.
The batt_chg line can be programmed through firmware to accommodate a variety of charging schemes.

4. System modes operation

Both the base and headset unit can be in the normal operating states and docked states. Each of these states has several sub-modes of operation.

4.1.1. Normal operation, undocked system states (Fig. 10)

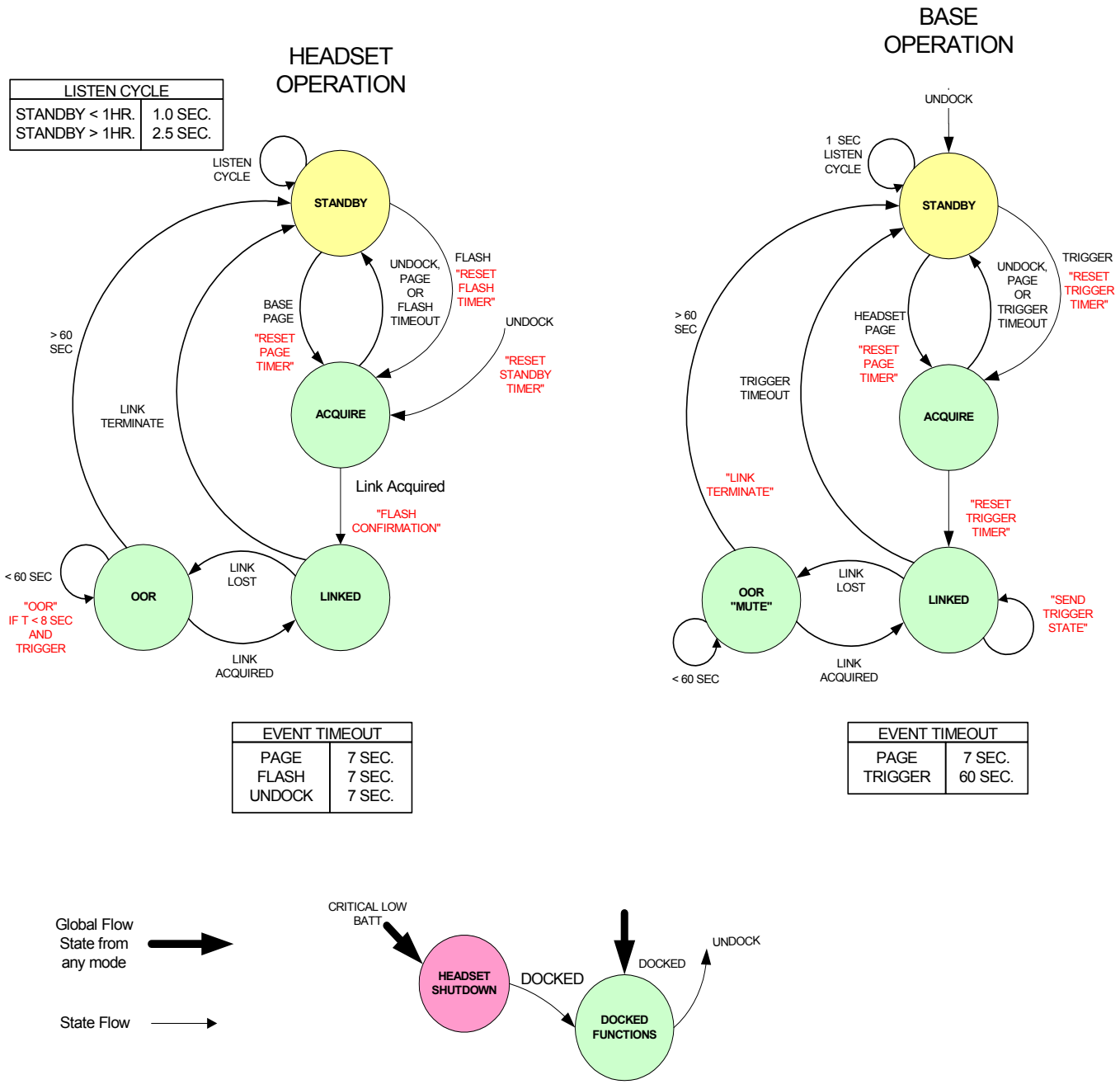

Fig.10. UNDOCKED OPERATIONAL STATE DIAGRAM

4.1.2. Standby

A power management mode of the Headset and Base where the units are listening for the presence of each other when undocked. When one of the pair detects a Page from the other, the pair will transition into the Acquire mode to establish

communication. The interval at which the units listen is dependent on the amount of time that the link has been inactive or if the headset has just been undocked.

4.1.3. Linked

The mode of the pair while in typical use. In this mode bi-directional audio communication occurs. The pair leaves this mode if it goes Out of Range for a preset time period, enters a critical shutdown, is docked, or if the link is terminated by a base timeout

4.2. Docked states (Fig. 11)

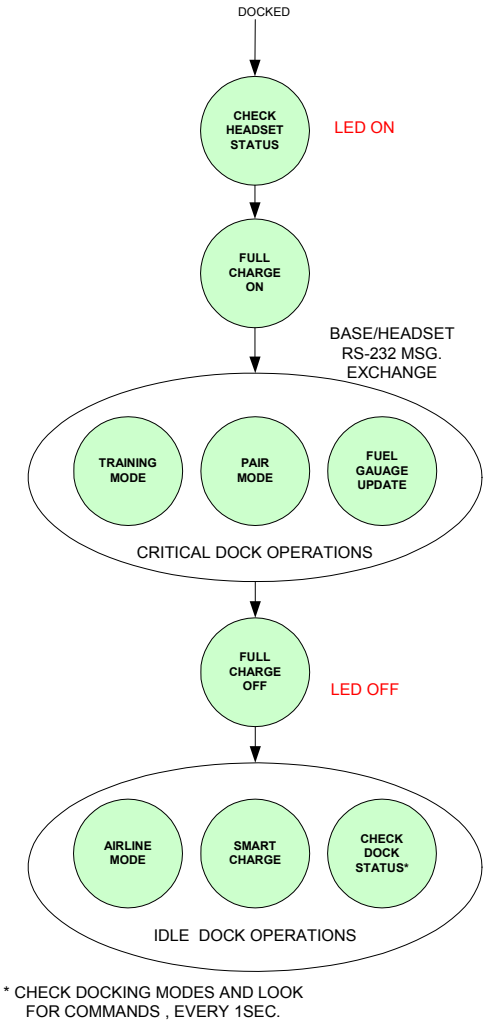

Fig. 11. DOCKED OPERATIONAL STATE DIAGRAM

4.2.1. Airline

This mode puts the Unleash headset and base into an inactive mode. Neither device will transmit or receive thus preventing the units from waking up out of standby mode. This mode will consume very little power. The pair must be docked in order to enter this mode. To exit, simply undock.

4.2.2. Smart charge

The mode in which the Base controls the charging process of the Headset battery using smart charge. Normal user operations are not possible in this mode however the charging mode is programmed to pause for housekeeping routines such as pairing.

5. The wireless headset system operation on the system level

Below is a discussion of the headset at the system level, including how the headset interacts with the base unit and how the base unit interfaces to the phone.

With the phone turned on and both the base and headset in standby mode, a call can be initiated. For outgoing calls, the user will begin by pressing the Flash button on the headset. The headset responds to the flash by calling for a link initiation with the base. Once a link is established, which takes less than a second in normal operating conditions, the system is ready to use. The user can either use the phone's voice recognition function, which requires the keying of one buttons then speaking into the headset, or he can dial the number manually. If the user dials manually, the Flash button is not necessary. Just dial and press 'send' or 'yes' as normal.
For incoming calls the phone responds by signaling the hands-free device that there is a call in progress. This is typically done by bringing the audio input line high, or turning on the Mic_bias pin of the phone. The phone manufacturers enable at least one pin to signal a call and the reference design is configured the to accept this signal on a_aux_3. This signal tells the base to wake from stand-by and begin link initiation with the headset. If the headset is not present (if it is more than 1.25 meters away), the base will continue polling for seven seconds. After seven seconds with no contact, the base will revert back to standby and the user must use the handset. If the headset is present the user will hit the Flash button. Flash will signal the base to answer the call if flash capabilities enable on the phone. If the headset is present and links with the base, but the user does not hit the Flash button, the call will continue to ring unanswered. The phone can be answered in the normal way.

Regardless of how the call is initiated, when the call is complete, the user hits the flash to hang-up. This will signal the base to turn one of the user definable lines (d0) on and pull down the phone_aud_in line. This line is used to signal the phone to switch hook. If the headset goes out of range during a call, the phone reverts to handset mode but does not hang up. The phone can be hung-up in the normal way.

6. Technical Characteristics of the Base

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	Characteristics	Description
	Size	64.3 mm x 46.3 mm x 21.0 mm
	Weight	28 gm
	Talk time	3hr. (180 min)
	Standby time	30 days
	Standby to operate interval	2 sec
	Recharge time	Not applicable
	Product life	2 yr
	Operating environment	0 to 120F
	Operator controls	Flash & Volume
	Status indicator	Red/green LED
	Range to base	4 - 6 ft
	Audio quality	64 kbps CVSD
	Storage environment	-40 to 180 F

Wireless Headset System
Headset Unit, Model: RDA444-UNLEASH
Technical Description

reason
PRODUCTS

Wireless Headset System
Headset Unit Model: RDA444-UNLEASH

The Unleash wireless headset system is a fully integrated Time Division Duplexed (TDD) digital communication system designed for use as wireless short-range audio link for mobile phones or similar devices. The system transmits a Gaussian Minimum Shift Keyed (GMSK) magnetic field between the base station and headset station. The headset uses a single magnetic coil for both transmit and receive. Spatial diversity is achieved through three orthogonal magnetic coils in the base, allowing the system to select the antenna axis that results in the optimum signal to noise ratio (lowest Bit Error Rate (BER)) for the link. Near-field magnetic transmission allows a lower cost system that makes more efficient use of power and space compared to conventional RF approaches.

The is able to operate on the two channels and utilize the "listen-before-talk" to automatically switch to the one of them with less interference.

The system is based on the LibertyLink single chip full duplex wireless transceiver consisting of a receiver, transmitter, codec, frequency synthesizer, microprocessor and memory. This same chip is used for the base and headset implementations with only minor circuit and firmware changes. The LibertyLink is fully integrated and only a handful of low-cost and readily available external components are needed to make a complete system. The versatile microprocessor firmware can be programmed to suit many specialized applications.

1. Headset unit

The wireless headset is used to transmit and receive voice over a wireless link for connection to a mobile phone or similar voice devices. The headset uses a single 4mm x 45mm coil on the headset, yielding 4 - 6 ft range. In this configuration, high quality voice is CVSD encoded and transmitted at 64kbps.

The PC board for the headset application is approximately 40mm x 14 mm. In addition to the PCB a headset requires a ferrite coil, two Ni-MH batteries, a speaker and microphone. A "Flash" switch is used to signal the phone to answer the call and for hook switch (if the phone supports these options). The Unleash headset is an 'earbud' style (fits in the ear).

2. LibertyLink ASIC Tranceiver

The LibertyLink chip supports full duplex transmission of audio and data. For discussion purposes, the system is broken down into five sections; the receiver, the transmitter, synthesizer timing block, microcontroller and the off-chip front-end. The LibertyLink block-diagram is shown on the Fig.1

The receiver chain is made up of an off-chip antenna block, a low noise amplifier, the IF strip, down converters, the detector, the CVSD decoder and audio output stage. Each of these are discussed in detail in the next section.

The transmitter chain consists of the following blocks; audio input stage, CVSD encoder, GMSK modulator, coil driver, and off-chip antenna block. Each functional block is described in more detail below.

The transmitter chain converts microphone signal into a GMSK modulated signal that is applied to the transmit/receive coil. The digitally encoded audio signal is not transmitted continuously over time, rather, each end of the system alternates between transmit and receive in 1.4 millisecond bursts or frames. This allows a single antenna for both transmit and receive modes and eliminates the possibility of the transmitter crosstalk into the receiver.

The synthesizer/timing block, based on a low cost crystal, provides local oscillator and reference clocks for the RF and baseband sections.

The microprocessor/control section and specialized functional blocks control almost every aspect of the system's operation. It is composed of a microprocessor core, MMU controller, DMA unit, link controller, a UART, an audio randomizer and derandomizer, watchdog timer, a timer/counter, a power manager, a user interface controller, and a system control block.

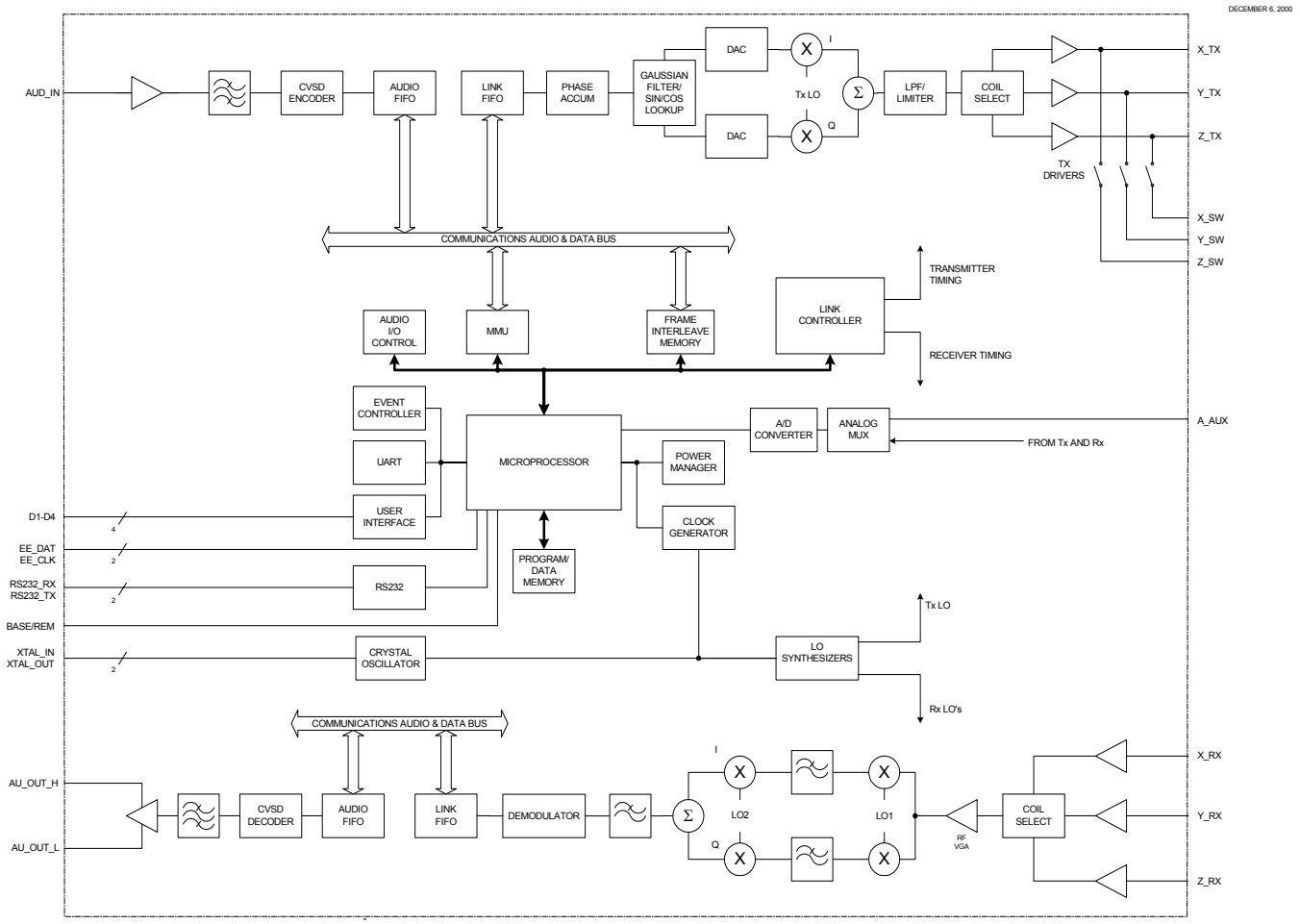


Fig. 1. The LibertyLink block-diagram

2.1. Receiver

The headset antenna act as a receiving coil during the appropriate time slot and feed the signal through a tuning network and into the X_RX pin on the chip. The Q of the receiving coil in conjunction with the chain of image-reject mixers and active filters reduces adjacent channel interference. The receiver amplifies the raw signal delivered by the antenna front-end, and provides adjacent channel filtering while downconverting to IF and baseband in a two stage conversion chain. The resulting baseband FM signal is demodulated to provide the audio data stream to the decoder.

The receiver consists of a Low Noise Amplifier (LNA), an RF Variable Gain Amplifier (RF VGA), two mixing stages, two filter stages, and a demodulator/detector stage. A block-diagram of the receiver is shown below in Fig. 2., followed by the receiver specification table and the sample of the frequency plan for Channel 1 (Fig.3.).

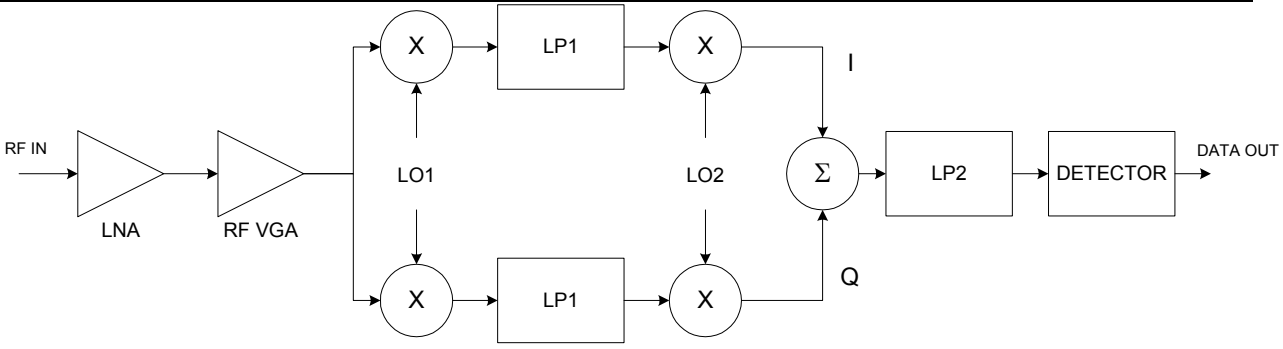


Fig. 2. LibertyLink Receiver Block Diagram

Receiver Specifications

Receiver		Min.	Nominal	Max.	Units
Carrier Frequencies			Ch1: 13.56, Ch2: 13.96		MHz
Modulation	GMSK				
Channel Spacing			400		KHz
Channel Bandwidth			215		KHz
Dynamic Range			80		dB
Baseband Data Rate			204.8		kbps
Total Operating Current			1000		uA
Antenna Interface					
Input Referred Noise			5.5		nV/root-Hz
IF					
IF Frequency			IF_{Ch1}: 508.47 IF_{ch2} : 491.52		KHz
IF Filter Type	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			500		KHz
IF Coupling Filter Type	Passive HPF				
Order			2		
Frequency Cutoff (3dB)			50		KHz
Baseband					
Baseband Bandwidth			300		KHz
Baseband Channel Filter	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			300		KHz
Baseband Coupling Filter Type	Passive HPF				
Order			1		
Frequency Cutoff (3dB)			25		KHz

The sample how receiver operates according to the following frequency plan when the input signal appears at 13.56 MHz.

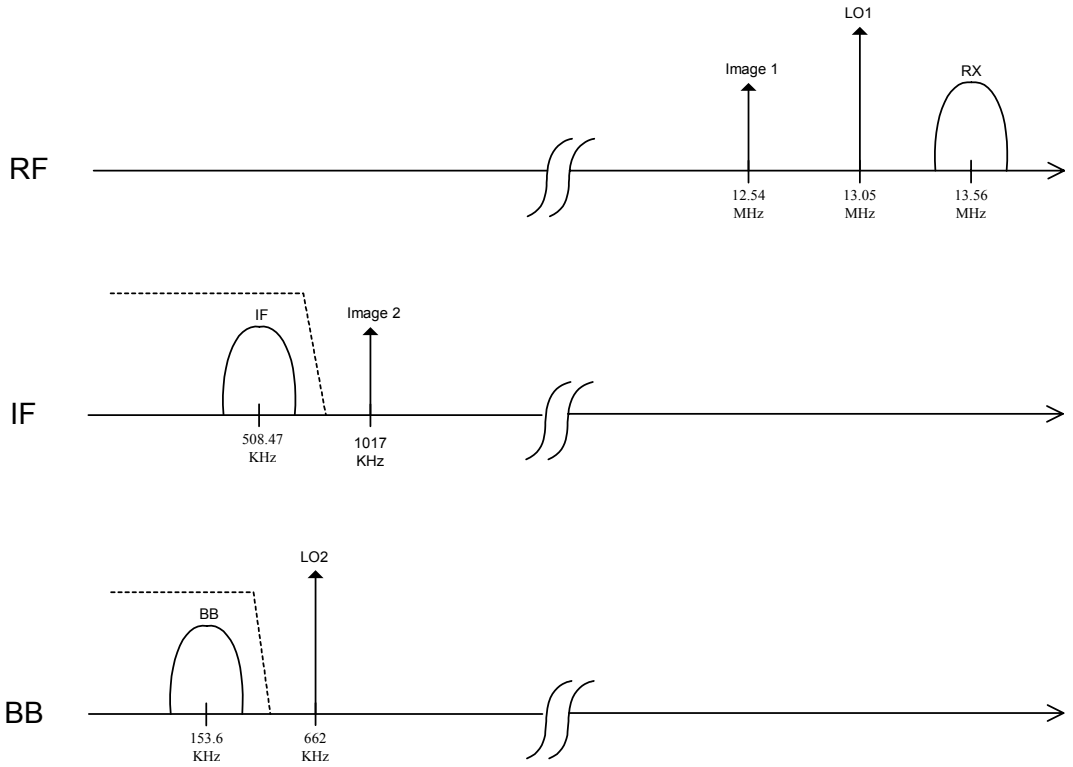


Fig. 3. LibertyLink Receiver Frequency Plan

2.1.1 LNA/RF VGA

Two gain stages, the Low Noise Amplifier (LNA) and the RF Variable Gain Amplifier (VGA), precede the image reject mixer. Both feature variable gain capabilities in order to address the 80dB dynamic range requirement. For small signals, the LNA provides 14dB of gain at 13.56 MHz. Due to the high signal levels experienced when system separation is small, the LNA incorporates signal attenuation circuitry. Since the maximum signal levels exceed the 1dB compression point of the LNA, attenuation is achieved by changing the input resistance of the receiver, resulting in a reduction in antenna Q. Two attenuation steps are possible, for three effective LNA gain states of 14dB, 8dB, and -7dB. The RF VGA addresses further internal dynamic range issues. A maximum gain of 15dB can be reduced to -9dB in 10 steps.

2.1.2 IF strip

The IF strip consists of in-phase and quadrature (I&Q) conversion and filter chains that are summed and filtered.

As can be seen in the frequency plan (Fig. 2.), significant selectivity can be achieved with a relatively low intermediate frequency and high-order low pass filters. Removal of all signal components at or below the LO1 frequency occurs after the subtraction of the second mixer quadrature products. At this point, further selectivity is achieved with additional low pass filtering at baseband (LP2).

2.1.3. CVSD Decoder

Although not generally considered part of the receiver, the CVSD decoder is the final stage of the receive chain. The decoder, shown in Fig. 4, receives a 1-bit 64Kbps digital signal that indicates the direction and values for two "leaky" digital integrators. The direction and values for the integrators are determined by the incoming bit value. The detection of four (4) consecutive 1's or 0's represents a condition called "slope-over/under load". It signals to the decoder that the estimate no longer has the same slope as the incoming signal and therefore, the integrators value (step-size) needs to be changed. The Syllabic integrator changes its step size up to a maximum value based on the sampling rate and the time constant. This bit also represents as direction (+ or -), based on the bit value of 1 or 0 respectively, of the Syllabic value as it is applied to the Principle integrator. The output of the Principle integrator feeds a 13-bit Digital-to-Analog Converter and a low-pass filter with an f_C of 4 kHz. The DAC output is a reconstructed version of the original baseband audio signal.

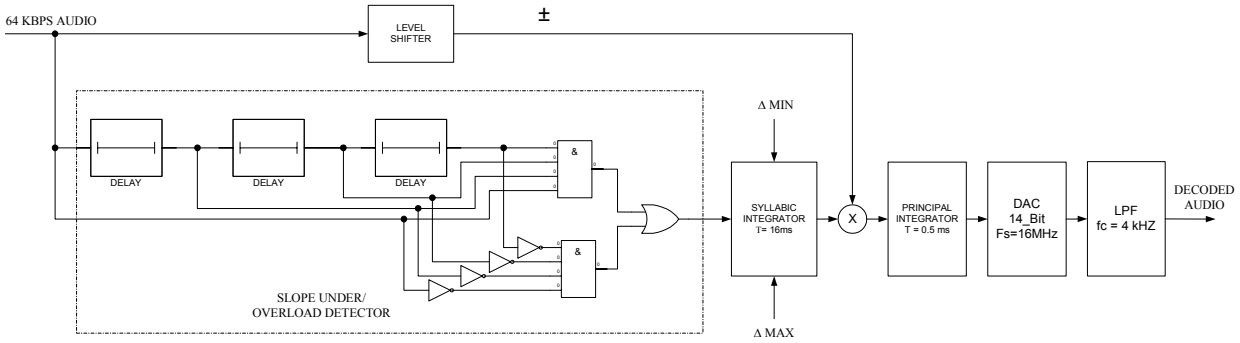


Fig. 3. CVSD Decoder.

CVSD Decoder Specifications

CVSD Decoder		Min.	Nominal	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits
Principal Integrator Time Constant					msec
Frequency Cutoff (3dB)		3.0		6.0	KHz

2.1.4. Audio Output Stage

The final stage of the receiver chain is the Audio Output stage. The audio output stage shown on Fig. 5 conditions the CVSD decoder's analog output so that it applied to a 32 ohm speaker. Reconstructed baseband audio from the CVSD decoder is fed into a programmable frequency response shaping block. This signal is then summed with a tone generator. These tones can be used to signal the user that a low battery condition exists or other useful information. A user or microprocessor controlled variable gain amplifier follows for volume control. A speaker driver for low impedance loads can be switched into the signal path depending on whether the chip is being used as a base or a headset.

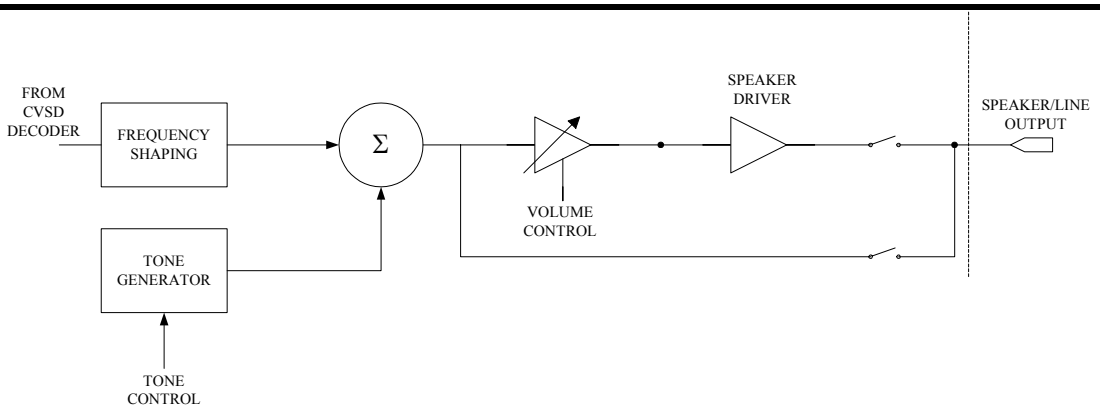


Fig. 5. Audio Output Stage Block Diagram.

2.2. Transmitter (GMSK modulator)

The transmitter system consists of the audio input stage, CVSD encoder, a data register, Gaussian Sine/Cosine lookup ROM's , I-Q 8-bit DAC's, low pass filter stages, Gilbert cell up conversion mixers, anti-alias/squaring circuitry, and the Tx driver.

Transmitter activity begins when a signal is presented at the AUD_IN pin. The signal is gained up, filtered, presented to a 13-bit ADC and input to the CVSD encoder. The driver of the system is the GMSK transmitter shown in block diagram form in Figure 5. It takes the CVSD Encoder's 64 kbps data stream as well as other data and combines them into a 204.8 kbps GMSK square wave at the carrier frequency. The input data to the GMSK transmitter is buffered and 8X oversampled. This bit stream is applied to SIN and COS Gaussian lookup tables stored in ROM. It is here that the Gaussian prefiltering with a B_t of 0.5 is performed. The lookup table values for Sine and Cos are then converted to an analog signal by the switched capacitor 8-bit DAC's. Once filtered, the Sine and Cosine signals are filtered and upconverted to become 13.56 MHz I and Q signals. The I and Q signals are then summed, filtered, and squared through a comparator. This signal is then applied to the Tx Driver and fed to the transmitter front end. Below is the block diagram, specification table and a more detailed discussion of the individual blocks.

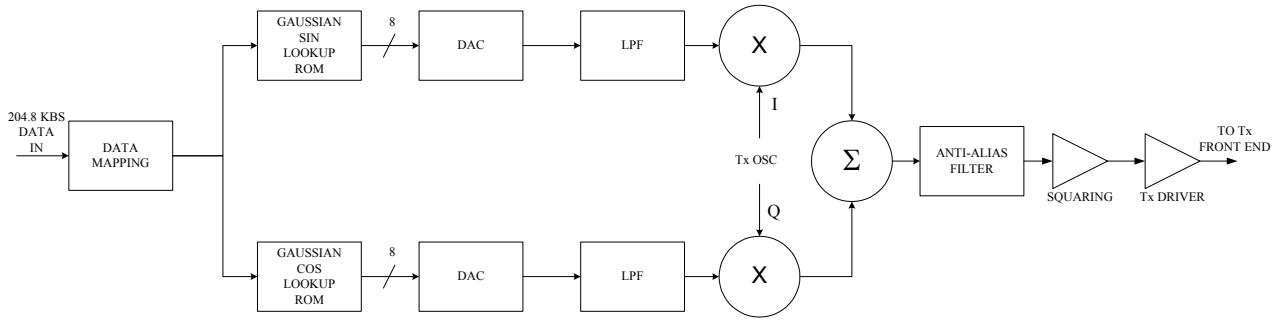


Fig. 6. GMSK Transmitter Block Diagram

Transmitter (GMSK Modulator) Specifications

Transmitter		Min.	Nominal	Max.	Units
Carrier Frequency			Ch1: 13.56 Ch2: 13.96		MHz
Modulation Type	GMSK				
Gaussian Filter Constant (BT)			0.5		

Channel Bandwidth			215		kbps
Input Data Rate			204.8		kbps
Encoding	Differential				
Data Oversampling Factor			8		samples / bit
Clock Frequency			1.6384		MHz
Baseband I-Q Filter Type	Butterworth LPF				
Order			4		
Frequency Cutoff (3dB)		165	175	185	KHz

2.2.1 Audio Input Stage

The audio input stage shown in Fig. 7 allows an electret/condenser microphone as a source for the wireless system. A preamplifier for use with low-level microphones can be switched in and out of the signal path. The level and frequency response of the audio input can be adjusted under the control of the microprocessor to suit specific applications and operating conditions.

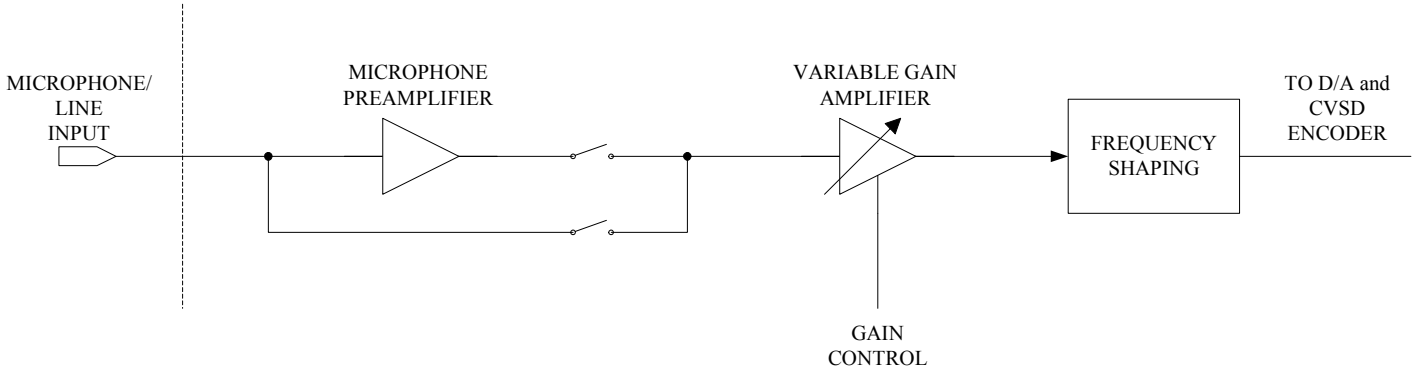


Fig. 7. Audio Input Stage Block Diagram.

Audio input specifications

Microphone/Line Input		Min.	Nominal	Max.	Units
Microphone Preamplifier Gain			24		dB
Variable Gain Amplifier Gain Range		-10		+20	dB
High Frequency Cutoff (3dB)			4		KHz
Low Frequency Cutoff (3dB)			200		Hz

2.1.2. CVSD Encoder

To encode the baseband audio signal, the signal from the audio input is fed to a continuously variable slope delta modulator (CVSD), as shown in Fig. 8. This type of digital encoder is used so that an optimal quantization resolution is achieved for a given amplitude of the signal to be encoded. By doing this, quantization noise at low signal levels can be reduced while keeping the data rate low even when large amplitude signals are encoded.

In the encoder, the audio signal is bandwidth limited by a low pass filter with an f_C of 4kHz. This signal is then compared to an estimated signal generated by the same type of CVSD decoder that is used at the receiving end of the wireless link. Thus the audio information is represented by a serial bitstream that represents the error between the actual audio signal and its estimated digital representation.

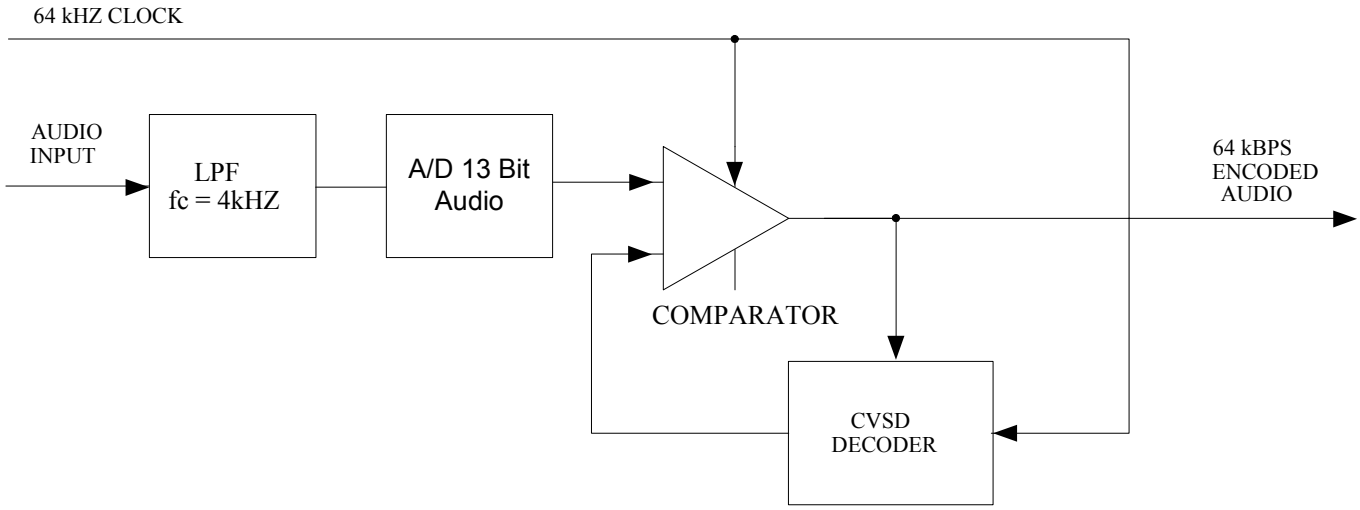


Fig. 8. CVSD Encoder.

CVSD Encoder Specifications

CVSD Decoder		Min.	Nominal	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits
Principal Integrator Time Constant					msec
Frequency Cutoff (3dB)		3.0		6.0	KHz

2.2.3. Data Mapping

This block maps the 64kbps encoded audio data along with other digital data into the I-Q plane based on three samples worth of input data. Mapping into the I-Q plane creates an address for the ROM lookup table. The two most significant bits (MSB) indicate which quadrant of the IQ plane the data is coded in. The three middle bits indicate last, current, and next data samples. The three LSB's describe the phase angle within each quadrant. Thus each LSB represents 11.25 degrees. This information is used in the ROM table to define the trajectory between constellation points.

2.2.4. Gaussian SIN/COS Lookup ROM

The function of this block is to filter the oversampled digital data using a Gaussian (B_T=0.5) response. Gaussian filtering allows spectrally efficient transitions between IQ constellation points as the data are transmitted.

The output of each table is an 8-bit word. The MSB represents the sign of the signal and the lower seven bits represent the magnitude.

2.2.5. DAC/LPF

Once the data has been Gaussian filtered and Sine/Cosine looked-up, the two 8-bit outputs are converted back into an analog signal. The DAC performs this function using the 3 MSB for the resistor ladder and the lower 5 bits in a switched capacitor array configuration. A low pass filter smoothes and bandwidth limits the DAC output before transmission. This filter is a 4-pole passive network with a 3dB bandwidth of 175kHz.

2.2.6. Upconversion

Once the baseband data has been modulated, it is mixed with the I-Q carrier clocks. In the LibertyLink, 2 programmable carrier frequencies are 13.56 MHz and 13.96 MHz.

The in-phase (I) signal chain is mixed with the Tx-I oscillator. The Tx-I oscillator is a square wave of the appropriate carrier frequency. Similarly, the quadrature (Q) signal path is mixed with the 90 degree shifted Tx-Q oscillator. The outputs of the I and Q mixers are then summed. The result is a GMSK signal centered at the Tx oscillator carrier frequency.

The mixers themselves are of the linearized Gilbert cell configuration and the output current of the I and Q mixers are summed on a resistor.

2.2.7. Smoothing Filter

The smoothing filter is a pseudo 2-pole, low pass, passive filter with a 15MHz cutoff. It serves to remove unwanted frequency components from the upconverted signal.

2.2.8. Squaring

The squaring circuit is a high-bandwidth comparator which converts the GMSK modulated sine wave output of the smoothing filter into a 50% duty cycle, GMSK modulated square wave.

2.2.9. TX Driver

The TX driver is a low output impedance buffer used to amplify the power of the transmitted signal before it is applied to the transmitter front end. The driver is also part of the resonant transmitter coil circuit. During receiver operation the output of the driver is switched into a high output impedance state. Power control to the front end is achieved by switching parallel drivers of different channel resistances in and out of the circuit.

2.3. Synthesizer/Timing

The Synthesizer/Timing subsystem generates frequencies that represent 4X the in-phase and quadrature TX-LO, RX-LO1, and RX-LO2. These signals are divided down locally in the transmit and receive sections for the I & Q clocks. Fig. 9. shows a block-diagram of the basic synthesizer. Individual synthesizers are required for each local oscillator.

The synthesizer uses the classical phase locked loop (PLL) topology. A 4 MHz crystal oscillator is the stable frequency reference for each loop. A frequency divider of value N divides the clock and is fed into one input of a digital phase detector. The output of the phase detector is a charge pump and represents the frequency error of the loop. So that the loop is stable under all operating conditions, a simple on-chip capacitor filter network with a stability compensation resistor is used to condition the error charge before it is applied to the VCO. Note that the Tx and LO1 loops have a different VCO scale factor than the lower frequency LO2 loop. The digital output of the VCO is then divided down in frequency by a factor M and fed into the other input of the phase detector. Since a PLL is a closed loop system, the output frequency of the VCO is the frequency of the crystal reference multiplied by M/N.

A wide range of Tx and LO frequencies are programmable using the 12-bit resolution of the frequency scaling factors M and N. The output of the VCO is actually a factor of four higher than the desired frequency. This allows the I/Q logic section to create 50% duty I and Q signal at the appropriate frequency.

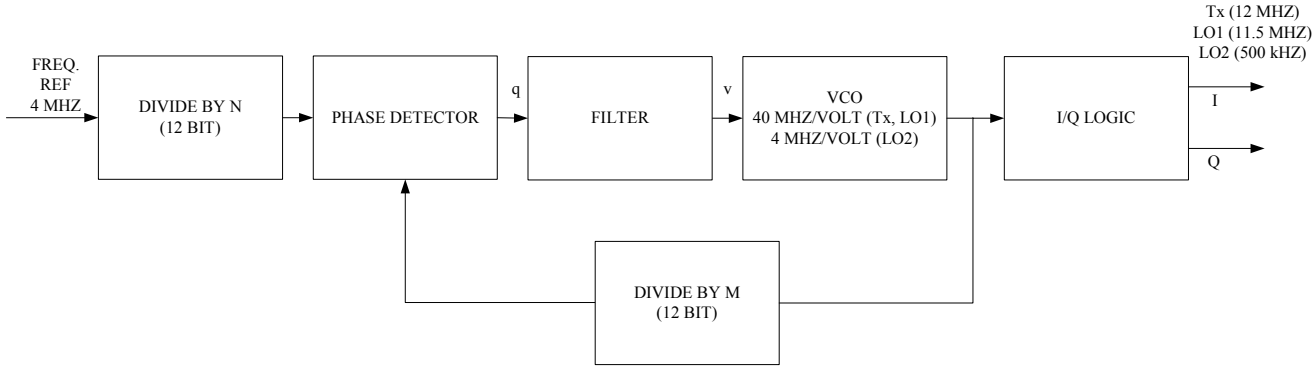


Fig. 9. Synthesizer Block Diagram.

The transmitter chain can convert microphone audio signal into a GMSK modulated signal that is applied to a transmit/receive coil. The digitally encoded audio signal is not transmitted continuously over time, rather, each end of the system alternates between transmit and receive in four millisecond bursts or frames. This allows a single antenna for both transmit and receive modes and eliminates the possibility of the transmitter crosstalk into the receiver.

The synthesizer/timing block, based on a low cost crystal, provides local oscillator and reference clocks for the RF and baseband sections.

The microprocessor/control section and specialized functional blocks control almost every aspect of the system's operation. It is composed of a microprocessor core, MMU controller, DMA unit, link controller, a UART, an audio randomizer and derandomizer, watchdog timer, a timer/counter, a power manager, a user interface controller, and a system control block.

3. Off-chip functions

There are several off-chip functions that were added to create an operating system. These functions, when taken with the LibertyLink chip, represent an entire working headset product. These sections, each discussed below, include the antenna front-end, audio input stage, crystal reference, audio output stage, EEPROM, regulator and battery charging circuit.

3.1 Off-chip functions: front-end

The transmit portion of the front-end converts the frequency modulated square wave output into a sine wave current in the antenna coil . This current through the antenna creates a modulated magnetic signal at the air interface. For receiver operation, the front-end must also convert the incident magnetic field from the base unit into a signal that can be amplified and demodulated.

The front-end is made up of two primary blocks, the tuning circuit and the coil antenna. Unlike the base unit, which uses three antennas for diversity, the headset uses only one. As a matter of convenience, Aura arbitrarily chose the x-channel to transmit and receive on, leaving the y_tx, y_rx, y_sw, z_tx, z_rx and z_sw open and unused.

The tuning circuit ensures that the proper impedance is present at the frequency of use. This is necessary due to variations in the coil impedance. A simple variable capacitor is used on the front-end to adjust the impedance. This is achieved in manufacturing by monitoring the transmit signal, using one of several methods, and adjusting the capacitor. Tuning of the receiver is accomplished automatically using a firmware driven capacitor table containing 7 programmable capacitors with 24 pF of range. This capacitor table loads into memory when the headset is turned on.

Since LibertyLink is a TDD system, the front end must be configured to alternately transmit and receive in synch with the base unit. During a transmit frame, the t/r switch is open and the transmitter driver applies a 50% duty GMSK modulated square wave to the transmitter tuning network. This front-end network, the antenna coils, and some impedance scaling capacitors form a series tuned band pass filter that is centered at the first channel frequency 13.56 MHz. It should be noted, that when second channel frequency 13.956 MHz in use, the transmitter front-end network is continue be tuned to 13.56 MHz
resonance frequency but receiver front-end is tuned to 13.956 MHz only. The result is a GMSK modulated sine wave coil current.

During receive mode, the low impedance of the transmitter driver must be removed from the circuit. This is accomplished by setting the drivers to a high output impedance state. The t/r switch is closed and the receiver tuning network switches in the on-chip capacitor that gives the largest receiver signal. In this mode, the series tuned band pass response of the transmitter path has been converted into a purely parallel band pass response.

3.2 Off-chip functions: audio input stage

The audio input stage of the headset uses an electret/condenser microphone as audio source for the wireless system. The chip to power the microphone supplies a Mic bias signal. An on-chip preamplifier for use with low-level microphones can be switched in or out of the signal path. The level and frequency response of the audio input can be adjusted under the control of the microprocessor to suit specific applications and operating conditions. As a default, it is assumes typical Mic conditioning and cellular phone frequency shaping.

3.3 Off-chip functions: audio output

The differential audio output swing of 2 Vp-p is optimized for a 32 ohm speaker. This speaker was chosen for the very small form factor, which allows it to fit in the ear. In addition, price, performance and power requirements were also considered.

3.4 Off-chip functions: crystal reference

The 9.8304 MHz crystal oscillator is the stable frequency reference for the system. An on-chip, low gain inverter is used as the oscillator amplifier. A high gain buffer squares the oscillator output and distributes it throughout the chip.

3.5 Off-chip functions: EEPROM

The LibertyLink chip contains only a boot ROM and relies on an off-chip 16 kbit EEPROM for operating instructions. At power up, program code and data is automatically uploaded into LibertyLink's 5k pagable RAM. This firmware can be burned into the EEPROM using a EEPROM writer. It is also possible to reprogram the EEPROM after installation by using RS-232 port and appropriate fixture .

3.6 Off-chip functions: regulator circuit

The regulator circuit is a simple linear regulator. As the battery drops from the fully charged voltage of 2.8V down to 2.1V, the regulator puts out a constant 2.0 V.

3.7 Off-chip functions: battery charging circuit

The headset is power up by 2 x 1.5 v rechargeable Ni-MH batteries. The charging time is around 5 hours.
.

4. System modes operation

Both the base and headset unit can be in the normal operating states and docked states. Each of these states has several sub-modes of operation.

4.1.1. Normal operation, undocked system states (Fig. 10)

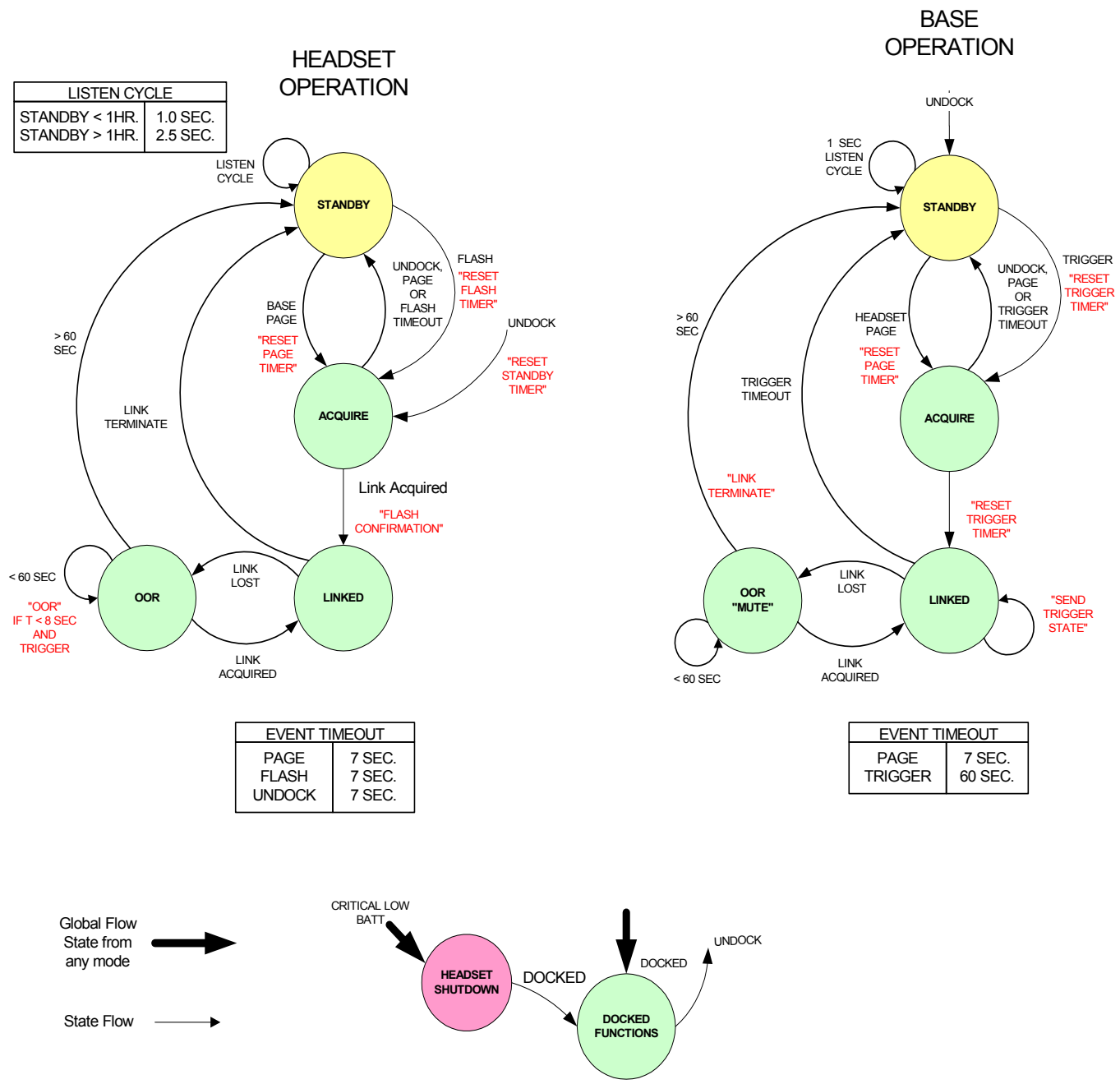


Fig.10. UNDOCKED OPERATIONAL STATE DIAGRAM

4.1.2. Standby

A power management mode of the Headset and Base where the units are listening for the presence of each other when undocked. When one of the pair detects a Page from the other, the pair will transition into the Acquire mode to establish

communication. The interval at which the units listen is dependent on the amount of time that the link has been inactive or if the headset has just been undocked.

4.1.3. Linked

The mode of the pair while in typical use. In this mode bi-directional audio communication occurs. The pair leaves this mode if it goes Out of Range for a preset time period, enters a critical shutdown, is docked, or if the link is terminated by a base timeout

4.2. Docked states (Fig. 11)

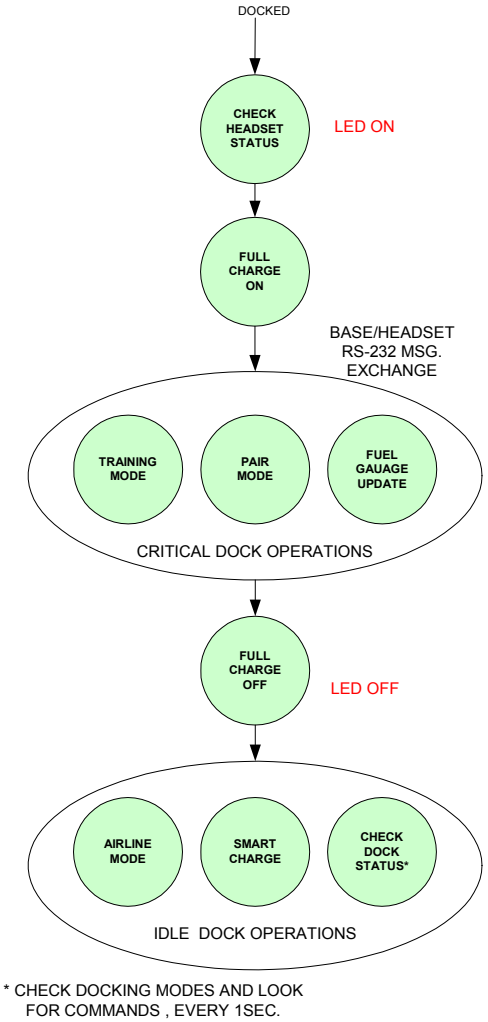


Fig. 11. DOCKED OPERATIONAL STATE DIAGRAM

4.2.1. Airline

This mode puts the Unleash headset and base into an inactive mode. Neither device will transmit or receive thus preventing the units from waking up out of standby mode. This mode will consume very little power. The pair must be docked in order to enter this mode. To exit, simply undock.

4.2.2. Smart charge

The mode in which the Base controls the charging process of the Headset battery using smart charge. Normal user operations are not possible in this mode however the charging mode is programmed to pause for housekeeping routines such as pairing.

5. The wireless headset operation on the system level

Below is a discussion of the headset at the system level, including how the headset interacts with the base unit and how the base unit interfaces to the phone.

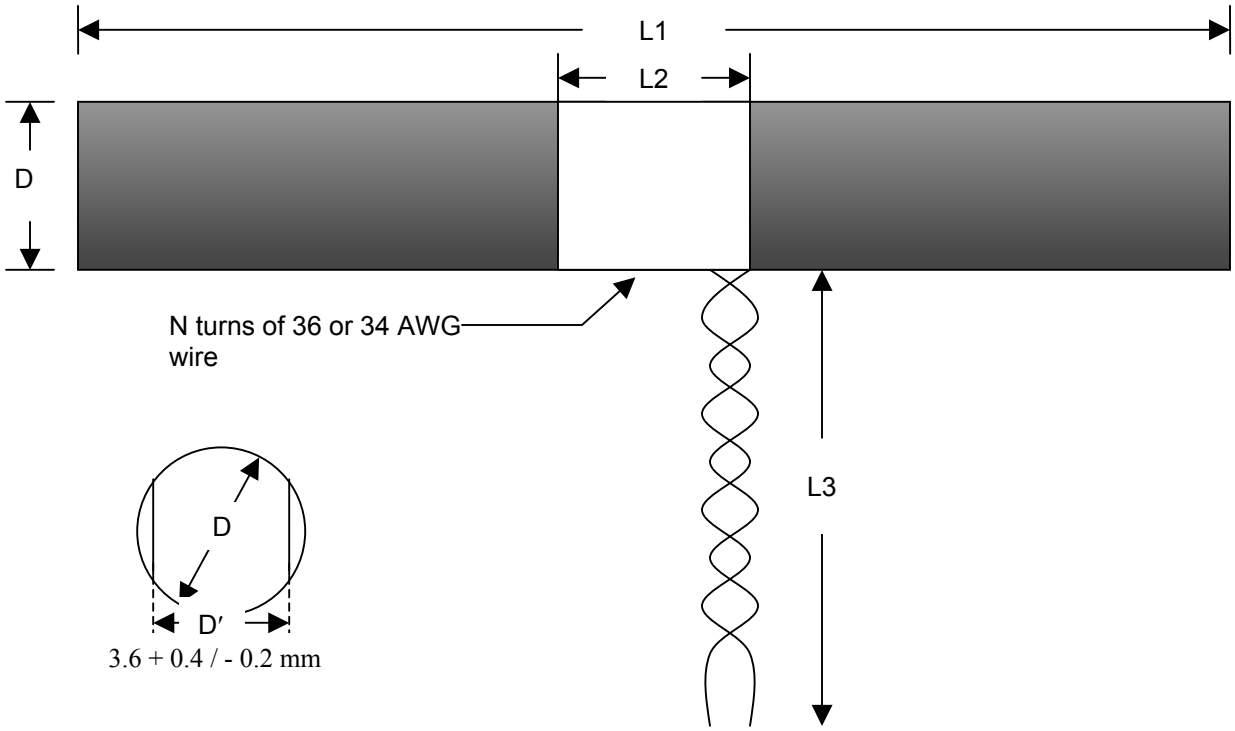
With the phone turned on and both the base and headset in standby mode, a call can be initiated. For outgoing calls, the user will begin by pressing the Flash button on the headset. The headset responds to the flash by calling for a link initiation with the base. Once a link is established, which takes less than a second in normal operating conditions, the system is ready to use. The user can either use the phone's voice recognition function, which requires the keying of one buttons then speaking into the headset, or he can dial the number manually. If the user dials manually, the Flash button is not necessary. Just dial and press 'send' or 'yes' as normal.
For incoming calls the phone responds by signaling the hands-free device that there is a call in progress. This is typically done by bringing the audio input line high, or turning on the Mic_bias pin of the phone. The phone manufacturers enable at least one pin to signal a call and the reference design is configured the to accept this signal on a_aux_3. This signal tells the base to wake from stand-by and begin link initiation with the headset. If the headset is not present (if it is more than 1.25 meters away), the base will continue polling for seven seconds. After seven seconds with no contact, the base will revert back to standby and the user must use the handset. If the headset is present the user will hit the Flash button. Flash will signal the base to answer the call if flash capabilities enable on the phone. If the headset is present and links with the base, but the user does not hit the Flash button, the call will continue to ring unanswered. The phone can be answered in the normal way.

Regardless of how the call is initiated, when the call is complete, the user hits the flash to hang-up. This will signal the base to turn one of the user definable lines (d0) on and pull down the phone_aud_in line. This line is used to signal the phone to switch hook. If the headset goes out of range during a call, the phone reverts to handset mode but does not hang up. The phone can be hung-up in the normal way.

6. Technical Characteristics of the Headset

	Characteristics	**Description**
	Size	20.7 mm diameter x 105.6 mm
	Weight	18 gm
	Talk time	3hr. (180 min)
	Standby time	5 days
	Standby to operate interval	2 sec
	Recharge time	90% 4 hr
	Product life	2 yr
	Operating environment	0 to 120F
	Operator controls	Flash & Volume
	Status indicator	Active audible
	Range to base	4 - 6 ft
	Audio quality	64 kbps CVSD
	Storage environment	-40 to 180 F

Figure 1: Ferrite rod and coil windings



1206 – 101 Headset 4mm X 45 mm Antenna

D	Rod Diameter	4 ± 0.1 mm
D′	Rod Minor Width	3.6 + 0.4 / - 0.2 mm
L1	Rod Length	45 ± 1.0 mm
L2	Winding Length	Not to exceed 1.25mm
L3	Lead Length	40 ± 2mm*
N	Number of turns	6
(not shown)	Winding Diameter With Conformal Coat	4.5 ± 0.1 mm

Rod Material	TDK Q5F
Wire Type	36 or 34 AWG Enameled Magnet

Ls	Series Inductance	1.7 ± 0.1 micro henries @ 13.56 MHz, 10mVRMS.
Q	Quality Factor	Not less than 100.

* NOTE: Varies depending on product design

Winding Instructions:

Wind six turns of 36 or 34 AWG enameled magnet wire in a single layer at the center of the rod. Twist leads with 4 twists per centimeter to required length. Tin each lead end 2mm. Conformal coat windings with suitable non-conductive material.

1206 – 102 Base 4mm X 10 mm Antenna

D	Rod Diameter	4 ± 0.1 mm
L1	Rod Length	10 ±0.3 mm
L2	Winding Length	Not to exceed 1.25mm
L3	Lead Length	10 ± 1mm *
N	Number of turns	8
(not shown)	Winding Diameter With Conformal Coat	4.5 ± 0.1 mm

Rod Material	TDK Q5F
Wire Type	36 or 34 AWG Enameled Magnet

Ls	Series Inductance	1.6 ± 0.1 micro henries @ 13.56 MHz, 10mVRMS.
Q	Quality Factor	Not less than 100.

* NOTE: Varies depending on product design

Winding Instructions:

Wind eight turns of 36 or 34 AWG enameled magnet wire in a single layer within +/- 0.5 mm of the center of the rod. Twist leads with 4 twists per centimeter to required length. Tin each lead end 2 +/- 0.5mm. Conformal coat windings with suitable non-conductive material.

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