Theory of Operation

1. Power Supply

Power supply of the radio is derived from the battery, which supplies battery B+ after passing through fuse 3A and then feeds through power switch. The power supplies voltage for three AVRs. IC504 supplies 5V (M5V) voltage for the control circuit. And IC503 supplies 5V (C5V) voltage for the shared circuit. IC502 supplies voltage for the transmit/receive circuit. In transmit mode, T5C becomes low voltage and Q502 is turned on to supply 5V (T5v) voltage for the transmit circuit. In receive mode, R5C becomes low voltage and Q504 is turned on to supply 5V (R5V) voltage for the receive circuit.

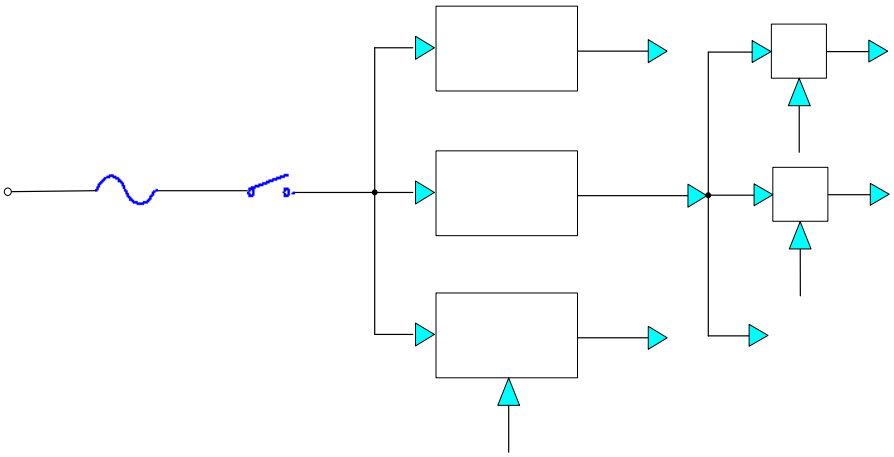

Fig. 1 Power Supply Block Diagram

2. PLL Frequency Synthesizer

PLL circuit generates the first local oscillator signal for reception and RF signal for transmission.

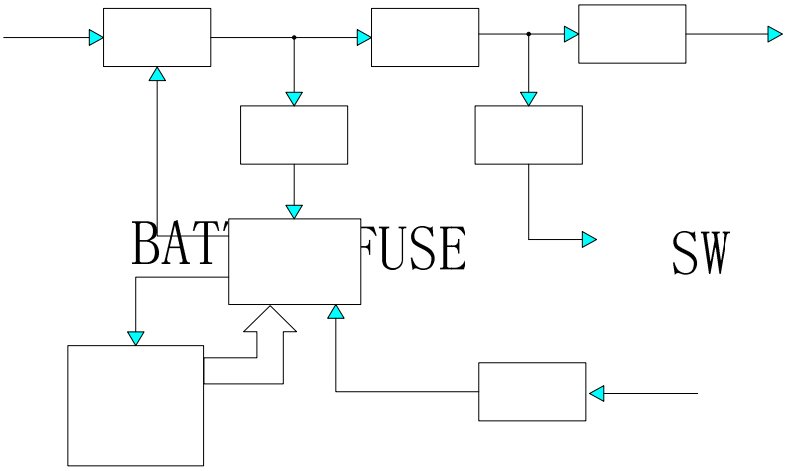

Fig.2 PLL Block Diagram

1） PLL Circuit

Step frequency of PLL can be 2.5 KHz, 5.0 KHz or 6.25 KHz. A 16.8MHz reference oscillator signal is divided at IC301 by a counter to generate a 2.5 KHz, 5.0 KHz or 6.25 KHz reference frequency. Output signal from VCO is buffer amplified by Q301 and divided at IC301 by a frequency divider. The divided signal is compared with 2.5 KHz, 5.0 KHz or 6.25 KHz reference signal in the phase comparator of IC301. The output signal from phase comparator is filtered through a low pass filter to generate a level D.C., and the level D.C. controls oscillator frequency by controlling VCO.

2） VCO

The operating frequency is generated by Q302 in transmit mode and by Q307 in receive mode. Operating frequency generate a control voltage by phase comparator to control varactor diodes so that the oscillator frequency is consistent with the MCU preset frequency(D301、D302、D303 and D304 in transmit mode, and D307、D308、D309 and D310 in receive mode). T/R pin is set high level in receive mode, and low level in transmit mode. The output from Q302 and Q307 is amplified by Q304 and sent to buffer amplifier.

3） Unlock Detector

An unlock condition appears if low level appears at MUXOUT pin of IC301. Transmission is forbidden if this condition is detected by microprocessor.

3. Receiver

The receiver utilizes double conversion superheterodyne (UHF)/(VHF).

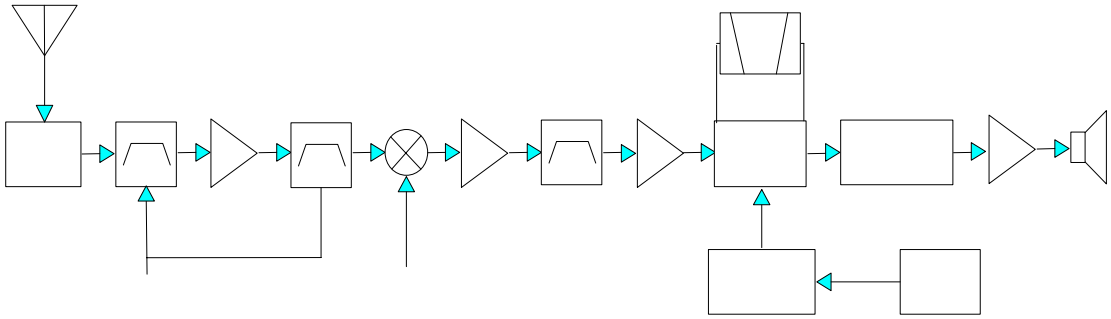

Fig. 3 Receiver Section Configuration

1） Front-end RF Amplifier

The signal from antenna is amplified at RF amplifier (Q207) after passing through a transmit/receive circuit and a band pass filter. Before passing the first mixer, the amplified signal is filtered through another band pass filter to remove unwanted signals.

2） First Mixer

The signal from RF amplifier is mixed with the first local from PLL frequency synthesizer circuit at the fix mixer (IC202) to create a 49.95MHz first IF signal. The first IF signal is then fed through a crystal filter (XF203) to further remove unwanted signals.

3） IF Amplifier

The first IF signal is amplified by Q206 before passing through crystal filter and by Q204 after crystal filter and then enters IF processing chip IC204. The signal from IC204 is mixed with the second oscillator signal again in IC204 to create a 450 KHz second IF signal. The second IF signal then passes through a 450KHz ceramic filter (wideband: CF201，narrowband: CF202) to eliminate unwanted signals before it is amplified and detected in IC204.

4） Narrowband/Wideband Switch Circuit

Pin WCON and NCON of IC500 outputs wideband (high level) and narrowband (low level) controlling signal respectively to turn on corresponding diode-connector, and to choose ceramic filter CF201 (wideband) or CF202 (narrowband) to filter useless spurious signal.

5） AF Amplifier

The resulting AF signal from IC204 enters base band processing chip IC408. The processed AF signal is then amplified by an AF power amplifier (IC401) to drive the speaker.

4. Transmitter

1） AF and Signaling

AF signal from the microphone is amplified and low-pass-filtered in IC402 before it enters base band processing chip IC408, which also enters CTC/CDC/DTMF/2-Tone/5-Tone etc signaling generated by CPU. The IC408 processed mixing signal enters VCO for direct FM modulation (see fig.5).

2） RF Power Amplifier

The transmit signal from VCO buffer amplifier (Q111) is amplified by Q101 and Q102. The amplified signal is then amplified by the power amplifier Q103 and Q104 (including a two-stage FET amplifier) to create 4.0W (UHF)/5.0W (VHF) RF power (see Fig. 6).

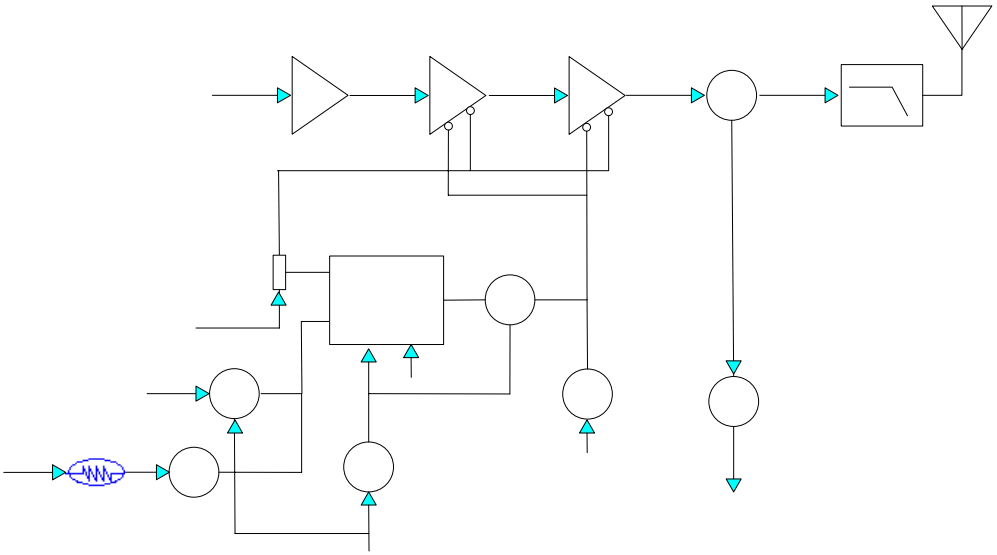

Fig. 4　APC System

3） Antenna Switch and LPF

Output signal from RF amplifier passes through a low-pass filter network and a transmit/receive switch circuit comprised of D102，D103 and D104 before it reaches the antenna terminal. D103 and D104 is turned on (conductive) in transmit mode and off (isolated) in receive mode.

4） APC

The automatic power control (APC) circuit stabilizes the transmit output power by detecting the drain current of final stage amplifier FET. IC101 (2/2) compares the preset reference voltage with the voltage obtained from final current. APC voltage is proportional to the difference between auto detect voltage and reference voltage output from IC101 (1/2). The output voltage controls FET power.

5. Base Band and Signaling System

The block diagram of signaling section is shown as figure 5.

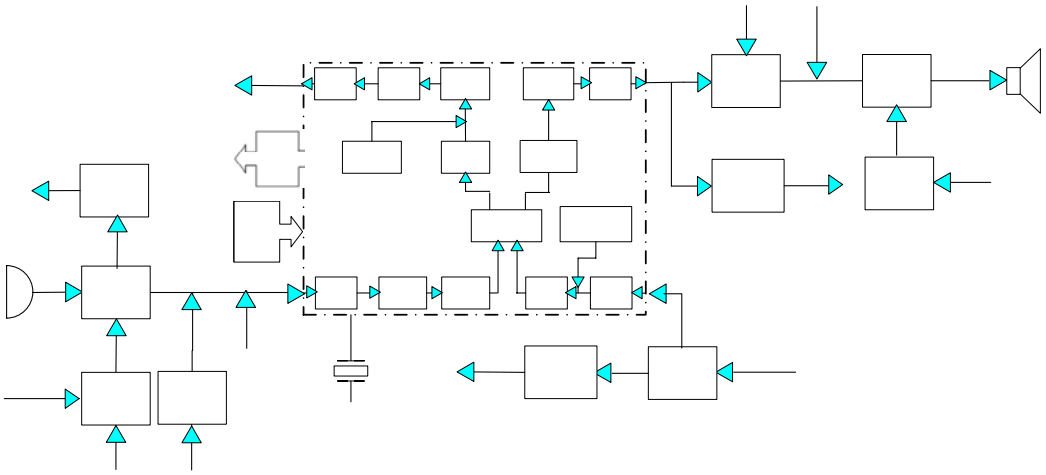

Fig. 5 AF and Signaling Circuit

1） CTC/CDC

Transmit: CTC/CDC signaling produced by CTC_PLL pass a low pass filter and then enters VCXO. CTC/CDC signaling produced by CTC_OUT pass a low pass filter and then mixed with AF before enters VCO.

Receive: Demodulated signal enters MCU after pass IC404、IC405. MCU then judges whether CTC/CDC matches the preset values or not. According the result, the out tone will be controlled by AFMUTE.

2） 2-Tone / 5-Tone and DTMF

Transmit: The signal produced by MCU provides a TX and SP out tone, and is then applied to the base band processing IC. The signal in mixed with the audio signal and goes to the VCO。

Receive: Demodulated signal is filtered after passing base band processing IC, and then enters MCU for decoding.

AUDIO PROCESSO
IC408
AK2346
MOD
SMF
VR2
Splatter
AFCK
CODIC
AFRDF
MSK
Modulator
Limiter
VOX
D402
RB706F-4C
AFDI
AFSK
AFDIR
1/20SD
TONEC
Scrambler
DeScramble
MIC

3） MSK

Transmit: MSK signal produced by base band processing IC enters VCO together with AF signal for modulation.

Receive: MSK input of demodulating IC is sent to AK2346 for demodulation after being amplified. The demodulated signal is then sent to MCU for decoding.

4） AF

Transmit: AF signal from MIC enters base band processed IC for amplification, pre-emphasis etc. after being amplified. And then it enters VCO for modulation.

Receive: Demodulated AF signal enters the base band processing IC for amplification, de-emphasis etc. after being amplified. And then it enters AF power amplifier drived speaker.

Base band processed chip provides functions for processing signal as amplifying, filtering, emphasizing, scrambling, companding, and amplitude limiting.

6. Control System

The IC500 CPU operates at 9.8304 MHz.

The block diagram of MCU control system is shown as following：

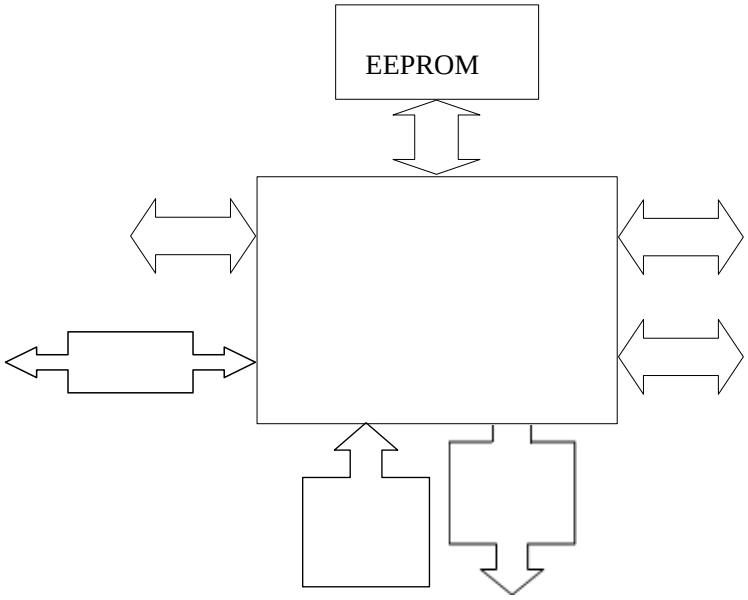

Fig.6 MCU Block Diagram

Circuit in this section is mainly comprised of MCU, EEPROM etc.

MCU control circuit accomplishes the following functions: accomplish the reset initialization according to the programmed feature of the radio when power on; detect keying signal and monitor battery voltage; send necessary frequency data to PLL

according to encode of the channel; switch and control transmit/receive according to the signal input from PTT; turn on/off the mute circuit according to the input signaling decode signal and squelch level signal; output control signal to control the light/off of LED; control signaling process IC to perform tasks.