DART Radio Module User Manual

Overview

The DART radio module is a compact low-power high-speed transeiver radio module with small integrated dipole antenna for use in the unlicensed 2.4Ghz ISM band.
It uses a fixed length data buffer of maximum 256 bytes to store data packets for transmission and reception. Each device has a fixed length bit address to receive only data sent to it. When data has been recieved, the DataReady pin goes high, and the data packet can be unloaded from the data buffer via the serial interface. In transmit mode, the packet to be sent is loaded into the device, and the ChipEnable pin is used to initiates transmission of the data at the 250Kbps RF rate. The high-power setting outputs a 0dBm, the low-power setting is -20dBm

Interface Pins

The module has a 7 pin .100 header with the following interfaces, Vcc, ChipEnable, ConfigSelect, DataReady, Clock, Data, and Ground. Vcc should be from 3.0Vdc to 3.3Vdc over Ground.

Configuration

Before the module can function, it must have a 120 bit configuration word loaded into the device. A 3ms delay must occur after power is applied before the configuration can be loaded. The ChipEnable should be low, the ConfigSelect pin should be high. Configuration data is passed in MSB order, using the Clock and Data pins to load serial data 1 bit at a time. The Data pin should contain the bit value, low is zero, high is one, and then the Clock pin should be toggled low-high to load in the Data bit. After the data is loaded, the ConfigSelect pin should go low. The device is now active using the loaded data. Once the initial configuration is loaded, updates can be loaded with just the data that must be changed. For example, the tx/rx mode switch can be done loading a single bit

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The configuration data is as follows

Bit Position	value
119 - 112	size of data packets (max 256)
111 - 104	size of data packets
103 - 64	device address
63 - 24	device address
23 - 18	size of device address (max 40)
17	CRC mode, 0=8bit, 1=16bit
16	CRC enable, 0=disable, 1=enable
15 - 10	value = 0x13
9 - 8	RF power, 0 = low, 3 = high
8 - 1	RF Channel, 2 to 81 for 2.400+ch
0	RX, 0=TXmode, 1=RXmode

Transmit

Once TX mode is configured, the ChipEnable pin should be low. The ChipEnable pin should be set high, then a data packet of the configured size should be transferred to the device, starting with the address. Then the ChipEnable pin goes low to initiate the transmission on the configured channel.

Receive

Once in RX mode, the device is monitoring for RF on the configured channel for data that matches its address and has a valid CRC. When a valid packet has been recieved, the DataReady pin will go high. The packet data can now be transferred from the device using the Clock and Data pins. The Data pin will have the current bit value in MSB order. A low-high transition on the Clock pin will shift the next bit to the Data pin. Once all data is transferred, the DataReady pin will go low, and the device will again wait for a valid packet to be received.