SpectraLux Corporation
12335 134th Court NE
Redmond, WA 98052

April 14, 2004

Letter Reference Number: 04-14-04-LFT001

Reference (1): CKC FCC Part 2.1033(c) Certification Submittal Checklist

Mary Ellen Clayton
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Attachments:
(1) Appendix A: Letter of Authorization
(2) Appendix B: General Agreement
(3) Appendix C: FCC Drug Compliance Letter
(4) Appendix D: Letter of Grantee Code Authorization
(5) Appendix E: Letter Requesting Confidentiality
(6) Appendix F: DLink+ Systems Requirements Document
(7) Appendix G: DLink+ Users Manual
(8) Appendix H: Schematics
(9) Appendix I: Nameplate Drawing
(10) Appendix J: Photographs
(11) Appendix K: ARINC AQP Phase 3 Test Report
(12) Appendix L: FAA TSO Approval Letter

Dear Mary Ellen,

Subject: Submission of Data Delineated in FCC Submittal Checklist

The purpose of this correspondence is to provide responses to the items listed in Reference (1). Enclosed with this letter is a CDROM which contains all of the Appendices. The following are the responses to the items listed in Reference (1):

Equipment Name: DLink+

Model Number: The DLink+ is identical to the Model CMS-1000 except for the nameplate. In several of the appendices herein, the documentation is for the CMS-1000. All CMS-1000 documentation is directly applicable to the DLink+. The name of the CMS-1000 was changed to DLink+ for marketing reasons.

Letter of Authorization: Refer to Appendix A

General Agreement: Refer to Appendix B

FCC Drug Compliance Letter: Refer to Appendix C

Letter for Grantee Code Authorization: The grantee code authorization number is R2H. Refer to Appendix D

FRN Number: 0010603223

Letter Requesting Confidentiality: Refer to Appendix E

Fees: Please invoice Spectra Lux Corporation for all fees, attention Bob Bernstein.

Frequency Tolerance: Frequency Tolerance is ±5 ppm of selected frequency

Operational Description: The DLink+ is a VHF Data Link device. It operates over the ARINC ground based VHF network in the frequency range of 117.975 MHz to 136.975MHz. It transmits in two modes of operation. One mode utilizes a Minimum Shift Keying (MSK) approach to modulation of the carrier frequency. The keying is between 1200 Hz and 2400 Hz. This allows for a data rate of 2400 Bits/Second. The other mode uses a Differential 8 Phase Shift Keying approach to modulation of the carrier frequency. The BIT rate for this mode is 31,500 Bits/Second (10,500 Symbols/Second, each symbol representing 3 Bits). For a more complete description, please refer to Appendix F.

Name of Applicant/Manufacturer: The applicant, and the manufacturer are:

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Product Line Manager

FCC IndentifierL R2H13281-1

Installation and Operating Instructions: Refer to Appendix G.

Type or types of emissions: Emissions Designator: **W7D**

RF Emissions From the Unit::

The unit complies with Section 21, Category M RTCA DO-160D standards for LRU RF Emissions. The following characterizes the emissions from the RF Transmitter.

Spurious Emissions from Transmitter:

When the transmitter is active and operating at full power, and terminated in a resistive load equal to the nominal output impedance, the power of any spurious emission at the output of the transmitter is as follows:

- <0.25 microwatts within a bandwidth of 1 KHz on any frequency in the range of 9 kHz to 150 kHz
- <0.25 microwatts within a bandwidth of 10 KHz on any frequency in the range of 150 kHz to 30 MHz
- <0.25 microwatts within a bandwidth of 100 KHz on any frequency in the range of 30 MHz to 108 MHz
- <0.25 microwatts within a bandwidth of 100 KHz on any frequency in the range of 108 MHz to 117.5 MHz
- <0.25 microwatts within a bandwidth of 10 KHz on any frequency in the range of 117.5 MHz to 117.8 MHz
- <0.25 microwatts within a bandwidth of 10 KHz on any frequency in the range of 137.175 MHz to 137.475 MHz
- <0.25 microwatts within a bandwidth of 100 KHz on any frequency in the range of 137.475 MHz to 1 GHz

Additionally, the level of spurious emissions at discrete frequencies, excluding harmonics) in the following bands does not exceed 4 nanowatts

- 47 to 68 MHz
- 88 to 108 MHz
- 162 to 244 MHz
- 328 to 336 MHz

- 470 to 862 MHz

Harmonic Emissions from the Transmitter:

Harmonic emission products are less than 60 dB below rated RF output power (-60 dBc).

Frequency Range: The unit operates at discrete frequencies spaced 25 kHz apart starting at 118 MHz and ending at 136.975.

Range of Operating Power: When on the ground (in the airport environment) the unit's RF power is restricted to 4 watts. When not on the ground and in Mode 0 (MSK) modulation, RF power is at 10 ±1 watts. When not on the ground and in Mode 2 (D8PSK) modulation, RF power is 15±1 watts.

Maximum Operating Power: 16 watts

DC Voltages Applied and DC currents of final RF Device in Normal Operation:

Bias Driver PA Voltage:	3.97V
Bias HPA Voltage:	3.72V
Driver PA Current:	234 mA
HPA Current:	1.61 A
Total Current:	1.844 A
Total Gain:	31 dBm

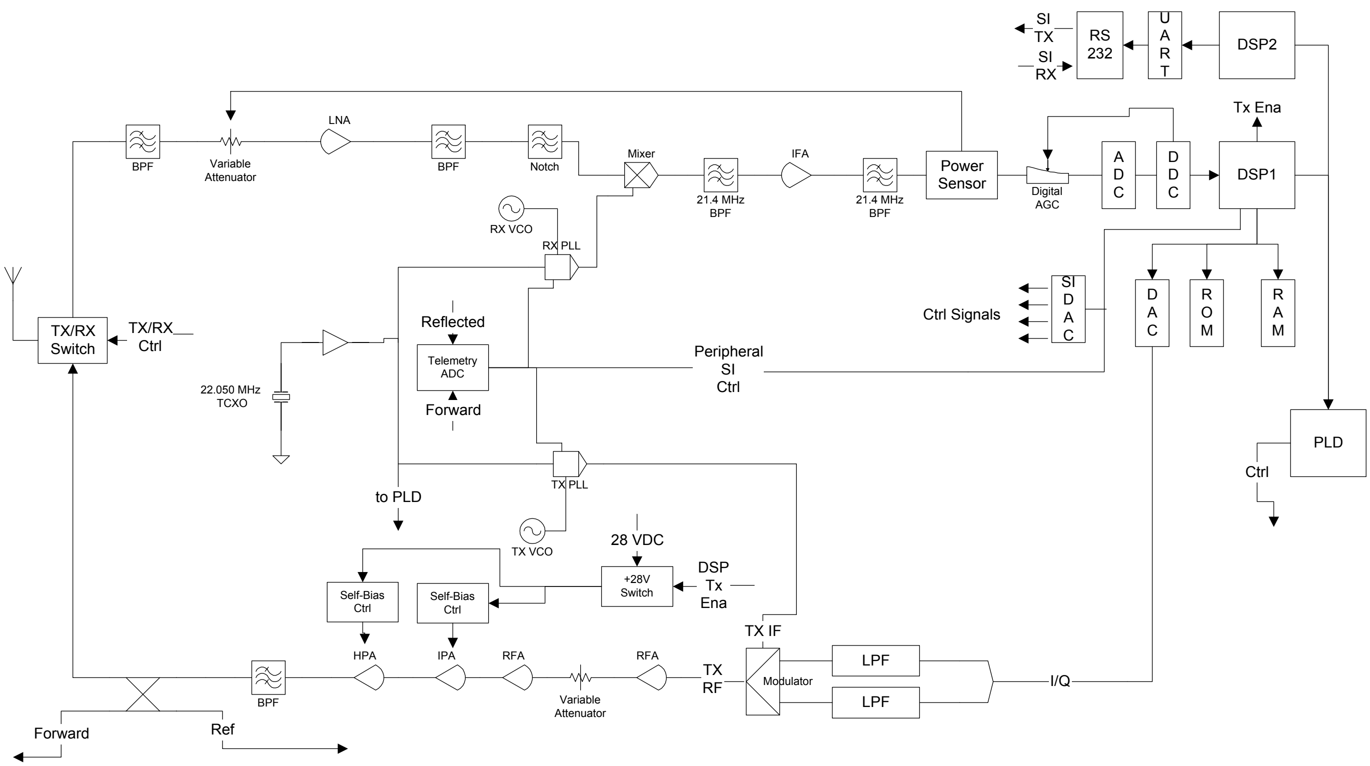
Tune-up Procedure: The procedure for operational tuning is detailed in ARINC Specification 618-4 in section 5.6. To briefly summarize the procedure, the unit, at power up, is tuned to 131.55 MHz. It awaits an uplink (usually in the form of a squitter). The squitter is broadcast from the ARINC ground station on the base frequency (131.55 MHz) about every 2 minutes in light traffic and every 10 minutes in heavy traffic. The squitter instructs the unit what frequency to tune to and broadcast on. The unit then sends a link message and two way communications are established. During this process (while at 131.55 MHz) the unit transmits in Mode 0 (MSK). The squitter may instruct the unit to tune 136.975 MHz and indicate that the station supports Mode 2 operation (D8PSK), in which case the unit will transmit and link up in Mode 2. Otherwise the unit will stay in Mode 0. The only current frequency used for Mode 2 operation is 136.975 MHz. The following table summarizes the Mode 0 frequencies which may be used:

Frequency	Use
131.550	Primary Channel worldwide
129.125	Additional channel for USA & Canada
130.025	Secondary channel for USA and Canada
130.425	Additional channel for USA
130.450	Additional channel for USA & Canada
131.125	Additional channel for USA
131.450	Primary channel for Japan
131.475	Air Canada company channel
131.525	European secondary
131.725	Primary channel in Europe
136.700	Additional channel for USA
136.750	Additional channel for USA
136.800	Additional channel for USA
136.900	European secondary

Frequency	Use
136.925	ARINC European Channel
136.85	SITA North American Frequency
136.750	New European frequency
131.850	New European frequency

Schematic Diagram and Description of Circuitry:

The following figure is a simplified schematic of the unit's internal VHF digital radio. The detailed schematics are contained in Appendix H.



The following is the design assumptions and baseline which was used for the radio design:

The VHF Data Link (VDL) CCA is the RF to CMU interface component of the CMS transceiver, a half-duplex radio that enables ARINC 750-2 based communications.

The VDL implements a digital radio design to reduce circuit complexity and size. AGC, modulation and demodulation is implemented via digital circuitry. The digital receiver is implemented once the signal of interest (SOI) has been downconverted to a 21.4 MHz intermediate frequency (IF). For purposes of simplicity, direct upconversion was used for the transmitter.

Software on the VDL CCA is responsible for implementing a CSMA link protocol to ensure network access. This software manages the VDL transmit and receive physical links to ensure messages are transmitted and received correctly. A database of link statistics is maintained in accordance with the SARPS and 750-2 specifications.

In order to feed the envelope detector of the AGC circuit properly, the in-band sampling alias must fall into a very narrow band, which is a function of the sampling frequency. In general, the following guideline applies when selecting the alias, Fa:

$$Fck/16 < Fa < Fck/10$$

The lower limit of Fck/16 applies in order to ensure that the 2nd harmonic of the alias will fall outside the passband and not interfere with the power estimate of the AGC.

Therefore, given that IF = 21.4 MHz, and the analog filter BW prior to the AGC stage =200 kHz, we can make an initial estimate for Fck as follows:

$$IF = 3*Fck + Fx.$$

Here, we imply that the alias signal will be the product of in-band sampling with the 3rd order product of Fck. This assumption is required because Fck must be an integer multiple of 73500 and 25000, and the 2nd harmonic of the alias signal must be low-pass filtered in the AGC circuitry.

Choosing Fx = Fck/15, we get:

$$21.4e6 = 3*Fck + Fck/15$$

Solving yields:

$$Fck = 6.97826 \text{ MHz}.$$

However, since we know that our target Fs, after decimating Fck is73,500 (7 samples per symbol), we must hone Fck to yield a result which is an integer multiple of Fs. Additionally, Fck must also be an integer multiple of the PLL channelization frequency, 25 kHz. Therefore, the closest value of Fck which meets these requirements is 7.35 MHz, which requires decimation factors of CIC=25 and FIR=2.

The resulting alias signal is 21.4 – 3*7.5 = -650,000 Hz.

Verifying that this Fa falls within the required bounds, we see that it is just slightly smaller in frequency than our intended limits:

Fck/16	689,063
Fck/8	1,378,125
2*Alias	1,300,000

However, the values are close enough to ensure that the 2nd harmonic of the alias will be sufficiently attenuated by the envelope detector circuit and will not affect our results.

The filter band restrictions also make it impossible to sample wideband data because the resulting aliases will not meet the filtering requirements of the AGC circuit. For example, to sampling a 20 MHz band, we need a sampling rate of at least 46 Msps in order to meet Nyquist requirements and prevent the generation of image frequencies. Regardless, since 46/10 is much less than many of the resulting alias frequencies (46*3 – 118 = 20 MHz), there is no way for a wideband design to meet the filtering requirements of the AGC. However, our narrowband downconversion approach does work.

Sampling a single channel without adequate out-of-band rejection introduces aliases with unresolvable ambiguity. This is because the in-band sampling LO (3rd harmonic of 7.35 Msps) is located within the targeted frequency band. Sampling an IF of 21.4 MHz with 7.35 Msps, the resultant alias signal is at 650 kHz. The image of the IF signal is at 22.70 MHz, which is 1.3 MHz from the IF. This signal will also be aliased to 650 kHz if it is not attenuated sufficiently prior to sampling. Therefore, the anti-aliasing filter implements sufficient attenuation to prevent the image frequency from interfering with the demodulation of the IF. The attenuation requirement is derived by examining several parameters, including:

- Minimum received signal
- Maximum received signal

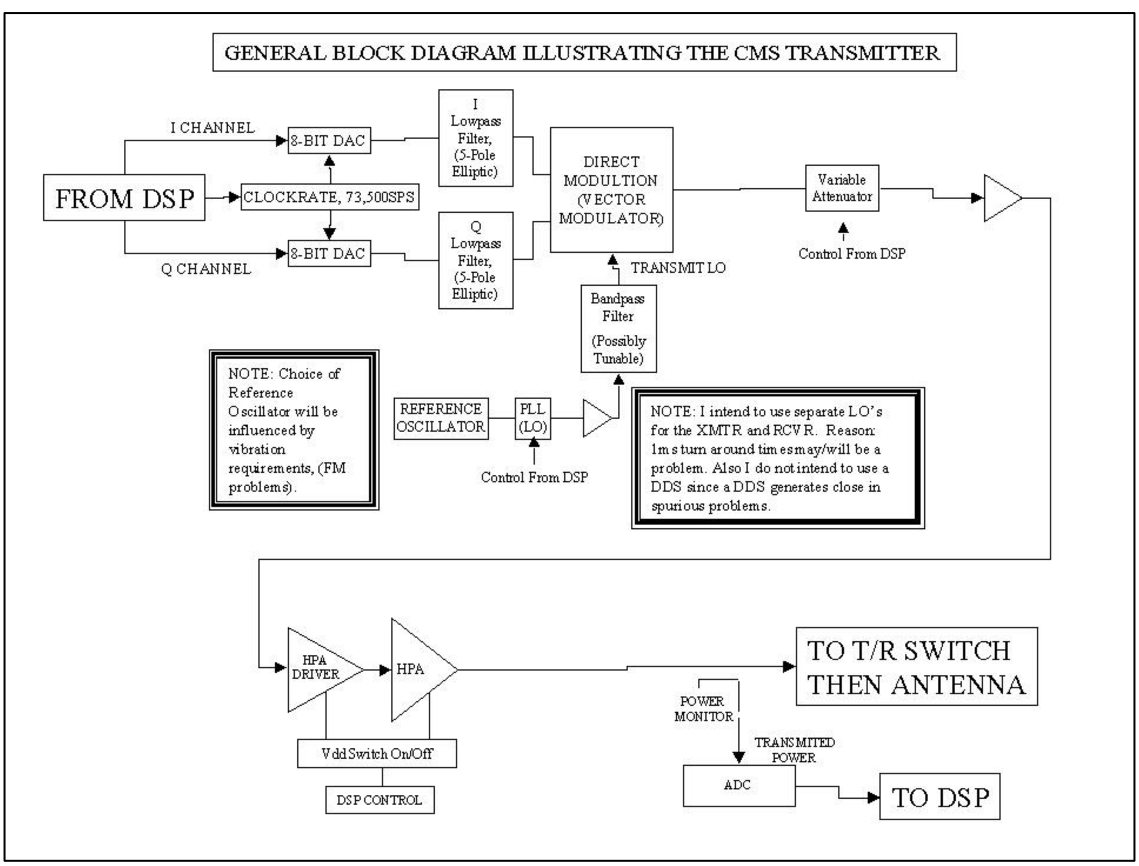
The minimum received signal is calculated as follows:

Noise floor = thermal noise + receiver noise figure + bit density + Eb/No
= -174 dBm + 12 dB + 45 dB + 13 dB = -104 dBm

The maximum received signal is specified to be –5 dBm. Therefore, we accommodate a dynamic range of 99 dB. The image frequency is attenuated by 100 dB to eliminate it as a source of interference. This is accomplished by cascading two crystal filters. The first filter implements the targeted close-in bandwidth of +/- 12.5 kHz with a stop-band attenuation of 50dB or better at +/- 50 kHz. The second filter is slightly wider (about 50 kHz wide) to reduce the effects of group delay and ripple. It has a stop-band attenuation of 50 dB or better at 100 kHz. An LNA is placed in between the filters to buffer the signal between the filter stages.

The first filter stage knocks down an adjacent channel by about 20 to 40 dB. Digital filtering in the DDC and DSP provide the remaining 60 to 80 dB of required attenuation.

The TX CCA consists of a single direct upconversion stage, a driver stage, a high power amplifier (HPA), HPA power controller and RF synthesizer. The transmitter RF design is based on the architecture shown in the following Figure.



Transmitter Input

The transmitter CCA accepts as an input I and Q channel signals with channel bandwidths of approximately 5.25kHz.

Direct Conversion Modulator

The transmitter uses a quadrature modulator to modulate the carrier with the baseband signal. The modulator is a vector modulator. At the output connector the EVM (Error Vector Magnitude) are 6% or less.

High Power Amplifier (HPA)

The HPA consists of a single power transistor operating in a class AB configuration. Over the –40° to +85° C operating temperature range the HPA is capable of delivering up to 16 watts at any channel at the output connector across the designated frequency band. Output power is adjustable by command from the DSP. The drive level to the HPA does not change bias voltages, etc. Drain voltage is 28VDC.

HPA Driver

The HPA driver consists of a single power transistor operating in class A. Drain voltage is 28VDC.

HPA Power Controller (HPC)

Output power is controlled by the HPA Power Controller (HPC). The HPC consists of an absorptive PIN diode attenuator placed in front of the HPA driver. The HPC is controlled by the DSP. Dynamic range of the HPC is 20 dB. Minimum attenuation corresponds to maximum output and maximum attenuation corresponds to minimum output power.

Transmitter RF Synthesizer

A PLL synthesizer (TxPLL) is used to provide a direct modulation LO covering the 117.975 to 137 MHz frequency band. The TxPLL is tunable in 25 kHz steps. The same 22.05MHz clipped sine wave clock oscillator shall providing the reference clock for the receiver LO PLL is used for the transmitter PLL LO. The transmitter LO synthesizer shall meet the same phase noise mask requirements as the receiver LO synthesizer. From 10 Hz to 100 Hz, -60dBc/Hz, from 100Hz to 1kHz, --90dBc/Hz, from 1kHz to 10kHz, -115dBc/Hz, from 10kHz to 100kHz, -125dBc/Hz and from 100kHz to 1MHz, -130dBc/Hz. At 12.5kHz offset, the phase noise is less than -113dBc/Hz. The synthesizer settling time is less than 2 milliseconds when tuning from the low end of the band to the high end with a tolerance of 1000Hz. The Tx synthesizer circuit provides a signal level no less than 7 dBm and no greater than 10 dBm to the vector modulator. The synthesizer is serially programmed using a CMOS level clock, data and chip select signals. A CMOS level compatible, buffered lock detect from the PLL IC is provided as telemetry for monitoring by the controller CCA.

Frequency Stability

The transmitter has an overall frequency stability of ±5ppm, including the effects of temperature, -40° to +85° C.

VSWR Stability

The transmitter is capable of operating into a 2:1 VSWR at any phase with no degradation in performance, except for a +/- 1 dB RF output power variation with corresponding DC power draw. The transmitter does oscillate or increase spurious emissions beyond limits specified in the emissions discussion above herein when subjected to a load with a 2:1 VSWR at any phase.

For a VSWR of 3:1 In-Band and Infinite Out-of-Band, at the transceiver RF connector, the output power does not degrade by more than 3 dB when the relative electrical phase at the RF connector is varied by up to one-half wavelength.

The transmitter does not suffer permanent damage when loaded with an Infinite VSWR at any phase angle.

Transmitter Duty Cycle

The transmitter tolerates a duty cycle of at least 20%. A transmitter may transmit continuously for a maximum of 15 seconds.

Digital Signal Processor

A digital signal processor (DSP) is capable of feeding samples to the transmitter DAC at rates up to at least 73500 sps. The DSP is shared with the receiver so as to operate in a half-duplex mode as commanded by the Transmit/MAC management Task (TMMT).

The TMMT implements a CSMA network access protocol and ensures that messages are transmitted and received appropriately. The TMMT forwards incoming messages from the SBC to the Transmit Physical Layer Task (TPLT). The TMMT maintains statistics on all messages that are transmitted.

The TPLT ensures that the transmit timer interrupt is properly configured and converts the data to be transmitted into the appropriate waveform as specified in the SARPS.

Transmitter DAC

A transmitter DAC is utilized which is capable of operating at an input sample rate of at least 73500 sps. The DAC has 8 bits resolution with a SFDR of –65 dBc or better.

DAC Reconstruction Filter

A DAC reconstruction filter follows the DAC. The filter characteristics are sufficient to attenuate the first DAC image at Fclk-Fsig to less than –80 dBc. The passband of the filter has a flatness of +/-0.1 dB and less than 200 nanoseconds of group delay.

Nameplate Drawing: We have allocated space for the FCC ID on the label drawing. The “XXX” will be replaced with the FCC number as soon as available. Refer to Appendix I.

Photographs: Refer to Appendix J.

Existing Certifications: The unit has completed ARINC AQP Phase 3 testing and scheduled to start Phase 4 testing (flight testing) on the ARINC VHF network in early May, 2004. Appendix K is the ARINC Phase 3 Test report. The unit has also received TSO approval from the FAA. Appendix L contains a copy of the approval letter.

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