Exhibit V: Frequency Block Diagram

FCC ID: QYT-4120

REMOTE INTELLIGENT COMMUNICATIONS (RIC)
4120 Interrogator

1. 4120 INTERROGATOR INTRODUCTION

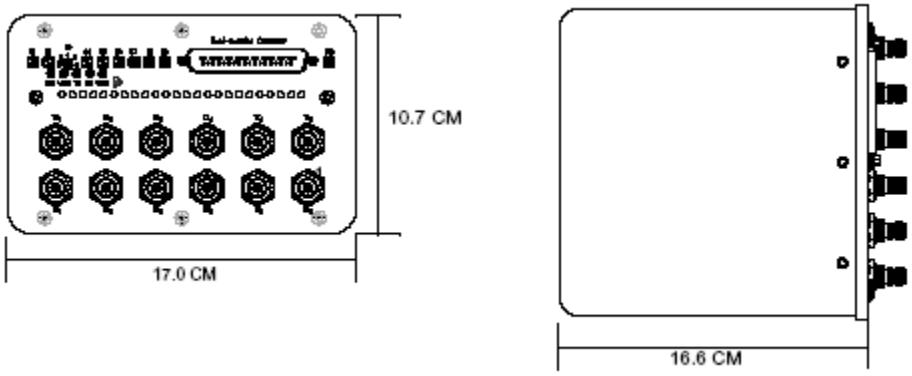
The IDmicro, Inc. (IDM) Remote Intelligent Communications (RIC) 4120 interrogator provides the communication functions necessary to implement a radio frequency identification (RFID) system using IDM RIC tags.

When running custom embedded application software on the internal Motorola MC68340 microprocessor, the interrogator manages all radio frequency (RF) communications with tags.

The 4120 interrogator can communicate digitally with a broad range of user-selected external devices through multiple, configurable, industry standard serial interfaces.

For detailed information on programming the 4120 interrogator, see the RIC *Developer's Reference Manual*. To learn more about how the RIC system can work for your business:

- call toll free (within the U.S.) 1.877.395.1479
- visit the IDmicro, Inc. web site at www.idmicro.com
- dial the U.S. country code and 1.253.396.1479



2. PHYSICAL COMMUNICATION PROTOCOL

The interrogator-to-tag and the tag-to-interrogator communications use different physical protocols. Both communication protocols are discussed in the following paragraphs.

2.1 Interrogator-to-Tag Physical Communication Protocol

The interrogator-to-tag physical communications protocol is called the “forward link” protocol. The interrogator sends forward link data in the following order:

CallSign
Preamble
Barker Code
Command Packet
Checksum

2.1.1 Spread Spectrum “Chipping” Pattern

A maximal length pseudo noise (PN) sequence is used in the direct sequence spread spectrum (DSSS) communications scheme in the forward link. A linear feedback shift register of the form [5,2] generates the sequence. There are five registers, and the output of register 2 is X-ORed with the output of register 5, and the result is fed into the input of register 1. This produces a repeating 31 “chip” sequence. The sequence ends with all registers set to 1. The sequence is taken from the output of register 1. This code is synchronous with the data in that each data bit comprises one, full PN sequence. The chip sequence for each bit is:

001 1010 0100 0010 1011 1011 0001 1111.

A zero bit is transmitted as one inverted full cycle of the PN sequence. A one bit is transmitted as one non-inverted full cycle of the PN sequence. The chip sequences are used to amplitude modulate (AM) a 2.4 GHz carrier.

2.1.2 CallSign

The CallSign consists of a Bit Sync, 33 bits; a Frame Sync, 31 bits; and a Calling Code, 63 bits. The Bit Sync is an alternating pattern of 1s and 0s starting with a 1. The Frame Sync is:

000 1101 1101 0100 0010 0101 1001 1111.

The Calling Code is user defined and can only be programmed once with a valid Calling Code. An invalid Calling Code of all 0s or all 1s prevents RF transmissions.

2.1.3 Preamble

The preamble precedes the data. The format for the preamble is:

1. a series of zeros for a duration equal to the wakeup interval (0.5, 4, 16, or 256 ms) plus a guardband followed by
2. a 13-bit start (Barker) code.

The Barker code is defined by the following bit string:

1111 1001 10101.

2.1.4 Command Packet

The command data is grouped into 13-bit words. Each word comprises 8 data bits and 5 error correction code (ECC) bits. The bit transmission order is (D7 is transmitted first):

D7, D6, D5, D4, D3, D2, D1, D0, P4, P3, P2, P1, P0...

The block ECC bits (P4-P0) are generated using the following equations:

P0 = (D1 + D2 + D5 + D7) modulo 2
P1 = [(D1 + D3 + D4 + D6) modulo 2] Complement
P2 = (D0 + D2 + D3 + D6 + D7) modulo 2
P3 = [(D0 + D4 + D5 + D6 + D7) modulo 2] Complement
P4 = (D0 + D1 + D2 + D3 + D4 + D5) modulo 2

The forward link has an effective data rate (adjusting for PN and ECC) of 189.3 Kbps.

2.1.5 Checksum

A 16-bit checksum[1] detects bit errors on the packet level.

[1] The protocol calls for a 16-bit CRC that will be implemented on future products.

2.2 Tag-to-Interrogator Physical Communication Protocol

The tag-to-interrogator physical communications protocol is referred to as the “return link” protocol. The return link messages are sent in the following order:

Preamble
Barker Code
Reply Packet
Checksum

2.2.1 Return Link Modulation

The return link uses a frequency hopped modulated backscatter protocol. After sending a command, the interrogator sends a continuous unmodulated RF signal on one of its pseudo-randomly selected channels. Return link data is differential phase shift key (DPSK) modulated onto a square wave subcarrier with a frequency of 596 kHz. A data 1 corresponds to no phase change from the previous bit, and a data 0 corresponds to a 180° phase change from the previous bit. The subcarrier is used to modulate a tag’s antenna impedance. For a simple dipole antenna, a switch between the two halves of the dipole antenna is opened and closed. When the switch is closed, the antenna becomes the electrical equivalent of a single half-wavelength antenna that reflects a portion of the power being transmitted by the interrogator. When the switch is open, the antenna becomes the electrical equivalent of two quarter-wavelength antennas reflecting very little of the power transmitted by the interrogator.

2.2.2 Preamble

The preamble contains the following bit stream:

1. preamble (1250 bits, alternating zeros and ones, before differential encoding) and
2. a 13-bit start (Barker) code.

The following bit string defines the start or “Barker” Code:

1111 1001 1010 1.

2.2.3 Reply Packet

The data is grouped in 13-bit words. Each word is composed of 8 data bits and 5 ECC bits. The block encoded sequence is:

D7, D6, D5, D4, D3, D2, D1, D0, P4, P3, P2, P1, P0.

The block ECC Bits (P4-P0) are generated using the following equations:

P0 = (D1 + D2 + D5 + D7) modulo 2
P1 = [(D1 + D3 + D4 + D6) modulo 2] Complement
P2 = (D0 + D2 + D3 + D6 + D7) modulo 2
P3 = [(D0 + D4 + D5 + D6 + D7) modulo 2] Complement
P4 = (D0 + D1 + D2 + D3 + D4 + D5) modulo 2

The bit duration is 6.71 μs; resulting in an effective data rate of 91.75 Kbps.

2.2.4 Checksum

A 16-bit checksum[2] is provided to detect bit errors on the packet level.

2.2.5 Interleaving

Each pair of data words is interleaved, starting with the Barker code and the first data word. The transmitted bit order for two sequential words, A and B, is D7A, D7B, D6A, D6B, D5A, D5B, D4A, D4B, D3A, D3B, D2A, D2B, D1A, D1B, D0A, D0B, P4A, P4B, P3A, P3B, P2A, P2B, P1A, P1B, P0A, P0B. D7A is the first transmitted bit. DPSK is applied to the interleaved data.

3. INTERROGATOR HARDWARE DESCRIPTION AND SPECIFICATION

Two circuit card assemblies (CCAs - digital CCA and RF CCA) and a chassis comprise the main components of IDM's interrogator. Figure 1 illustrates a high-level block diagram of data flow between CCAs.

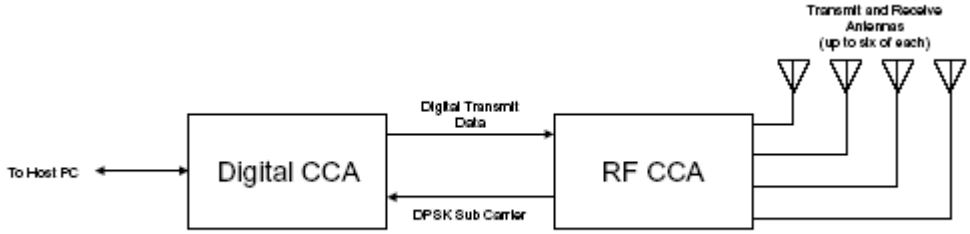


Figure 1: Interrogator Circuit Card Assemblies

3.1 Digital CCA

The digital CCA functionality may be logically divided into two sections; a control section and a data demodulation section.

[2] The protocol calls for a 16-bit CRC that will be implemented on future products.

Figure 2 illustrates a functional block diagram of the control section of the digital CCA. The interrogator uses an industry standard RS-232, RS-422, or RS-485 port to communicate with a host system. The control section provides all of the digital logic required to coordinate sending and receiving a tag message. The control section transmits data from a RAM buffer, converts the data to serial data, and encodes it. The control section then waits for data from the tag, converts it to bytes, and stores it in a RAM buffer. Messages consist of up to 64 bytes of user data.

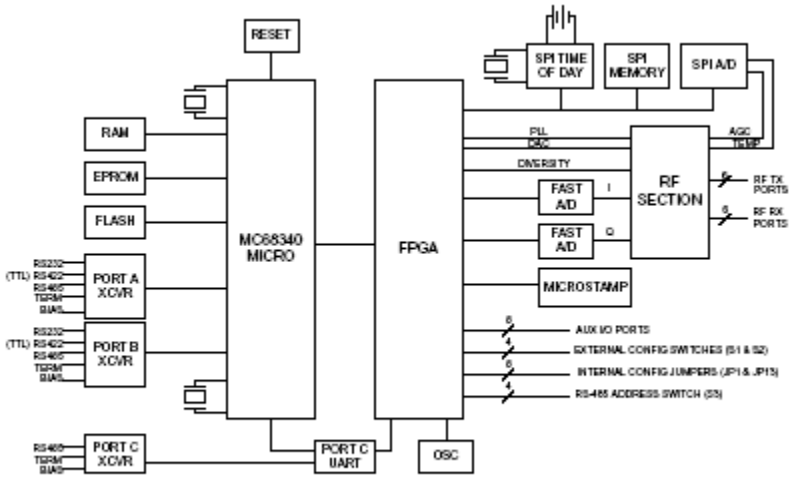


Figure 2: 4100 Interrogator Functional Block Diagram

Figure 3 shows a functional block diagram of the DPSK section. The DPSK section receives an I and Q signal, containing the DPSK modulated subcarrier, from the RF CCA. The I and Q signals are converted from analog to digital signals. The signals are then combined and sent to the DPSK demodulator. The data, clock, and a lock detect signal are then sent to the control section.

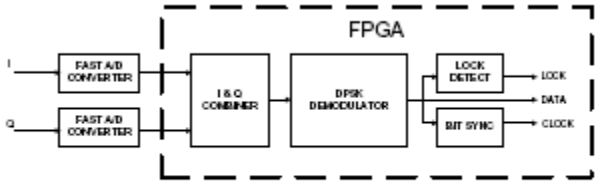


Figure 3: 4100 Interrogator Block Diagram

3.2 Radio Frequency CCA

The radio frequency (RF) CCA interfaces with the external transmit and receive antennas. The RF CCA performs three main functions:

- it modulates the data for transmission to a tag,
- it provides a continuous wave (CW) carrier for the tag backscatter, and
- it receives the backscatter signal from the tag.

A synthesizer is built onto the CCA to tune the RF CW carrier for frequency hopping and band selection. Figure 4 shows a functional block diagram of the RF CCA. The transmitter receives data from the Digital CCA. This data is low-pass filtered and then amplitude modulated (AM) onto a carrier using a mixer. The signal is then amplified by one of two power amplifiers (PA) and sent to the output select switch for transmission through one of six antennas. During CW transmission for backscatter mode, the mixer is biased to the on state. When the transmitter is in CW mode, the tag backscatters the signal with a DPSK modulated sub carrier. This signal is received via one of the six antennas and is amplified by a low noise amplifier (LNA). The signal is coherently downconverted using a quadrature downconverter. The amplitude of the signals are then set using automatic gain controls (AGCs). The I and Q signals, which contain the DPSK modulated subcarrier, are then passed to the DPSK CCA for demodulation.

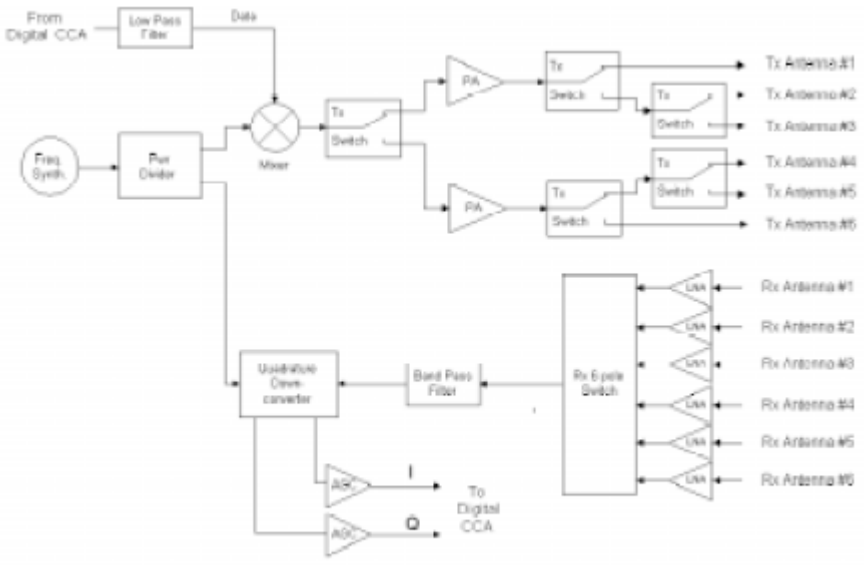


Figure 4: Interrogator RF Circuit Card Assembly Block Diagram

4. INTERROGATOR COMMUNICATION INTERFACE MODES

The embedded interrogator digital card has several options for interfacing with a host computer.

There are three UARTs. For discussion, the UARTs will be labeled Port A, B, and C. Ports A and B are configurable with drivers for RS-232, RS-422, RS-485, or TTL levels (RS-232 and RS-485 only). Port C is fixed as an RS-485 port. All of the serial ports are fully configurable without removing the cover. The switches on the interrogator are used to select the Port A mode and the termination and bias values for all of the ports. Software is used to configure the baud rate, parity, start and stop bits, handshaking, and the Port B mode. All UART lines are brought to the single 37-pin D-Sub connector. Power (+8 volts @ 2 amps and -8 volts @ -0.5 amps) is also brought in through the 37-pin D-Sub connector.

4.1 RS-232 Mode

I/O levels are generated using 5 volt buffers that generate RS-232 signal levels for the output drivers. RTS and CTS lines are available at the same drive levels to provide hardware handshakes, if necessary.

4.2 RS-422 Mode

This interface can be used in systems up to 4000 feet apart. RS-422 is used in systems that have one host and one interrogator. The outputs are 0 to 5 volts differential. There is a dedicated pair of wires for each direction of transmission. To operate at 4000 feet, shielded twisted-pair cables with individual shields, with a 120 ohm impedance properly terminated into 120 ohms is required. CTS and RTS lines are not available in this configuration.

4.3 RS-485 Mode

This configuration allows multiple interrogators to be connected with one cable. The signals are 0 to 5 volts differential. There is only one pair of wires in a standard RS-485 cable. Transmission and reception occur on the same pair in a time-multiplexed mode. The maximum specified distance is 4000 feet as in the RS-422 case. To operate at 4000 feet, shielded twisted-pair cables with a 120 ohm impedance, properly terminated into 120 ohms is required. The host (or the interrogators) only drive the cable when necessary. Because of this, there are times when the cable is not being driven, but must maintain a defined state. This is accomplished by biasing the lines with resistors to a defined state as illustrated in Figure 5. The biasing should only be added on one host or interrogator.

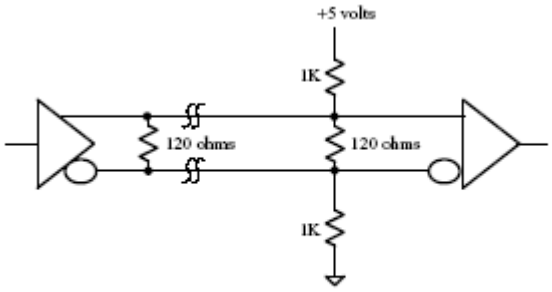


Figure 5: RS-485 Biasing

All three serial ports have provisions for enabling the bias resistors.

4.4 TTL Mode

A TTL serial mode is also available. This mode (referred to as TTL level RS-232) is obtained by using one side of the RS-422 differential driver. The non-inverting output is used as a TTL level signal for output. On the receive side, the non-inverting input is used. The inverting input on the receive side is biased at 1.7 volts (a reasonable TTL level threshold). The inverting input on the receive side must be left floating to maintain this bias. It is recommended that no wiring be placed on this pin when this mode is used. RTS and CTS lines are not available in this mode.

5. INTERROGATOR DETAILED CONFIGURATION

The switches on the back of the chassis are labeled SW1 through SW10 (left to right). The boot software interprets switches SW1 through SW3 and initialized the hardware appropriately. The MSL libraries may impose some restrictions on these. Switches SW4 through SW10 control hardware directly, and have a fixed interpretation.

Figure 6: Switch Layout

Determine boot baudrate for MceMon	Autoexecute FLASH application	Xilinx Configuration File Selection	Undefined	0 - 15 RS-485 Address	Port C Bias LO (RS-485)	Port C Bias HI (RS-485)	Port C Termination (RS-485)	Port A RS-422 Mode	Port A RS-232 Mode	Port A RS-485 Mode	Port A Bias LO (RS-485)	Port A Bias HI (RS-485)	Port A Termination (RS-485 / RS-422 Transmit)	Port A Termination (RS-422 Receive)	Port B Bias LO (RS-485)	Port B Bias HI (RS-485)	Port B Termination (RS-485 / RS-422 Transmit)	Port B Termination (RS-422 Receive)	
S1		S2		S3	S4		S5		S6		S7		S8		S9		S10		
L	R	L	R	Rotary	L	R	L	R	L	R	L	R	L	R	L	R	L	R	
U																			Port A: 9600 Baud (No Parity, 8 Data Bits, 2 Stop Bits)
D																			Port A configured from JP1 and JP13 settings
	U																		Boot application from EPROM
	D																		Boot application from FLASH
		U																	Configure FPGA from EPROM
		D																	Configure FPGA from FLASH
																			Undefined
								U	D	U									Port A: Use RS-232 hw driver
								D	U	U	U	U	U	U					Port A: Use Serial TTL level drivers
								D	U	U	U	U	D	D					Port A: Use RS-422 hw driver with XMT & RCV bus termination
				#				U	U	D	U	U	U						Port A: Use RS-485 hw driver
				#				U	U	D	D	D	U						Port A: Use RS-485 hw driver with bus bias
				#				U	U	D	D	D	D						Port A: Use RS-485 hw driver with bus bias and termination
															U	U	U	U	Port B: Use Serial TTL level drivers[a]
															U	U	D	D	Port B: Use RS-422 hw drivers with XMT & RCV bus termination
				#											U	U	U		Port B: Use RS-485 hw drivers
				#											D	D	U		Port B: Use RS-485 hw drivers with bus bias
				#											D	D	D		Port B: Use RS-485 hw drivers with bus bias and termination
				#	U	U	U												Port C: Use RS-485 hw drivers
				#	D	D	U												Port C: Use RS-485 hw drivers with bus bias
				#	D	D	D												Port C: Use RS-485 hw drivers with bus bias and termination

a. When initializing *SerialPortB* for this mode, the RS-422 driver must be used (DeviceType = RS422_DRIVER).

Table 1 - Switch Definitions and Settings

All non-RF interface connections in 4100 series interrogators are combined on a 37-pin D-style connector located on the back panel. This connector includes the power and ground connections, three serial ports, 8 auxiliary digital input/output ports, and two analog inputs. The following codes are used:

L Switch must be in the left position.
R Switch must be in the right position.
U Switch must be in the up position.
D Switch must be in the down position.
RS-485 mode: each unit on a common bus must have one of the 16 positions (0-15) selected to define its unique address.

PIN #	SIGNAL	DEFINITION
1	---	NOT USED
2	TX232_1	Port A RS-232 Transmit
3	RX232_1	Port A RS-232 Receive
4	RTS_1	Port A Ready-To-Send
5	CTS_1	Port A Clear-To-Send
6	AUX2	Auxiliary I/O Port 2*
7	GND2	Port B Signal Ground (100 ohm series resistance to ground)
8	P422_1	Port A RS-422 Receive HI / TTL Receive
9	GND	Ground
10	P485_1	Port A RS-485 / RS-422 Transmit HI / TTL Transmit
11	M485_1	Port A RS-485 / RS-422 Transmit LO
12	M485_2	Port B RS-485 / RS-422 Transmit LO
13	M485_3	Port C RS-485 LO
14	AUX4	Auxiliary I/O Port 6*
15	AUX6	Auxiliary I/O Port 4*
16	CTS_2	Port B Clear-To-Send
17	TX232_2	Port B RS-232 Transmit
18	EXTAN0	External Analog Input 0 (0 to +5 volts)
19	DCDCVDC	DC-to-DC Converter Input (Reserved)
20	---	NOT USED
21	AUX0	Auxiliary I/O Port 0*
22	M422_2	Port B RS-422 Receive LO
23	M422_1	Port A RS-422 Receive LO
24	AUX1	Auxiliary I/O Port 1*
25	AUX3	Auxiliary I/O Port 3*
26	P422_2	Port B RS-422 Receive HI
27	POSVDC	Positive Power Input (+8VDC to +9VDC)
28	NEGVDC	Negative Power Input (-8VDC to -9VDC)
29	P485_2	Port B RS-485 / RS-422 Transmit HI / TTL Transmit
30	GND1	Port A Signal Ground (100 ohm series resistance to ground)
31	P485_3	Port C RS-485 HI
32	GND	Ground
33	AUX5	Auxiliary I/O Port 5*
34	AUX7	Auxiliary I/O Port 7*
35	RX232_2	Port B RS-232 Receive
36	RTS_2	Port B Ready-To-Send
37	EXTAN1	External Analog Input 1 (0 to +5 volts)

Table 2 - 37-pin D-Sub Connector Pin Assignments

* The logic device in the interrogator is supplied from 3.3 volts. It is 5 volt compliant on input but does not source more than 3.3 volts. External logic should use TTL thresholds.

Auxilary Line Output Specifications	
Voltage	**Current**
≥ 3.0 V	0.5mA source
≥ 2.4 V	4.0 mA source
≤ 0.3 V	1.5mA sink
≤ 0.4 V	12.0mA sink

Auxilary Line Input Specifications	
Low Input	0 to 1.25 V
High Input	1.25 to 5 V

Table 3 - Auxilary Line Input - Output Port Specifications

6. IDmicro 4120 RF INTERROGATOR SPECIFICATIONS

Microprocessor
Motorola MC68340

Memory (Bytes)
Flash: 1 MB - contents upgradeable from field
EPROM: 128 KB - socket accepts devices to 512 KB
SRAM: 1 MB no-wait state static RAM (a small portion of this memory is used by the system)

Physical Dimensions
10.7 x 17.0 x 16.6 cm

Operating Temperature
-40 to +85 °C

Humidity
95% non-condensing (preliminary)

Vibration
7 Grms all axes

Shock
Operates properly after 3-foot drop onto concrete (shipping caps installed on RF connections).

Power Requirements
VDC: +8.0 to +9.0 VDC at 2.0 Amps (typical)
-8.0 to -9.0 VDC at 0.5 Amps (typical)
85/260 VAC UL approved Power Supply available. (-40 to +85 °C operation)

RF Output Power (max)
TX1, TX6: 28.0 dBm ± 2 dB @ 25 °C
TX2, TX3, TX4, TX5: 27.0 dBm ± 2 dB @ 25 °C
Over -40 to +85 °C all tolerances increase to ± 3 dB
Programmable in 1 dB steps down to +5 dBm (6 dB gain (or less) antenna required for operation)

RF Ports (TNC socket)
Option 1: • 2 RF Transmit Ports
• 2 RF Receive Ports
Option 2: • 6 RF Transmit Ports
• 2 RF Receive Ports
Option 3: • 6 RF Transmit Ports
• 4 RF Receive Ports

Option 4: • 6 RF Transmit Ports
• 6 RF Receive Ports
RF Port Isolation:
Between TX1, TX2, TX3 10 dB (min)
Between TX4, TX5, TX6 10 dB (min)
Between TX1-3 and TX4-6 30 dB (min)
All RX ports 20 dB (min)
Receive Sensitivity:
-90 dBm @ 25 °C

System Interfaces
1. 2 serial ports for use with RS-232, RS-422, RS-485, or TTL line drivers
2. 1 serial port for use with RS-485 mode only
3. 8 TTL-compatible auxiliary control lines for application use
4. 5 LEDs: 2 available for user control, 2 provide unit status, 1 indicates power on
5. 2 analog-to-digital converter input ports (0-5 volts)

Interface Connector
37-pin filtered D-sub miniature connector (pins on unit)

Application Development
Custom software must be programmed for embedded applications.
The IDmicro RIC Development Kit includes:
• MsAssist.exe, an application program designed to aid the user in gaining familiarity with RIC functions and commands,
• Software Library (MSL) (available for RFID-related tasks),
• example programs,
• 4100 utility library with source code (available for MC68340 related tasks), and
• developer's web-based training program.

Safety Certification
U.S.A. UL1950; Canada, CUL 1950/CSA-C22.2; Europe CE Mark (EN60950)

Regulatory Certification
FCC Certification (Part 15), Industry Canada Certification, *privat* Cetecom (tested per I-ETS 300 440). FCC approval is contingent on the use of specific antennas. Contact IDmicro, Inc. for information on approved antennas and cables. Professional installation of this product is required.