

The diagram illustrates the internal architecture of the LPS (Low Power System) with the following components and connections:

- Power Management:** 12V DC input to a Regulator, which outputs 3.3V DC and 5.0V DC. The 5.0V DC is connected to the Inverter Control, which in turn controls the Inverter I/F.
- Video Input Path:**
  - Graphic Card input to DDC ROM, which connects to the Scaler (Micom).
  - Red, Green, Blue, and Sync inputs to an 8bitx3 ADC, which connects to the Scaler (Micom).
  - CVBS and SVHS inputs to a Video decoder, which connects to the Scaler (Micom).
  - A 24.576MHz CLOCK input to the Video decoder.
- Scaler (Micom) Core:**
  - Receives MCKEXT\_122MHz and DCKEXT\_99MHz signals from PLL IC1 and PLL IC2.
  - PLL IC1 and PLL IC2 are clocked by 24.576MHz and 14.31818MHz signals.
  - Outputs to LCD I/F TTL and LCD I/F LVDS, which connect to the P A N E L.
  - Outputs to Debug I/F (RS-232).
  - Connected to NVM (Non-Volatile Memory) and FLASH MEM. via LPS internal usage.
- Control and Interface:**
  - Remote controller input to IR receiver, which connects to the Scaler (Micom).
  - OSD I/F (On-Screen Display Interface) connects to the Scaler (Micom).
- Audio Path:** Audio in input to Volume Controller, which connects to Audio Amplifier, which then connects to Speaker Out.
- Optional Component:** A TV Tuner (option) is shown in a green box, connected to the system.