

MS-6526

Version 300

INTEL (R) Brookdale-G Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-G Chipset:

**INTEL GMCH (North Bridge) +
INTEL ICH4 (South Bridge)**

On Board Chipset:

**BIOS -- FWH
AC'97 Codec -- ALC201A
LPC Super I/O -- W83627HF-AW
Clock Generation -- ICS950218AF
LAN -- Intel 562ET**

Expansion Slots:

PCI2.2 SLOT * 3

Title

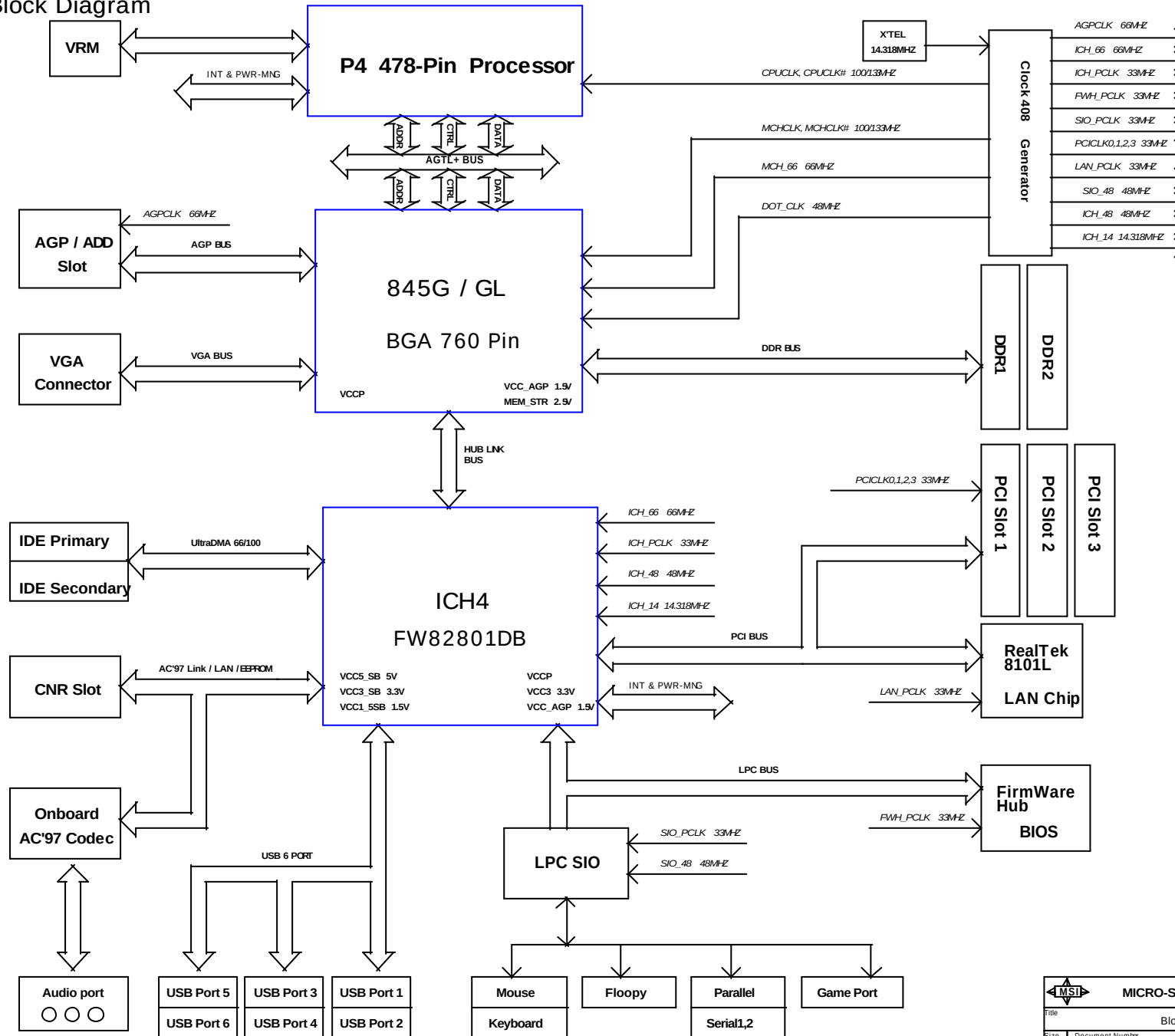
Page

Cover Sheet	1
Block Diagram	2
Voltage Distribution	3
General SPEC	4
Clock ICS950218AF & ATA100 IDE CONNECTORS	5
mPGA478-B INTEL CPU Sockets	6 - 7
INTEL Brookdale-G GMCH -- North Bridge	8-10
INTEL ICH4 -- South Bridge	11-12
LPC I/O -- W83627HF-AW	13
DDR DIMM1&2 and DDR Terminator Resistor	14-15
AGP Slot	16
VGA Connector	17
PCI SLOT 1 & 2 & 3	18
FWH & CNR	19
USB Connectors	20
AC'97 Codec ALC201A & Connectors	21-22
IO Connectors	23
FAN & 1.5V Voltage Regulator	24
W83302D ACPI Controller	25
VRM9.9 -- CPU Power	26
Front Panel & ATX Connectors	27
RealTek 8101L PCI Lan / MC97 Controller	28
Manual Parts	29

MODEL Config.	ORCAD Config.	Function	ERP Number
MS6526 STD	cfg6526-STD	STD	601-6526-08S
MS6526 Option:L	cfg6526-LAN	STD+Intel LAN	601-6526-09S
MS6526M1 STD	cfg6526M1-STD	STD+M1	
MS6526M1 Option:L	cfg6526M1-LAN	STD+M1+Intel LAN	

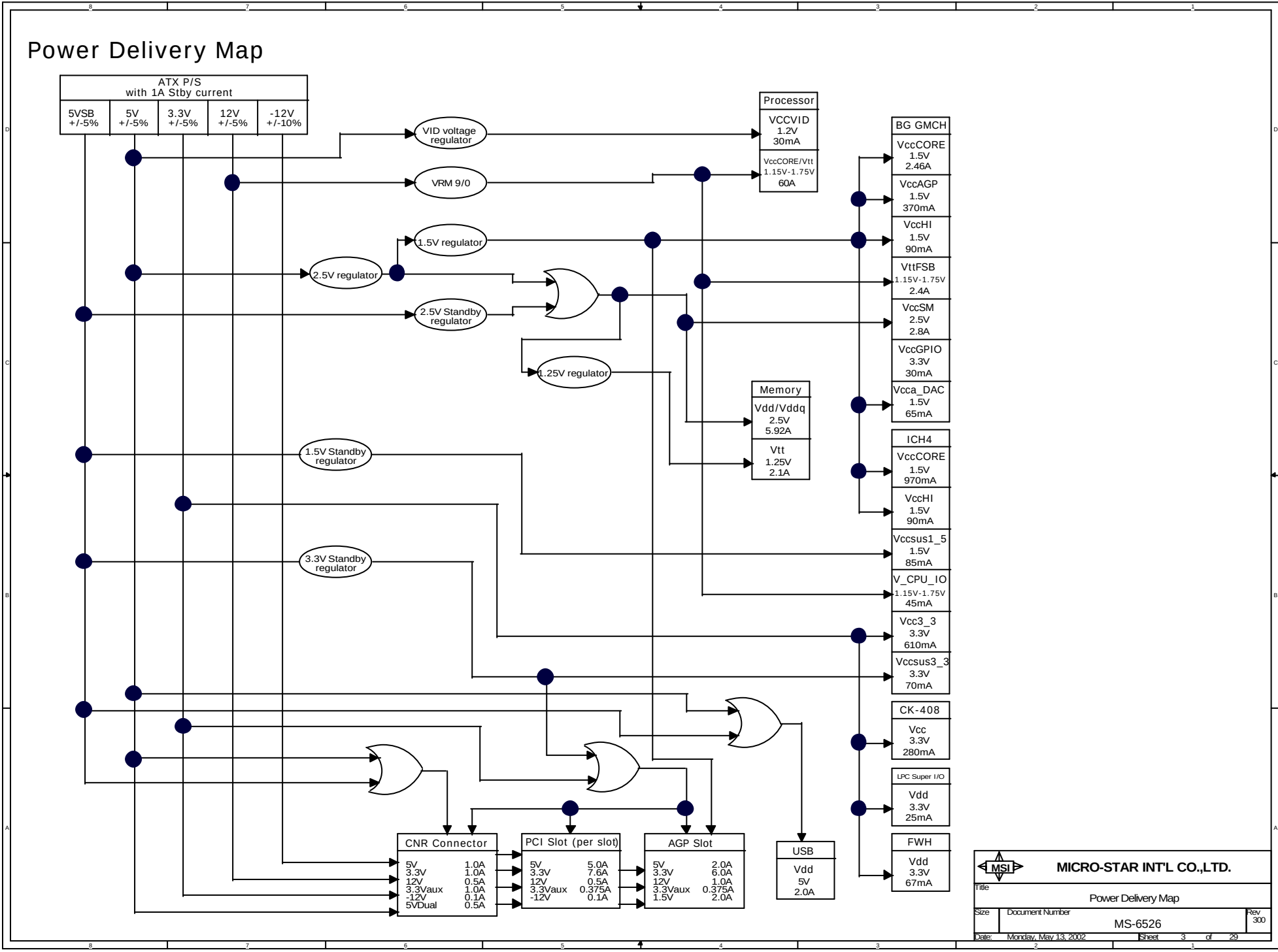
		MICRO-STAR INT'L CO.,LTD.	
Title		Cover Sheet	
Size	Document Number	MS-6526	
Date: Monday, May 13, 2002		Sheet	1 of 29

Block Diagram



MICRO-STAR INT'L CO.,LTD.		
File Block Diagram		
Size	Document Number	Rev. 300
MS-6526		
Date	Monday, May 13, 2002	Sheet 2 of 29

Power Delivery Map



General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntn pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2	12 (PCI5)
PCI LAN	INTG# INTF#	AD29	LAN_PCLK	17 (PCI9)

* ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK 0# DCLK1/DCLK 1# DCLK2/DCLK 2#
DIMM 2	1010001B	DCLK3/DCLK 3# DCLK4/DCLK 4# DCLK5/DCLK 5#

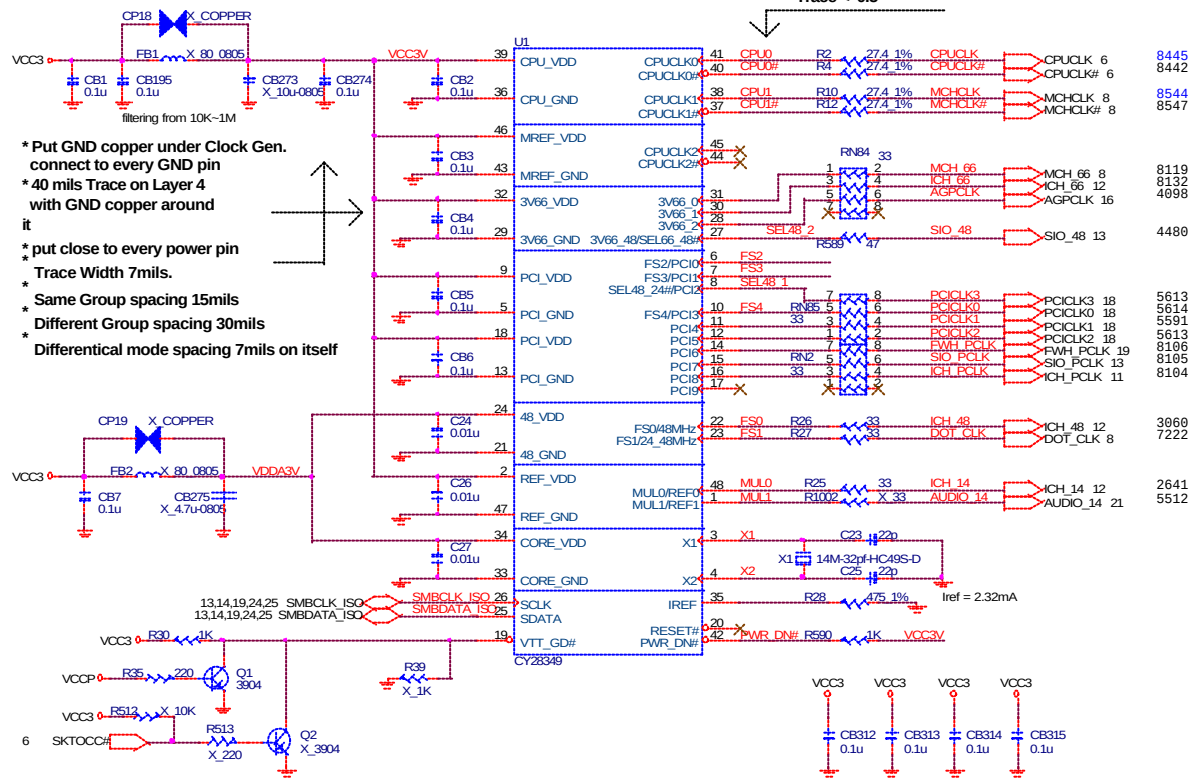


MICRO-STAR INT'L CO.,LTD.

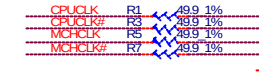
Title General SPEC			
Size	Document Number	MS-6526	Rev 300
Date:	Monday, May 13, 2002	Sheet	4 of 29

CLOCK GENERATOR BLOCK

*Trace < 0.5"



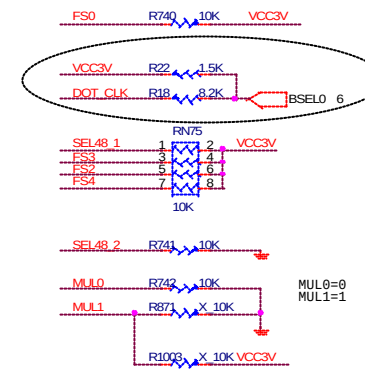
Shut Source Termination Resistors



Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS

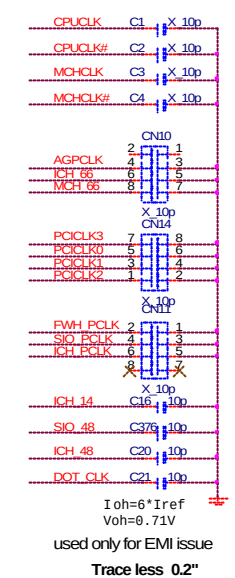


FS4 FS3 FS2 FS1 FS0 FSB (MHz)

1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz



Pull-Down Capacitors

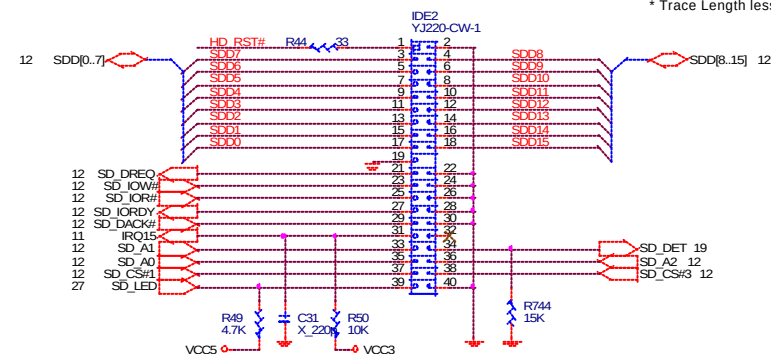
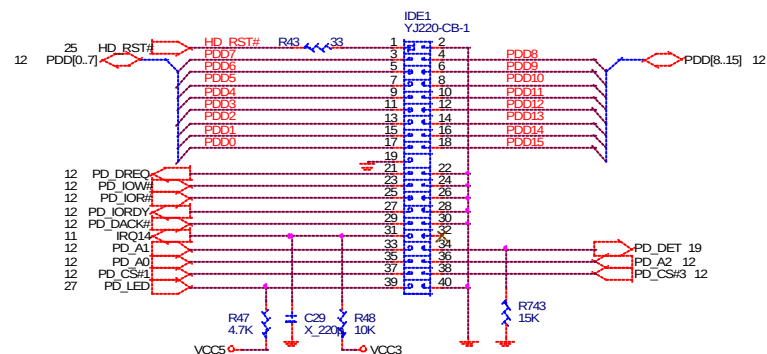


PRIMARY IDE BLOCK

ATA100 IDE CONNECTORS

SECONDARY IDE BLOCK

- * Trace Width : 5mils
- * Trace Spacing : 7mils
- * Length(longest)-Length(shortest)<0.5"
- * Trace Length less than 5"



MICRO-STAR INT'L CO.,LTD.

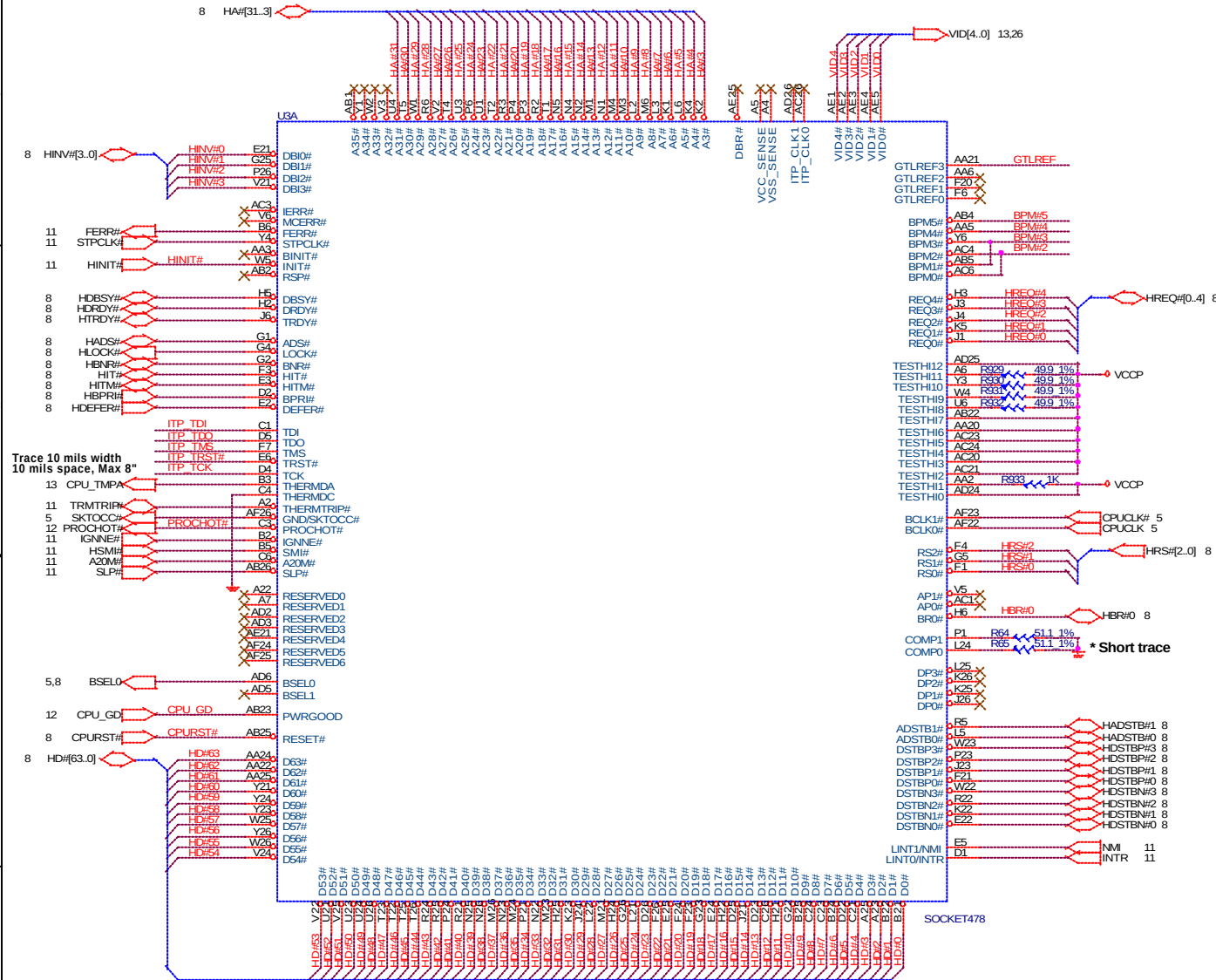
Title	Clock Gen & ATA100 IDE Connectors
-------	-----------------------------------

Size	Document Number	Rev
------	-----------------	-----

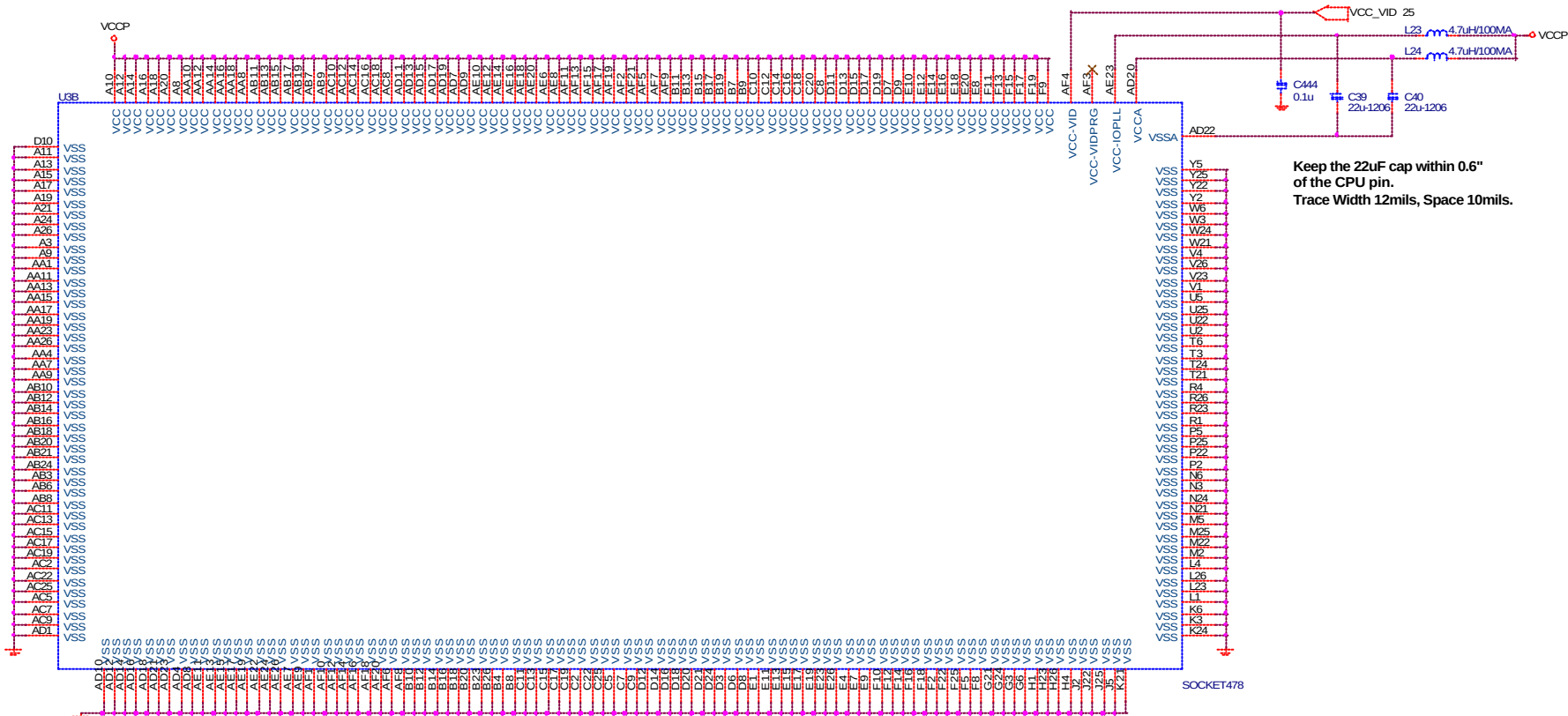
MS-6526 300

Date: Monday, May 13, 2002 Sheet 5 of 29

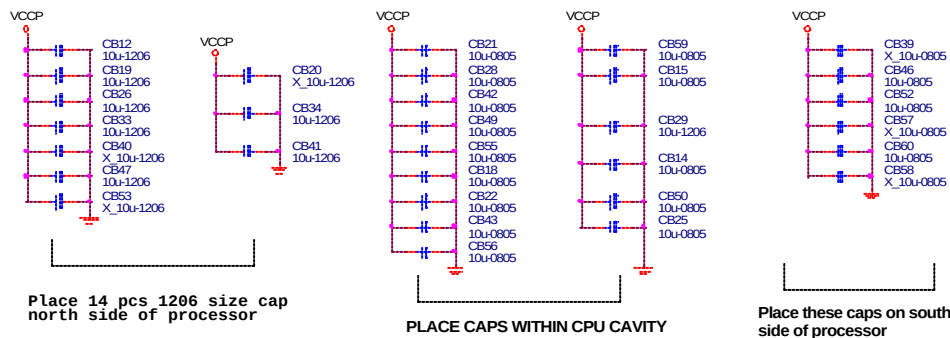
CPU SIGNAL BLOCK



CPU VOLTAGE BLOCK

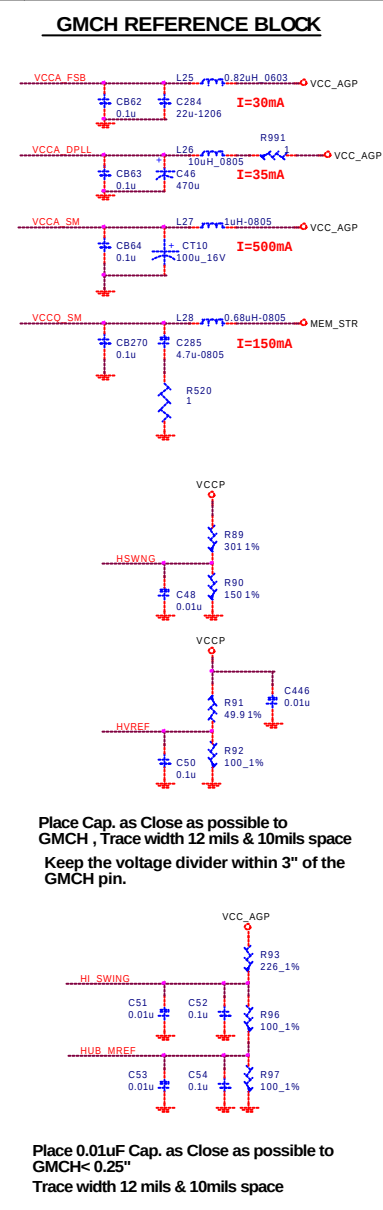
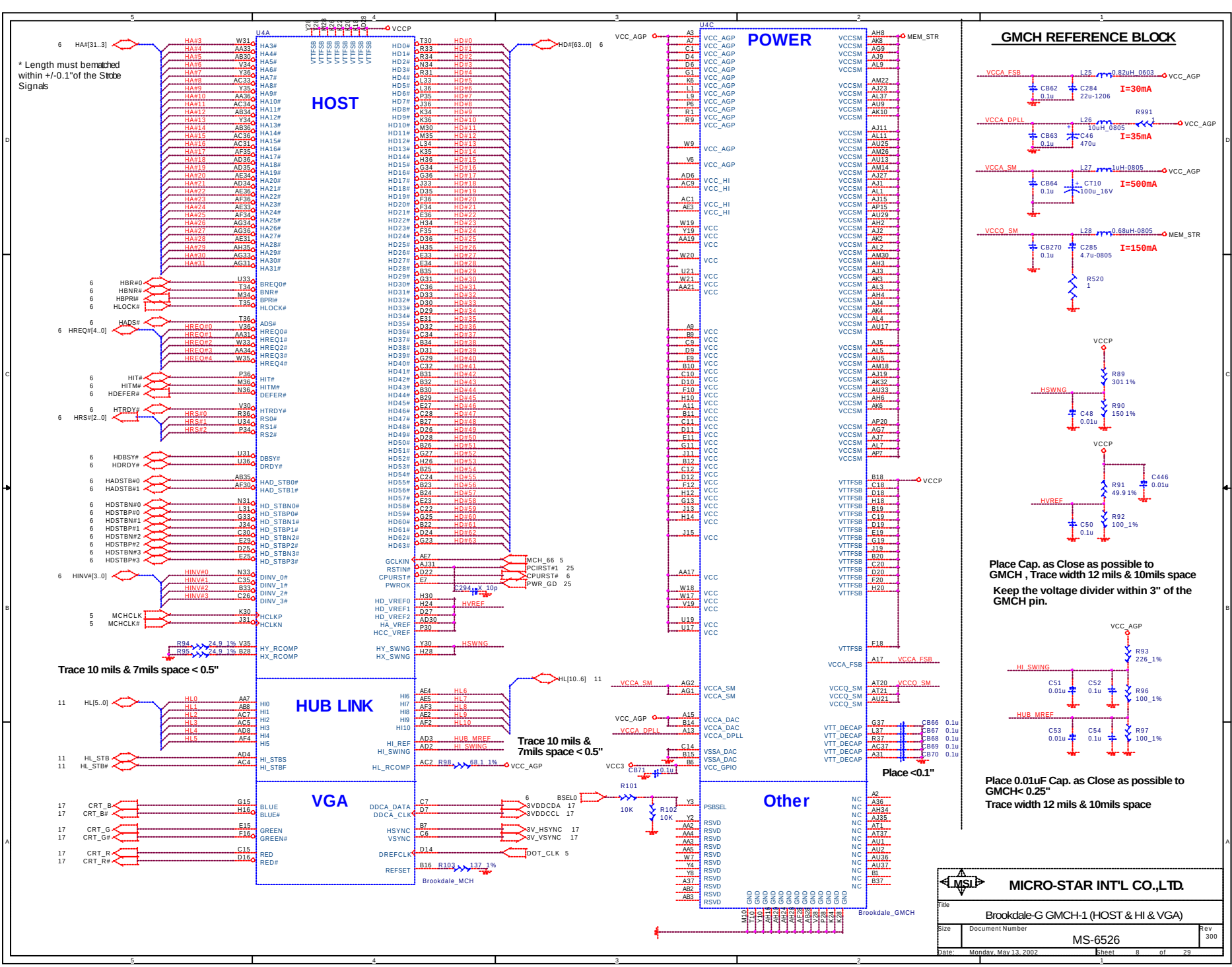


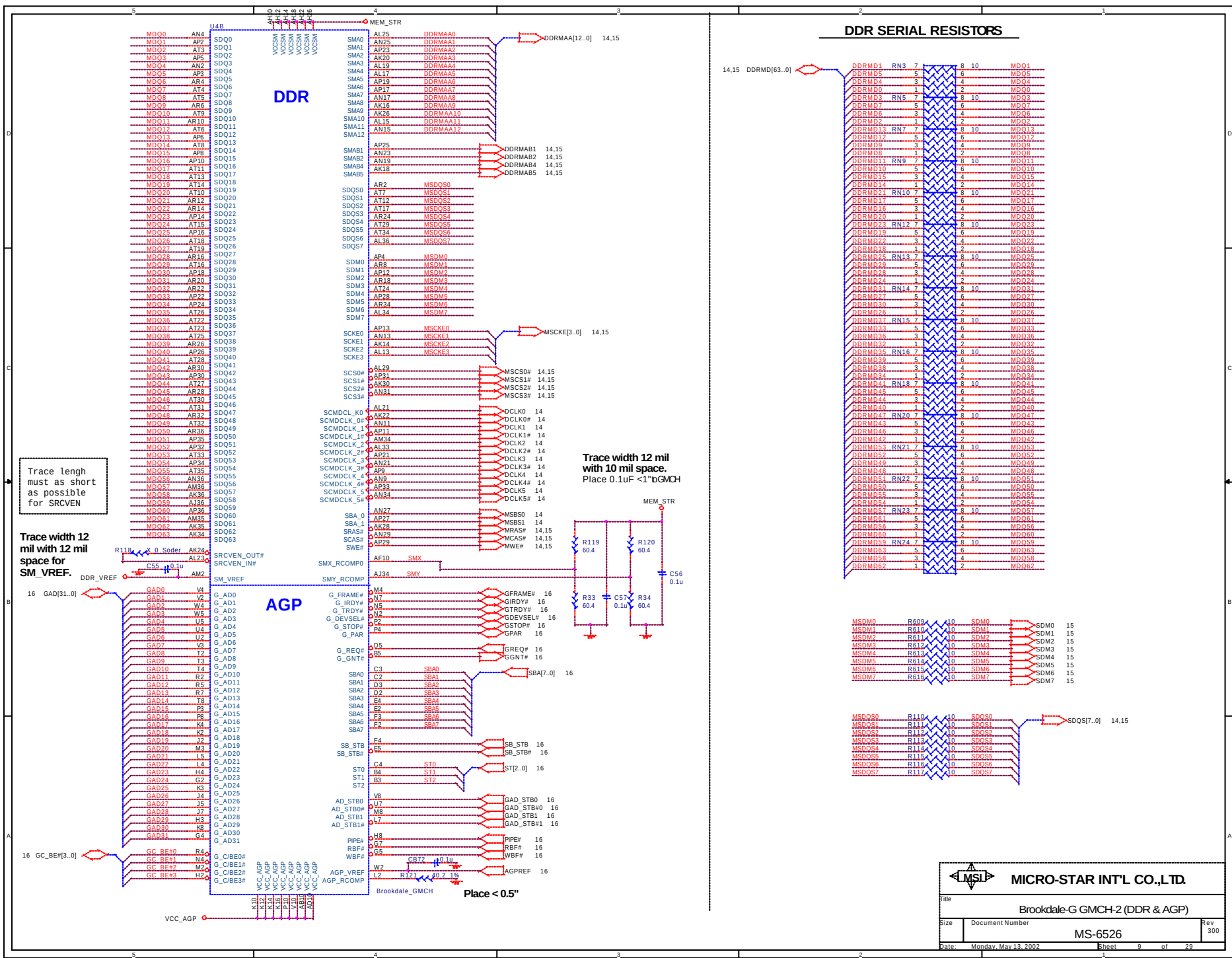
CPU DECOUPLING CAPACITORS

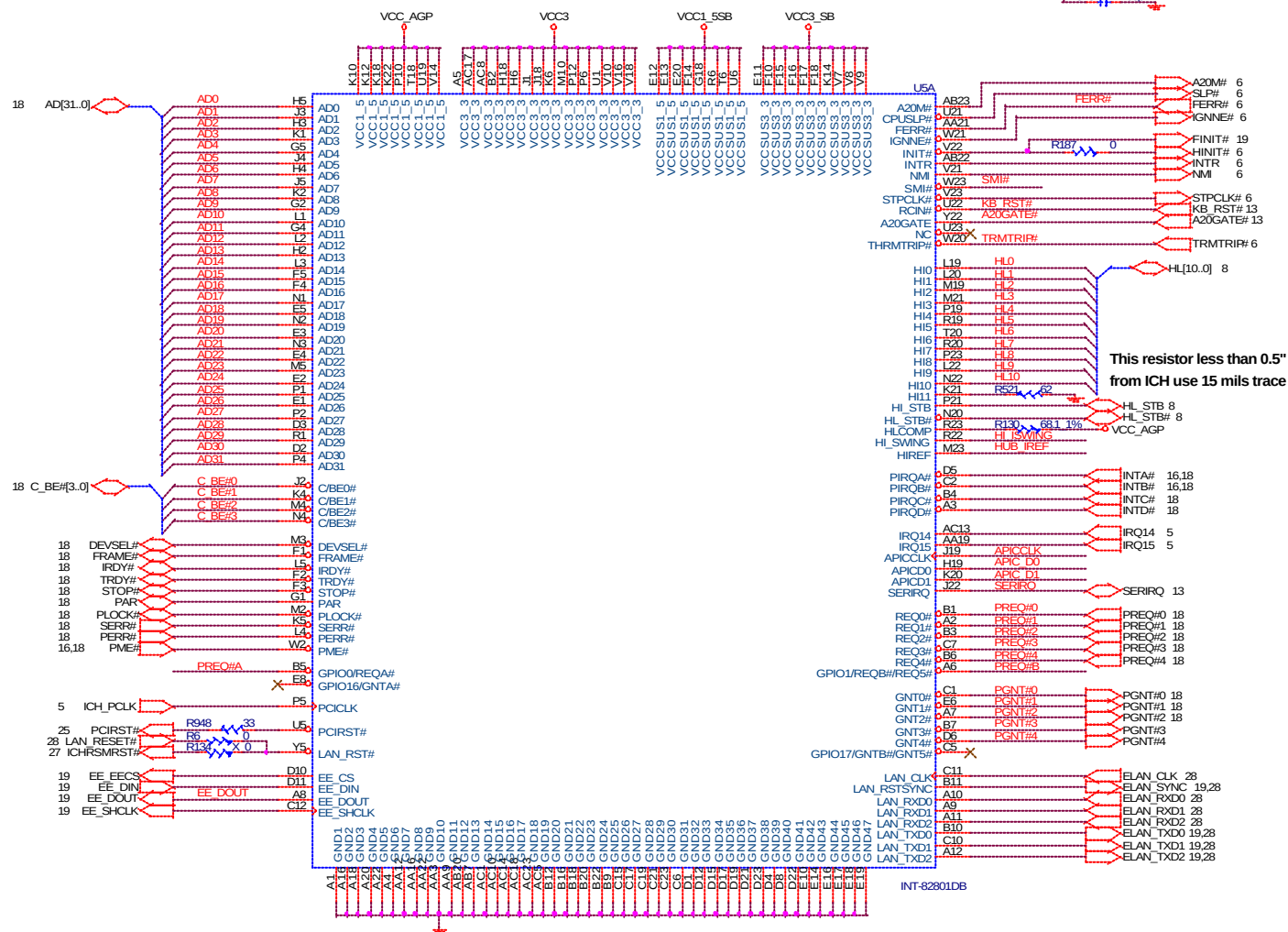


Within CPU Cavity Solder Side

MICRO-STAR INT'L CO.,LTD.			
Title mPGA478-B INTEL CPU Part2			
Size	Document Number	MS-6526	Rev 300
Date: Monday, May 13, 2002	Sheet	7	of 29

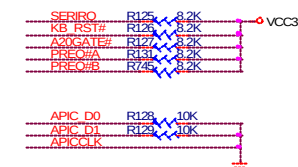






EE_DOUT R133 X_10K

Reserved pull-down resistor for ICH4 reserved function straps.



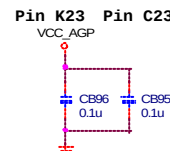
Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

Pin A1 Pin H1 Pin AC10

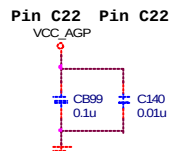
VOC3

Pin A4 Pin T1 Pin AC18

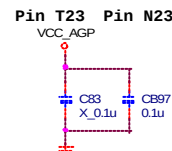
CB102 0.1u CB103 0.1u CB104 0.1u CB105 0.1u CB106 0.1u CB107 0.1u



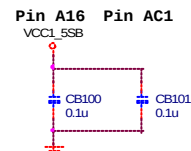
FOR Core Logic



FOR PLL



FOR Hub Interface

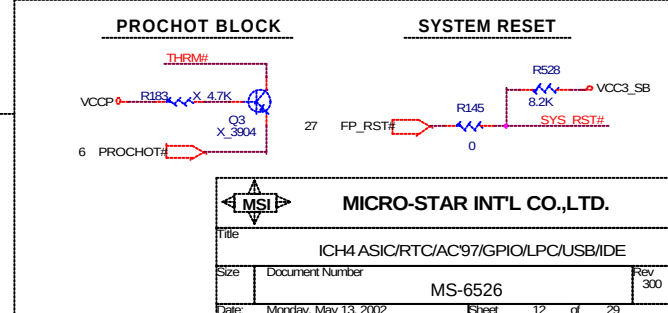
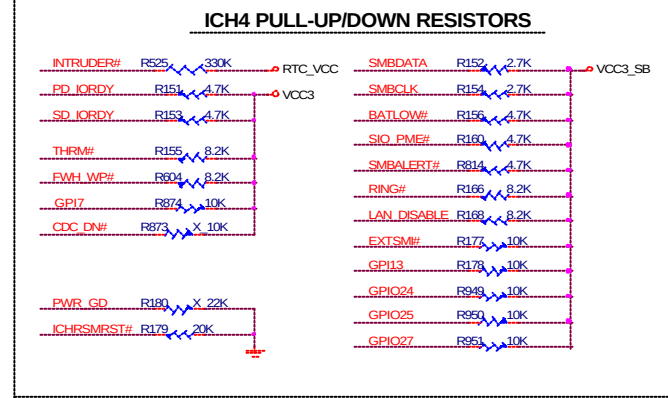
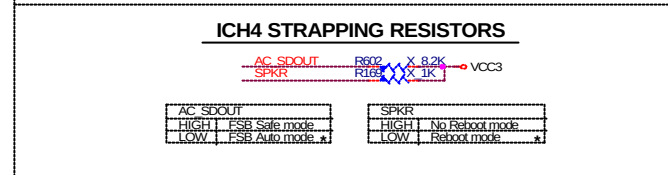
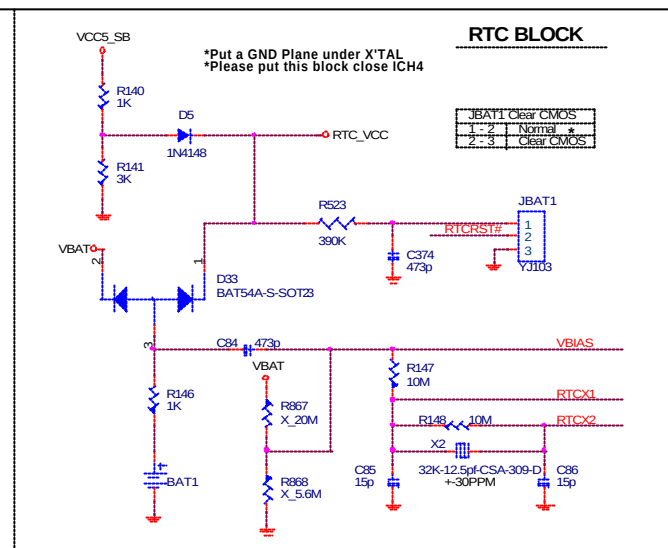
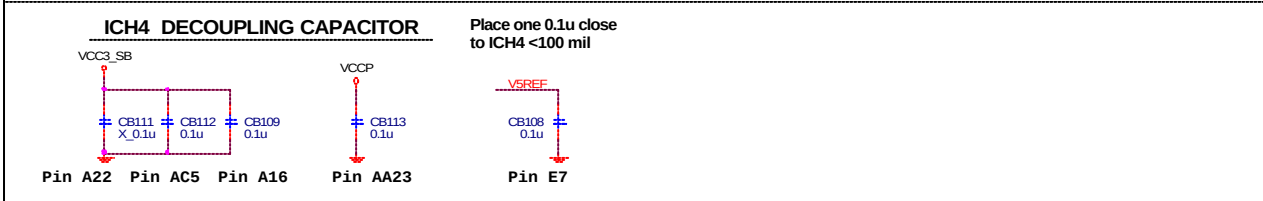
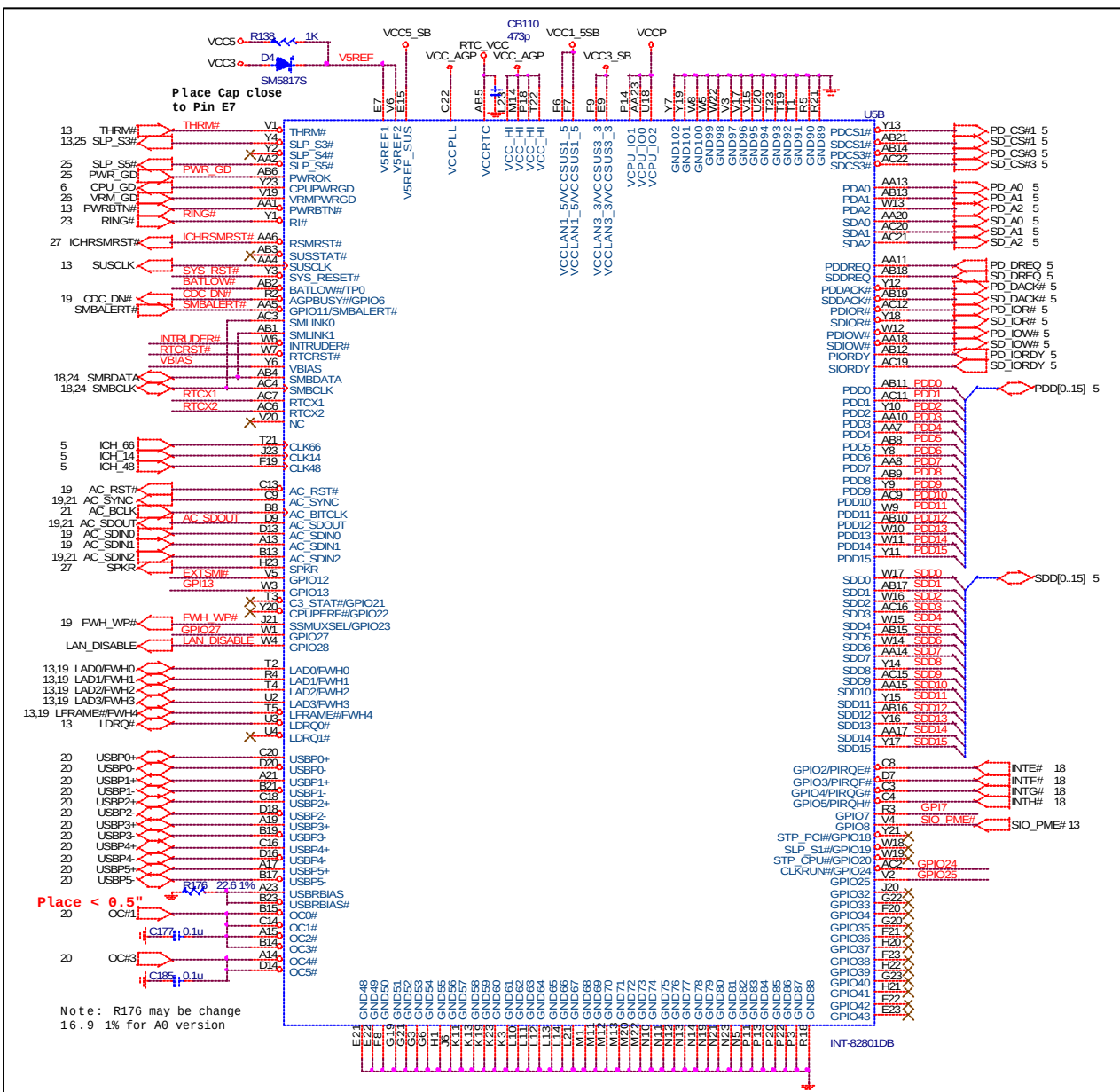


MICRO-STAR INT'L CO.,LTD.

ICH4 PCI & HI & LAN

Size	Document Number	Rev
	MS-6526	300
Date:	Monday, May 13, 2002	Sheet 11 of 29

Date: Monday, May 13, 2002 Sheet 11 of 29



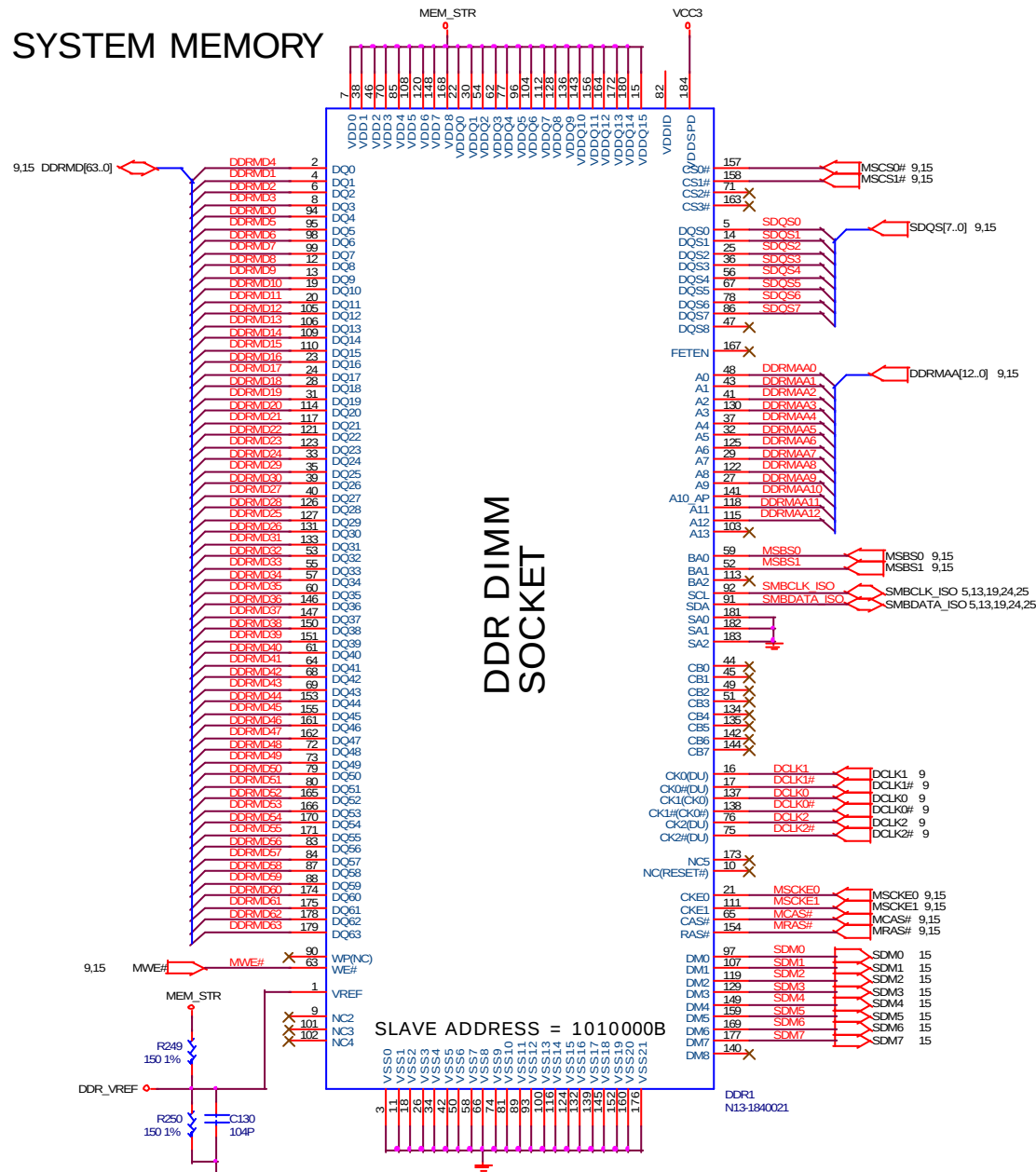
18



DTRA#	L: PNP Default	H: PNP no Default
-------	----------------	-------------------

Date: Monday, May 13, 2002 Sheet 13 of 29

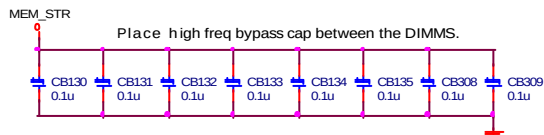
SYSTEM MEMORY



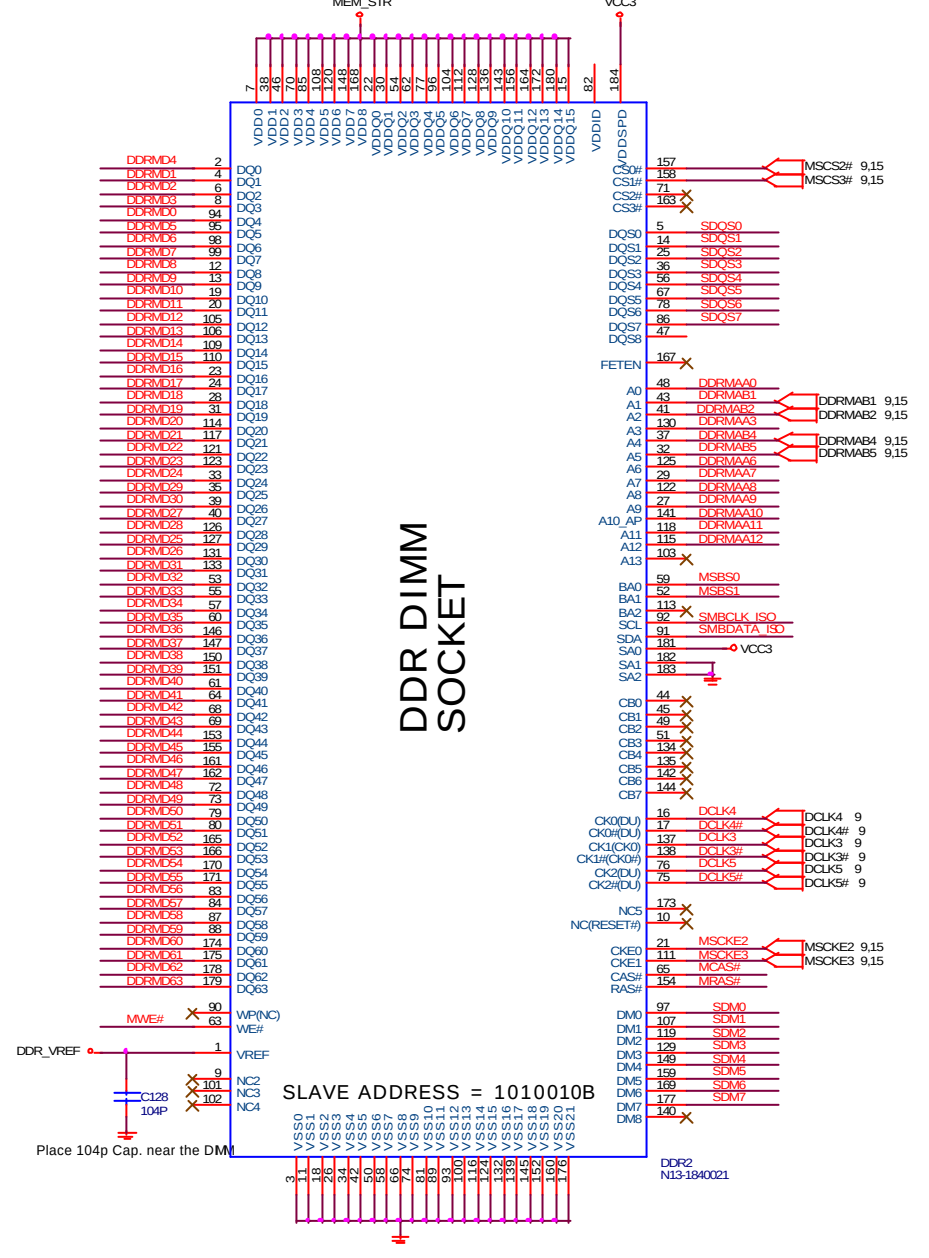
DDR DIMM
SOCKET

SLAVE ADDRESS = 1010000B

Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DMM



Place high freq bypass cap between the DIMMS.



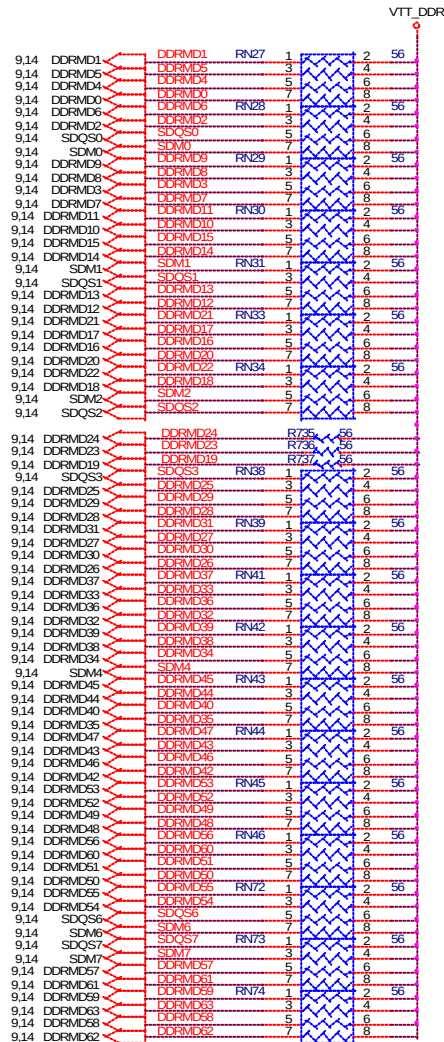
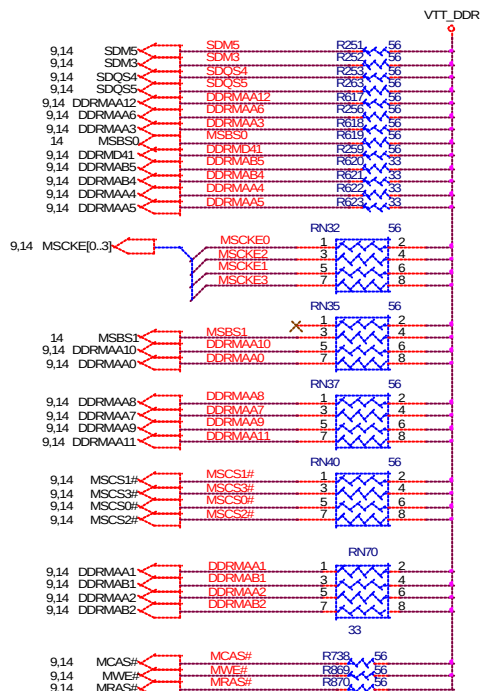
DDR DIMM
SOCKET

SLAVE ADDRESS = 1010010B

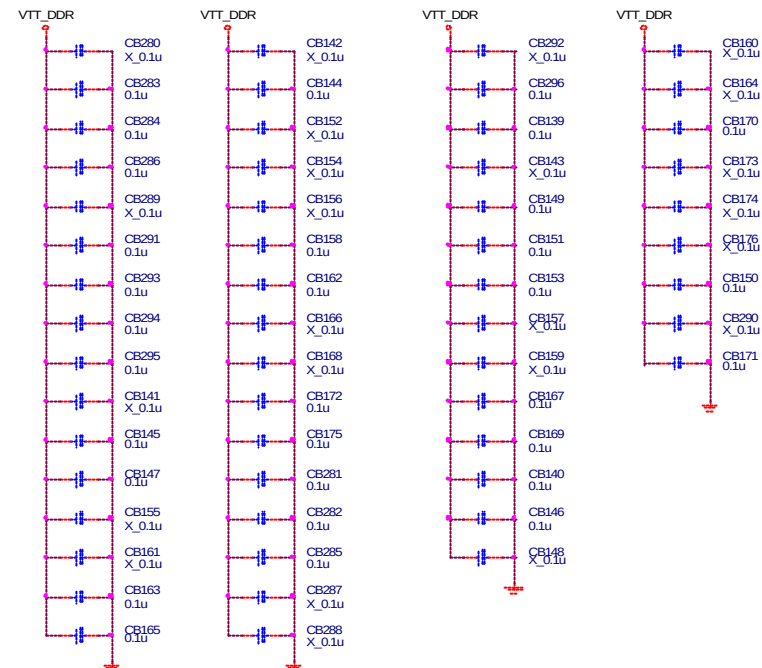
Place 104p Cap. near the DMM

MICRO-STAR INT'L CO.,LTD.			
Title: DDR DIMM1&2			
Size	Document Number	Rev 300	
MS-6526			
Date: Monday, May 13, 2002	Sheet 14	of 29	

DDR TERMINATORS

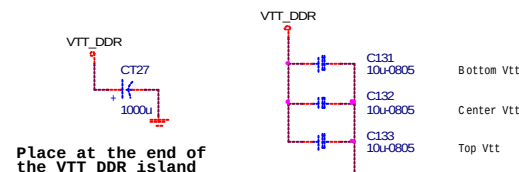


DDR Decoupling Caps



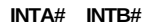
Total 110 signal, need 55 pcs decoupling.

Place for VTT_DDR island



		MICRO-STAR INT'L CO.,LTD.	
Title: DDR Terminator Resistor			
Size:	Document Number:	Rev: 300	
		MS-6526	
Date:	Monday, May 13, 2002	Sheet:	15 of 29

VCC5 = 60mils trace / 15 mils space



VCC_AGP

R277
1K_1%

AGPREF: 10uA

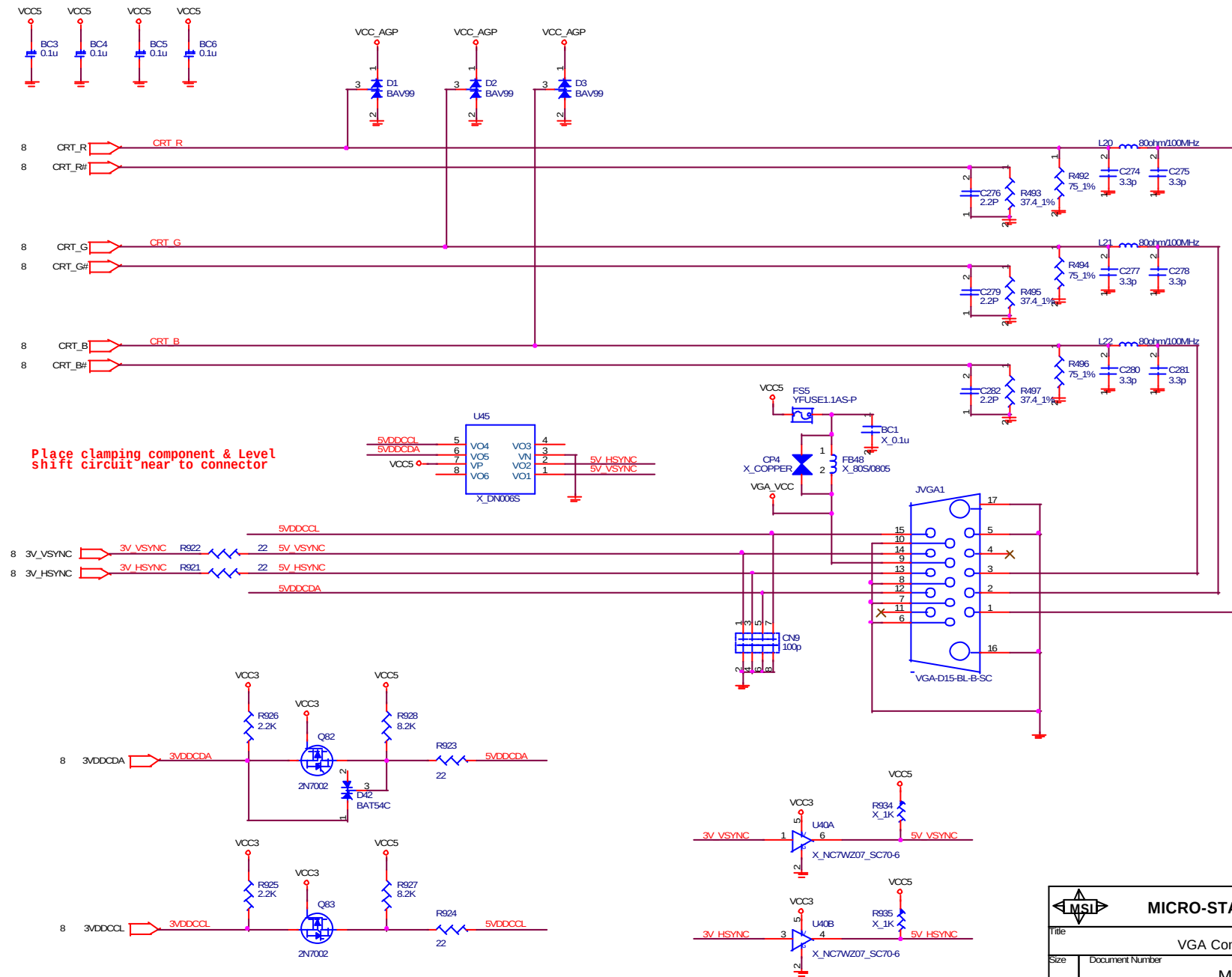
AGPREF

R278
1K_1%

NEAR AGP SLOT

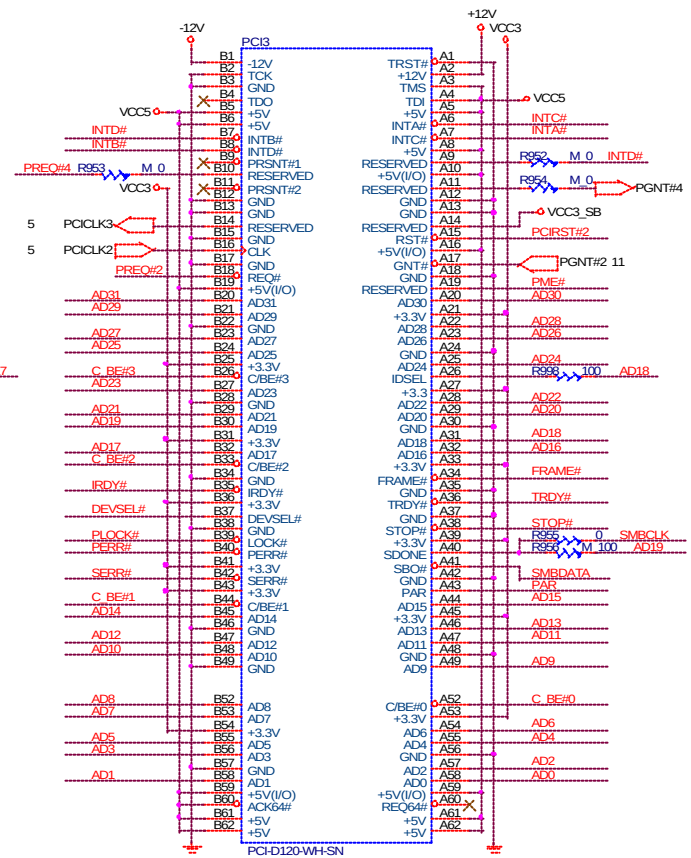
Diagram showing the connection for Pin 10 of the RN91 component. The pin is connected to VCC_AGP. The component is labeled X_10P8R-8.2K.

Video Connector



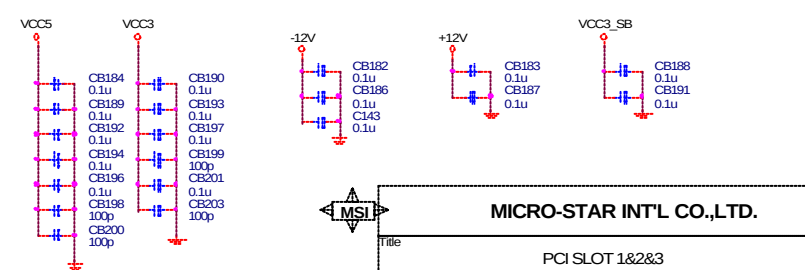
		MICRO-STAR INT'L CO.,LTD.	
Title			
VGA Connector			
Size	Document Number		Rev
	MS-6526		300
Date:	Monday, May 13, 2002	Sheet	17 of 29

PCI SLOT 3 (PCI VER: 2.2 COMPLY)



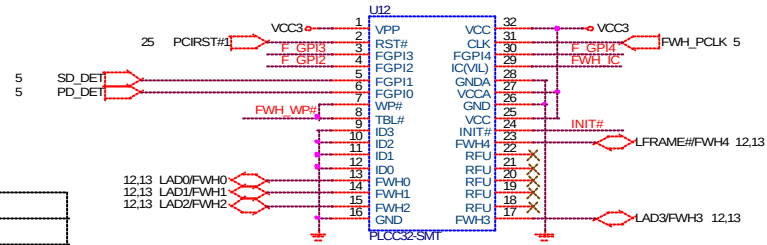
```
IDSEL = AD18
MASTER = PREQ2
INTC#
```

PCI SLOT DECOUPLING CAPACITORS

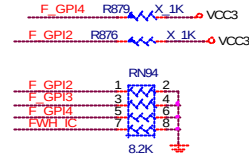


300

Firmware Hub (FWH)



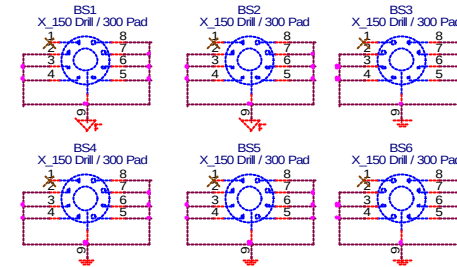
FWH RESISTORS



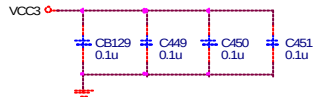
J6 Config.		
1 - 2	Normal	*
2 - 3	Configuration Mode	
OPEN	Recovery	

* Default

PCB Mounting Holes

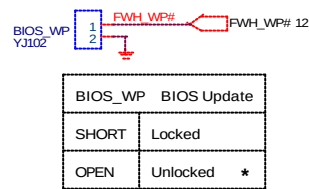


FWH DECOUPLING CAPACITORS



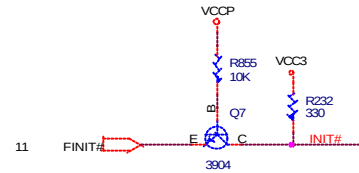
Place Cap. as Close to FWH< 350 mil

FWH write protect

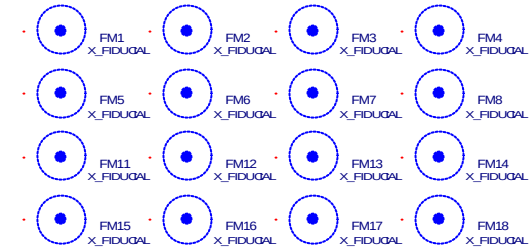


BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block



PCB Fiducials



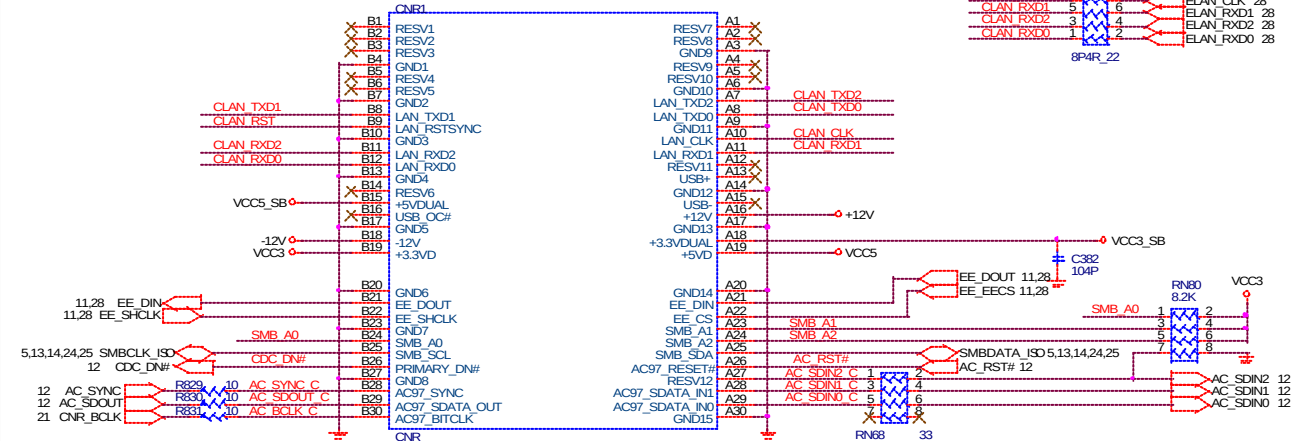
CNR RISER

* LAN Trace width : 5 mils

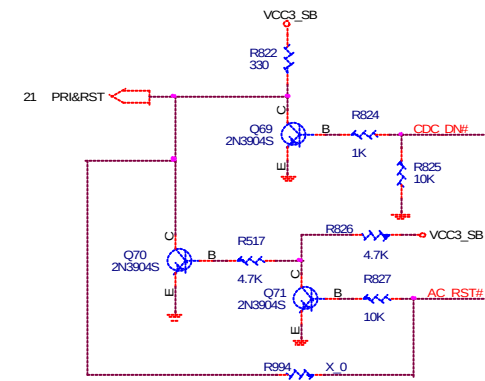
* AC'97 Trace Spacing : 10 mils

* Maxium trace length < 9.5"

* Equal to or up to 500 mils shorter than the ELAN_CLK trace



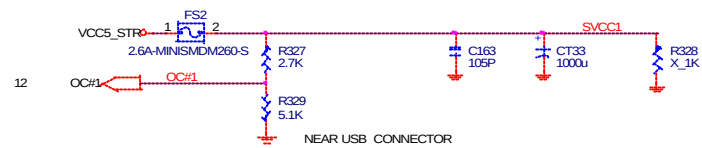
SIMULATION TRACE



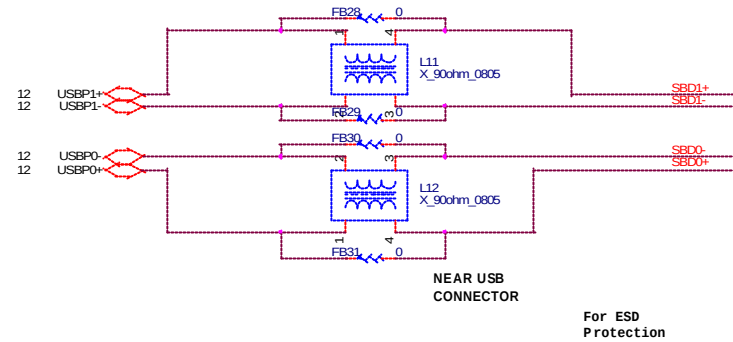
MICRO-STAR INT'L CO.,LTD.

Title		
FWH & CNR		
Size	Document Number	Rev
	MS-6526	300
Date:	Monday, May 13, 2002	Sheet 19 of 29

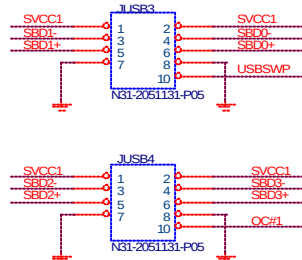
POWER CIRCUIT FOR USB PORT 0,1,2,3



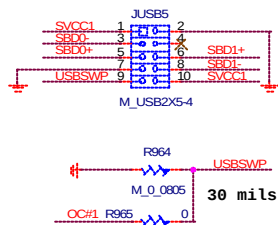
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



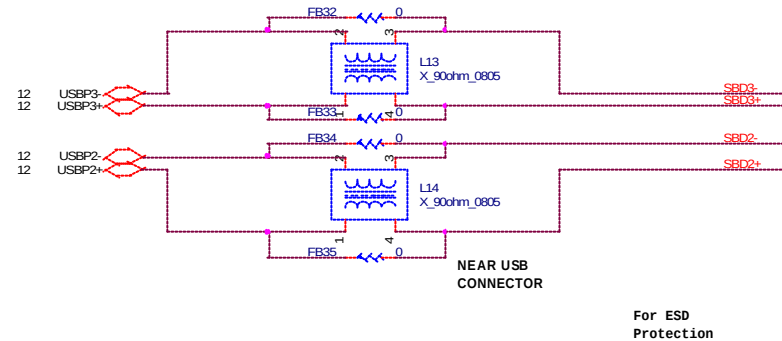
Intel Front USB Header



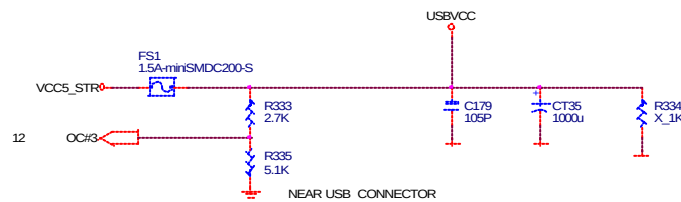
MSI Front USB Header



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

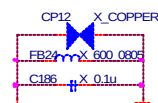
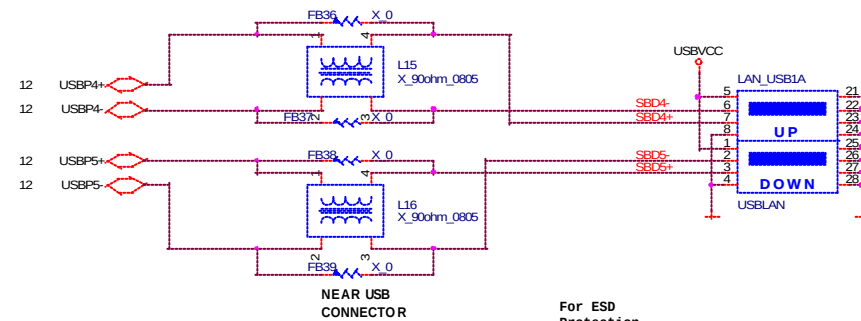


POWER CIRCUIT FOR USB PORT 4,5



- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signal Trace, Spacing : 18 mils
- * USB Power Trace must be 40mils width

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

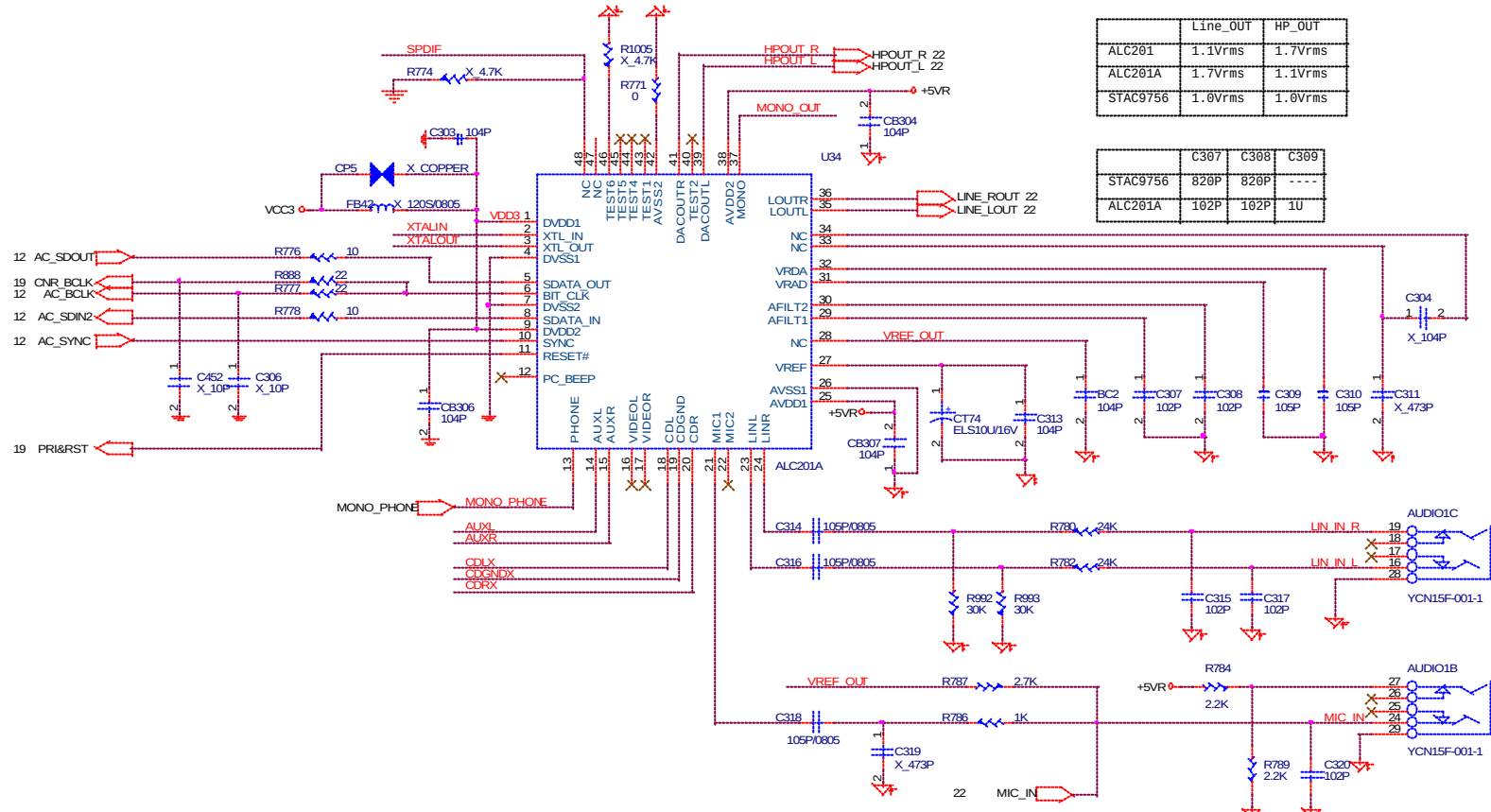


MICRO-STAR INT'L CO.,LTD.			
Title: USB CONNECTORS			
Size	Document Number	MS-6526	Rev 300
Date: Monday, May 13, 2002	Sheet	20	of 29

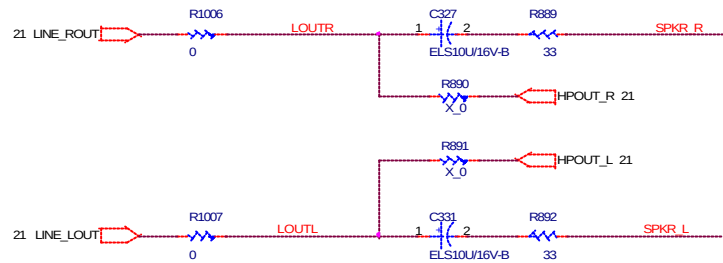
ALC201A AC97 CODEC

	Line_OUT	HP_OUT
ALC201	1.1Vrms	1.7Vrms
ALC201A	1.7Vrms	1.1Vrms
STAC9756	1.0Vrms	1.0Vrms

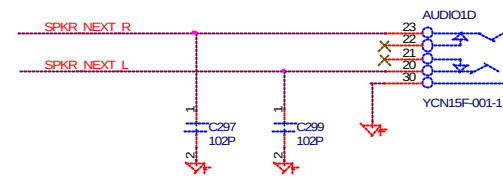
	C307	C308	C309
STAC9756	820P	820P	---
ALC201A	102P	102P	1U



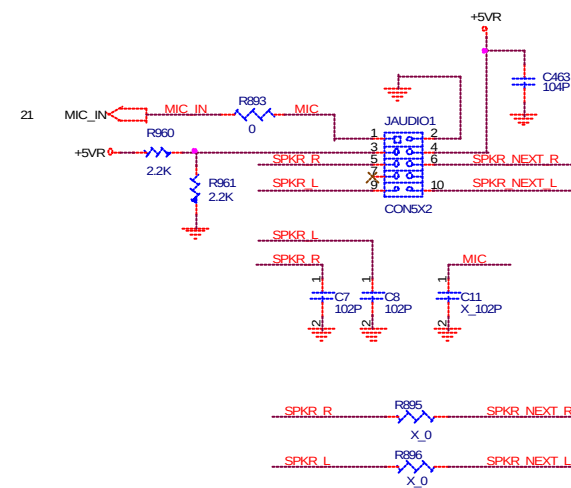
SPEAKER OUT CIRCUIT



SPEAKER OUT JACK



FOR Intel INTERNAL HEADER



MICRO-STAR INT'L CO.,LTD.

Title **AUDIO AMPLIFIER**

Size	Document Number
	MS-6526

Date: Monday, May 13, 2002 Sheet 22 of 29

[illegible][illegible]

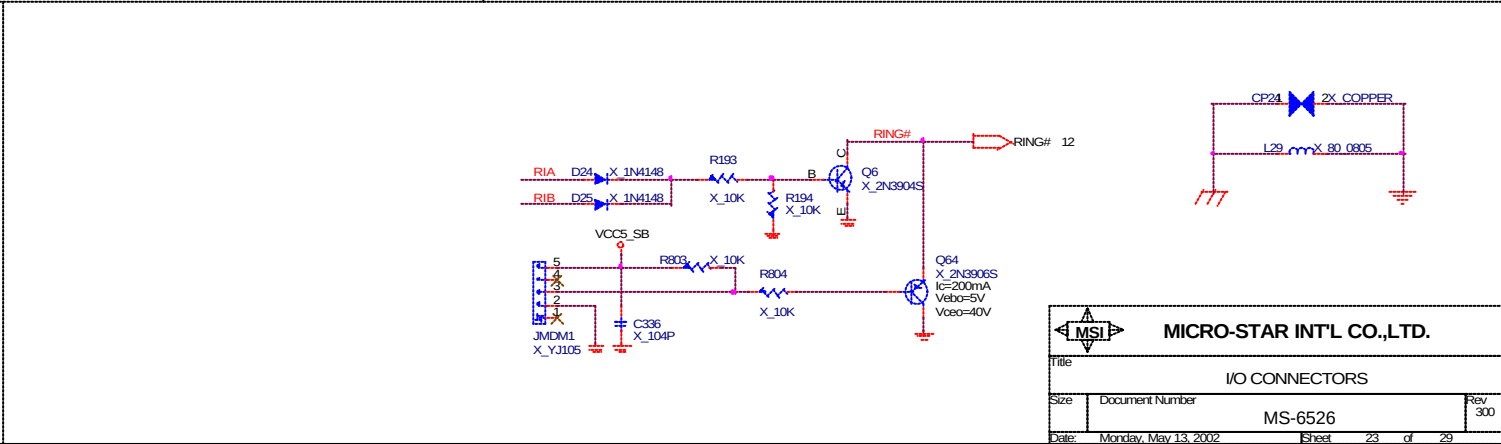
The schematic diagram illustrates the Parallel Port interface. It shows the connection between the microcontroller's parallel port pins and the LPT1A chip. The data bus (D0-D7) is connected to the LPT1A data pins. The status signals (ACK#, BUSY, ERR#, INIT#, SUN#) are connected to the LPT1A status pins. The control signal (STB#) is connected to the LPT1A STB pin. The LPT1A chip is also connected to VCC and GND. A 2.2K pull-up resistor is connected to the STB# line. The LPT1A chip is labeled LPT1A.

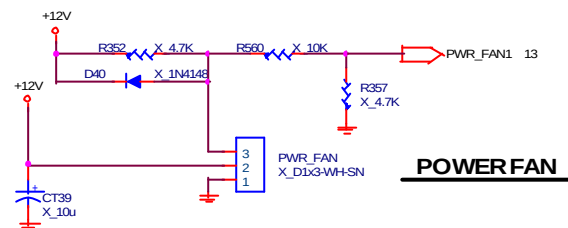
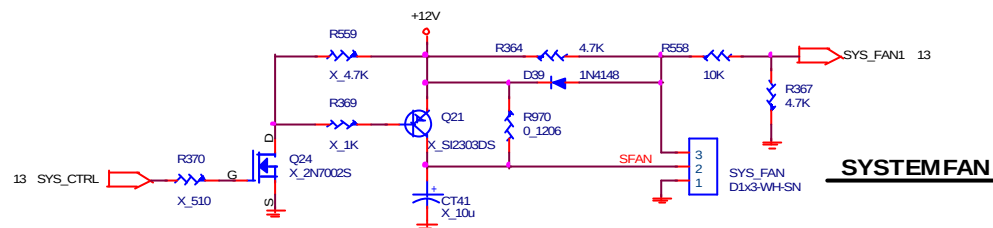
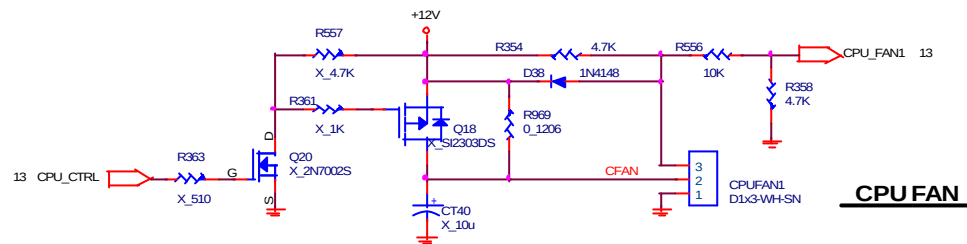
FLOPPY CONNECTOR

The diagram shows a vertical connector with 34 pins. Pins 1 through 34 are numbered on the left. Pins 1, 5, 9, 13, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are connected to a common ground rail on the left. Pins 2 through 34 are connected to various signals on the right. The signals are: DRVDEN0 13, DRVDEN1 13, INDEX# 13, MOT_A# 13, DRV_B# 13, MOT_A# 13, MOT_B# 13, DIR# 13, STEP# 13, WT_DT# 13, WT_EN# 13, TRACK0# 13, FDD_WP# 13, RDATA# 13, HEAD# 13, and DSKCHG# 13.

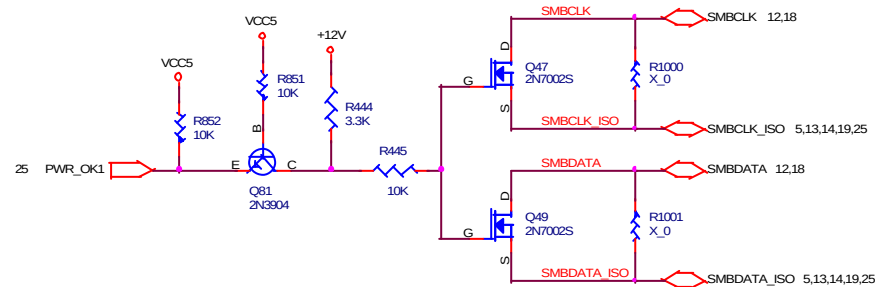
Pin	Signal
1	Ground
2	DRVDEN0 13
3	Ground
4	Ground
5	Ground
6	DRVDEN1 13
7	Ground
8	INDEX# 13
9	Ground
10	MOT_A# 13
11	Ground
12	DRV_B# 13
13	Ground
14	MOT_A# 13
15	Ground
16	MOT_B# 13
17	Ground
18	DIR# 13
19	Ground
20	STEP# 13
21	Ground
22	WT_DT# 13
23	Ground
24	WT_EN# 13
25	Ground
26	TRACK0# 13
27	Ground
28	FDD_WP# 13
29	Ground
30	RDATA# 13
31	Ground
32	HEAD# 13
33	Ground
34	DSKCHG# 13

D2x17-1:31-BK



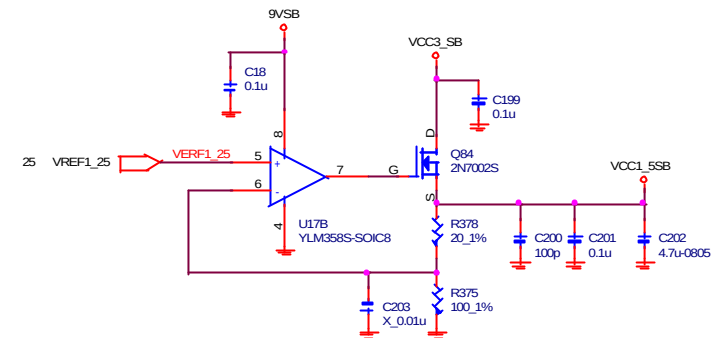


SMBus Isolation

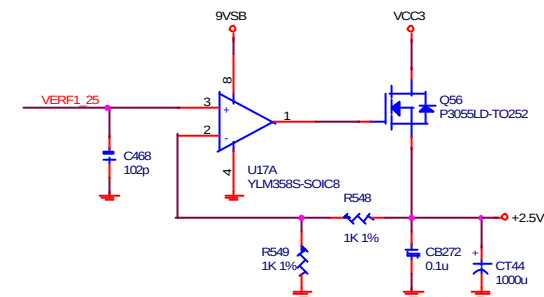


1.5V STANDBY POWER TRANSLATOR

(40mils trace/20 mils space)



AGP4X & GMCH 1.5V POWER TRANSLATOR



MICRO-STAR INT'L CO., LTD.

Title			FAN
Size	Document Number		MS-6526
Date	Monday, May 13, 2002	Sheet	24 of 29

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	OV
MEM_STR	Main	Standby	OV

Near
302D

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

DDR VTT Power

1.25V/2.1A

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR SETTING BY SEL1

FOR 3VDUAL
SETTING BY
SEL1

** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

Wide Trace

DDR 2.5V Power

2.5V/2.8A+5.92A

5V DUAL Power

CHARGE PUMP VOLTAGE OUTPUT

VCC_VID / VID_GOOD

Place MOSFET near CPU

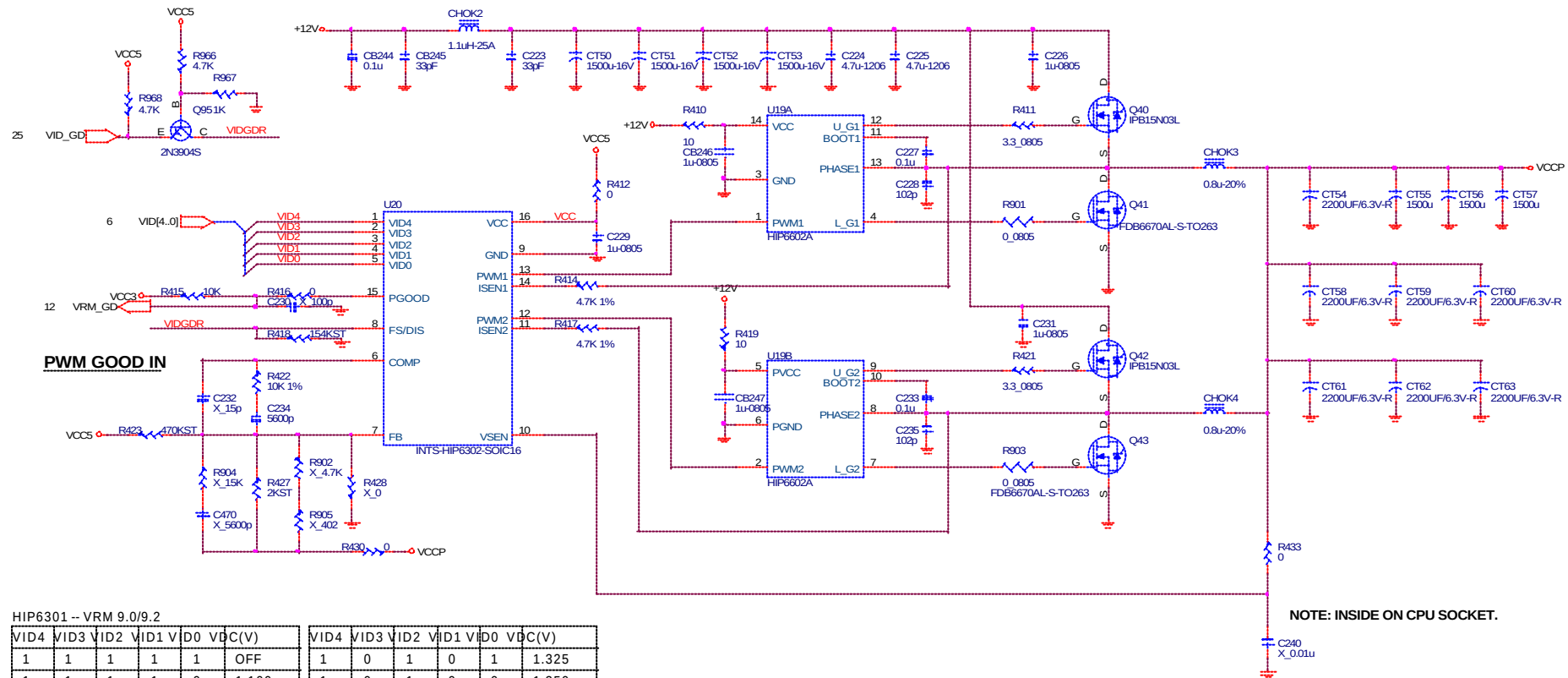
THIS PIN IS OPEN DRAIN OUTPUT

+2.5V
D30
1N4001-S-SM-1
MEM_STR



MICRO-STAR INT'L CO.,LTD.

Title ACPI CONTROLLER		
Size	Document Number MS-6526	Rev 300
Date	Monday, May 13, 2002	Sheet 25 of 29

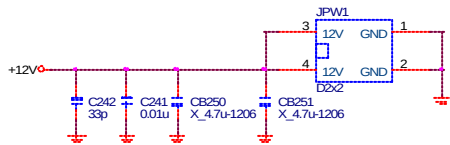


HIP6301 -- VRM 9.0/9.2

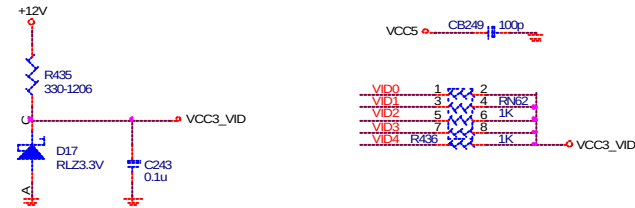
VID4	VID3	VID2	VID1	V	D0	VDC(V)
1	1	1	1	1	0	OFF
1	1	1	1	0	0	1.100
1	1	1	0	1	1	1.125
1	1	1	0	0	0	1.150
1	1	0	1	1	1	1.175
1	1	0	1	0	0	1.200
1	1	0	0	1	1	1.225
1	1	0	0	0	0	1.250
1	0	1	1	1	1	1.275
1	0	1	1	0	0	1.300

VID4	VID3	VID2	VID1	V	D0	VDC(V)
1	0	1	0	1	1	1.325
1	0	1	0	0	0	1.350
1	0	0	1	1	1	1.375
1	0	0	1	0	0	1.400
1	0	0	0	1	1	1.425
1	0	0	0	0	0	1.450
0	1	1	1	1	1	1.475
0	1	1	1	0	0	1.500
0	1	1	0	1	1	1.525
0	1	1	0	0	0	1.550

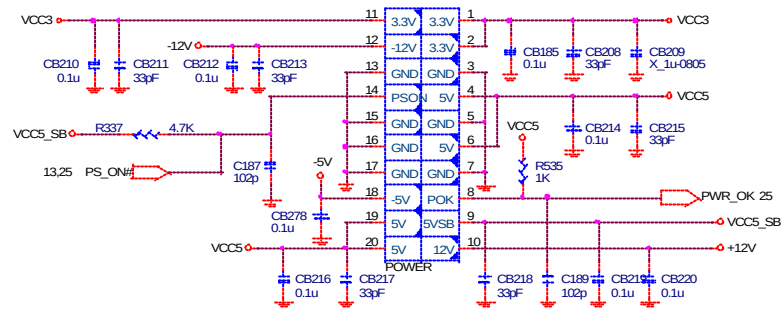
ATX12V POWER CONNECTOR



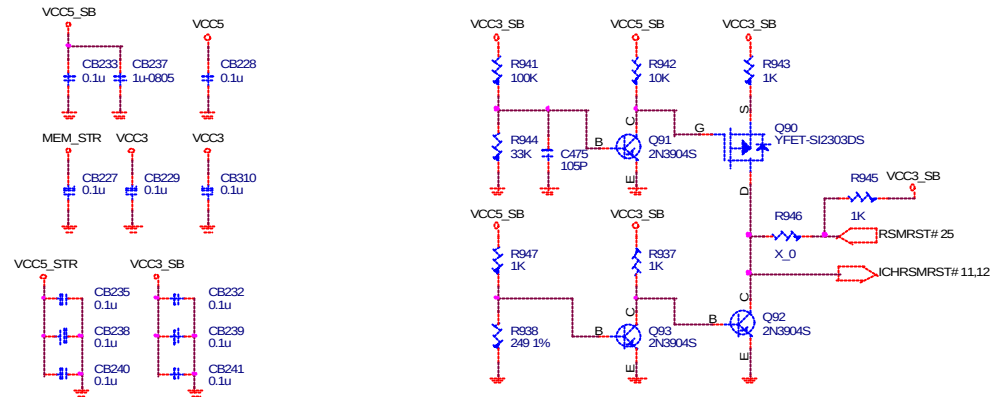
VID PULL-UP RESISTORS



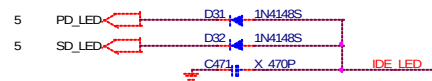
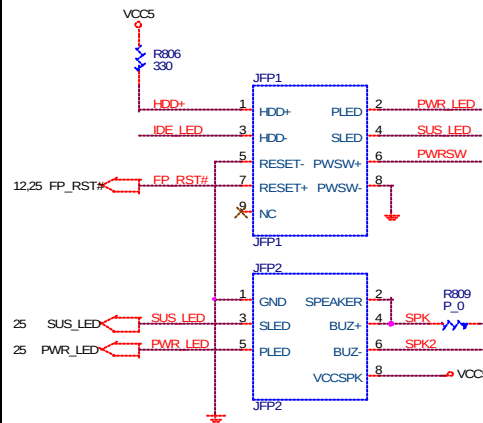
ATX CONNECTOR



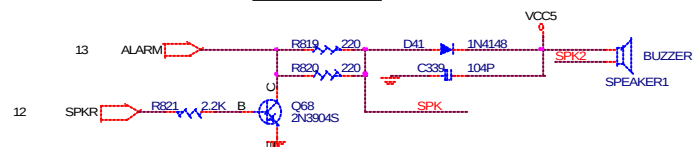
REGULATORS OUTPUT DECOUPLING CAPACITORS



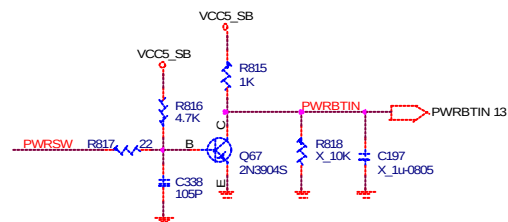
MSI/Intel Front Panel



SPEAKER



POWER BUTTON



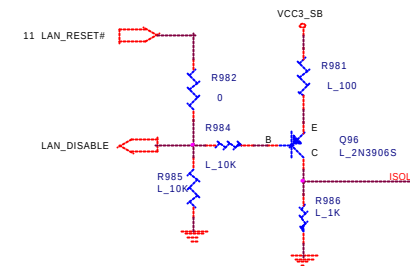
MICRO-STAR INT'L CO.,LTD.

Title	Front Panel & ATX Connector & FAN
-------	-----------------------------------

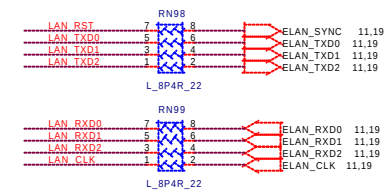
Size	Document Number
	MS-6526

Date: Monday, May 13, 2002 Sheet 27 of 29

LAN DISABLE

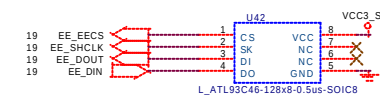


LAN OPTION RESISTORS



LAN EEPROM

Near ICH4

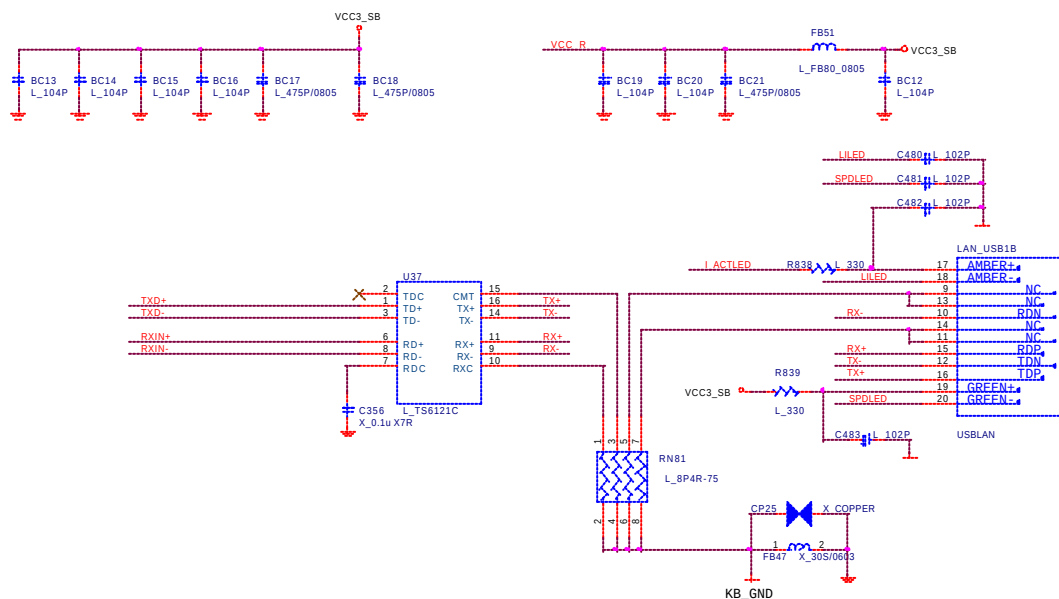
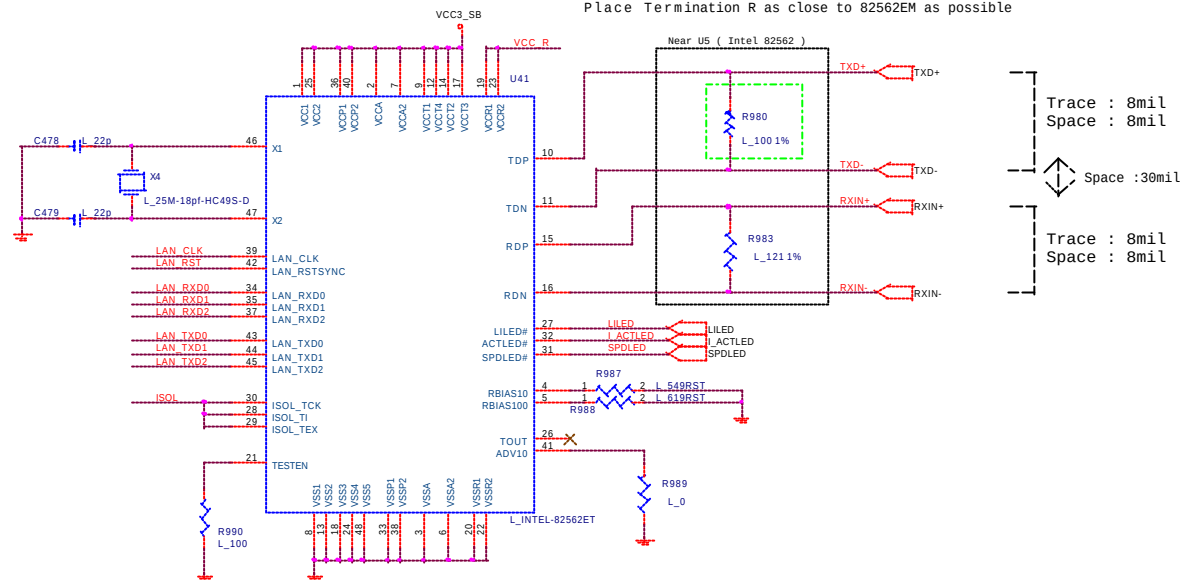


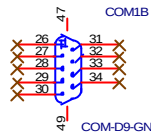
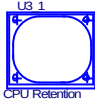
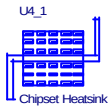
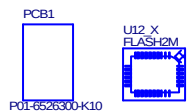
Remark:
82562EM with 93C66:M33-26N0103-A26
82562ET with 93C46:M33-1500203-A26 *

MICRO-STAR INT'L CO.,LTD.

Title			LAN INTEL 82562EM/ET
Size	Document Number	MS-6526	Rev 300
Date	Monday, May 13, 2002	Sheet	28 of 29

Place Termination R as close to 82562EM as possible

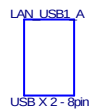
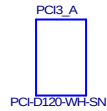




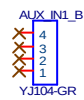
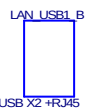
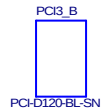
JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED



Option :M



Option :M



MICRO-STAR INT'L CO.,LTD.

Title			
MANUAL PARTS			
Size	Document Number		Rev
	MS-6526		300
Date:	Monday, May 13, 2002	Sheet	29 of 29