7.THEORY OF OPERATION

Circuit Composition And Operation Theory The basic explanation for the circuit composition

21-1901 consists mainly of the one board controlling the analog circuit parts and the digital circuit parts for the other control.

Receiver

21-1901 transmission parts is composed in the double conversion system, which has the 1st IF Frequency of 10.7MHz and the 2nd IF frequency of 450KHz . With the frontend circuit which has an excellent band characteristic and spite characteristic, the Ceramic filter used in the 1st IF, and the 3 pole ceramic filter in the 2nd IF, the reception interrupting factors such as the image and the sensitivity repression are reduced for the more stable reception.

RF Frontend

The signal received by the antenna will be transmitted to the frontend through the antenna switching circuit consisted of LT6, LT7, CT24, CT23 and CT25. The fronted consists of the RF amplifier transistor QR1, primarily diminishes the other signal rather then the 1st IF image and other signal within the reception band and amplifies only the necessary signal within the RF.

1st Mixer

The receiver signal which has been amplified in the RF fronted is provided to the base of the 1st mixer QR2. The 1st L/O signal provide from the PLL circuit is supplied to the emitter of QR2 and converted to the 1st IF 10.7MHz.

1st IF Filter and 1st IF Amplifier

The signal covered by QR2 to 10.7MHz, the 1st frequency, change its impedance through LR4 and then is infused to the fundamental CF which has the center frequency of 10.7MHz and the band width of +/- 280KHz.
Here, the signal reduces the image and other unwanted signal for the 2`nd IF, Then the signal is infused to the QR3, the 1st IF amplifier. The signal infused to the 41th of the is amplified approximately by 20dB in other to acquire the required reception sensitivity, and infused to the IC8which functions as the 2`nd mixer, the 2`nd IF amplifier, and the FM detector.

2nd Mixer, 2nd IF, FM Detector (IC 8)

The receiver IF signal of 10.7MHz, which has been infused to IC8 is mixed with the 2nd L/O signal of 10.250MHz, and converted to 450KHz, the 2`nd IF frequency. The receiver signal converted to the 2nd IF frequency passed through the FC2, the ceramic filter of 450KHz again. After the limiting inside the IC8 and the FM demodulating by the quadrature detector inside the IC8, the signal offers the output through the 26th pin of the IC8.
The squelch circuit is composed to detect the noises from the received signal demodulate in the 26th pin of the IC8. For this purpose, the noise filter is using the OP amplifier inside the IC8.

De-Emphasis

The audio signal which has been FM demodulate in the IC8 is supplies to CR16,21,34,35,RR15,17,18 which function as the De-emphasis.

Audio Power Amplifier (IC2)

The received audio signal which has been adjusted to the 2nd pin of the IC2 and amplified approximately by 20dB. Then, it turns up

the speaker with the maximum output of 0.3Watts.
The 3th pin of the IC2 is the audio mute terminal. If a voltage supply to the 7th pin of the IC2 is supplied to this terminal, the IC2 stops functioning as the audio power amplifier regardless of the signal supplied to the 2nd pin of the IC2, and there is no sound from the speaker.

Transmitter

The transmission part of the 21-1901 is designed to amplify the RF signal oscillated and modulated by the synthesizer to approximately below 0.3(0.23) W by the power transistor of QT3.

Pre-emphasis (IC8)

The voice signal input from the microphone is pre-emphasized at the 9th of the IC8. The signal which comes out of the 18th of the IC8 is limited to a certain amplitude for the voice signal not to exceed the allowable band width assigned for transmission.

TX Power (QT3)

The transmitted signal of approximately 7mW, combined at the PLL module is supplied to the
base of the QT3 amplifier. The transmitted signal amplified to 0.7(0.55) Watts here passes the TX LPF of the 2nd characteristic of the LT4 and the LT5, and RX/TX switching takes place by the DT2. After this, the signal is provided to the antenna the TX LPF of the 1st characteristics, consisted of the LT6.

Frequency Synthesizer

Voltage Control Oscillator (VCO)

The VCO of the 21-1901 oscillates 462 ~ 467MHz under the transmission condition and 451 ~ 457MHz under the reception condition. The VCO consists of the colpits oscillator of the QV2, and contains the oscillator frequency of approximately 10.7MHz during the transmission / reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared to transmission, the DV2 is directly biased by the QV1.
Therefore as a result, the CV6 is added in parallel to the resonance circuit of the VCO to oscillate a low frequency. During transmission, a relatively high frequency should be oscillate compared to reception. Therefore, the DV2 is adversely biased by the QV1, and as a result, the CV6 which is added in parallel to the resonance circuit of the VCO is removed to oscillate the desired transmission frequency.
The VCO is controlled by the IC8 PLL IC in order to oscillate the accurate frequency. The VCO is controlled by the IC8 PLL IC in order to oscillate accurate frequency. The output frequency of the VCO is supplied to the IC8 PLL IC immediately. At the IC8, TCXO(10.25MHz) by the TCXO-1 is compared to the output frequency of the VCO. The VCO is controlled through the loop filter consisted of the RL4, and the CL5 in order to oscillate the stable frequency wanted for the radio.
The VCO controlled voltage which voltage passed the loop filter is supplies to the DV1 varactor diode, and the VCO an oscillate the PLL programmed frequency by the capacity varation in the DV1. In addition, the LV2 on the VCO circuit functions as frequency for the VCO to be properly controlled by the IC8 PLL IC.

RX/TX Buffer Amplifier (QF1, QT1)

The RF signal oscillate at the VCO is provide to the QR2 RX 1st mixer through the QR2 during the reception, and is provide to the QT2 power driver amplifier through the QT1 during the transmission.

PLL Frequency Synthesizer (IC8)

The PLL synthesizer of the 21-1901 consists of the signal loop PLL circuit with the reference of 12.5KHz. The IC8 PLL IC includes all the functions such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.

At the reference oscillator, the 10.25MHz TCXO of the CTX1 is connected to the pin 53 of the IC8 to oscillate the frequency of 10.25MHz. The TCXO(10.25MHz) is the temperature compensation circuit to maintain the frequency withen the allowable error range even under a low temperature of -20 .

The phase detector send out the output power to the loop filter through 46 pin of the IC8. If the oscillation frequency of the VCO is low compared to the reference frequency, the phase detector sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector sends out the output power in negative pulse. Therefore, the VCO can maintain the frequency set.

The programmable divider maintains the desired frequency with the control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below :

N = VCO oscillation frequency / reference frequency

If the desired frequency is 462.5625MHz

N = 462.5625MHz / 0.00625MHz = 74010

CPU and Memory

Most of the control functions of the 21-1901 are controlled by the IC3 CPU. The IC3 CPU has the internal ROM in the capacity of 8Kbyte, and the program for the operation of the IC3.