Redwire M-12 User's Manual

The M-12 module from Redwire is a fast and easy way to create a 6LoWPAN, Zigbee, or general 802.15.4 device without additional RF design or certifications and without the need for an external host microcontroller.

Features

- based on the Freescale MC13224v ARM7 microcontroller with 802.15.4 radio
- 3.6V - 2.1V operating voltage
- 24MHz, 96kB RAM
- FCC certification
  FCC ID: QP0-M12
- on-board PCB trace antenna
- 3dBm output power
- Integrated Bootloader
  (UART1, SPI, or I2C)
- Secondary boot flash to facilitate robust over-the-air reprogramming
- 32.768 kHz real time clock crystal
- includes buck inductor for additional efficiency in battery operated applications
- Mini-card PCIe card edge connector (not PCIe compatible)
- 48 General purpose I/O pins, 46 with peripheral functions.
- 6LoWPAN support with the Contiki OS software environment
- Zigbee support with Freescale BeeKit

Specifications

Dimensions

Overall

Length:	45.1	mm
	1.775	in
Width:	30.1	mm
	1.185	in
Height:	6.2	mm
	0.245	in

Current Draw

Sleep

Min:	2	uA
Max:	150	uA

Idle

Typical:	3	mA

Transmitting

@3dBm:	35	mA

Receiving

Typical:	24	mA

RF

TX power

Max:	3	dBm
Min:	-30	dBm

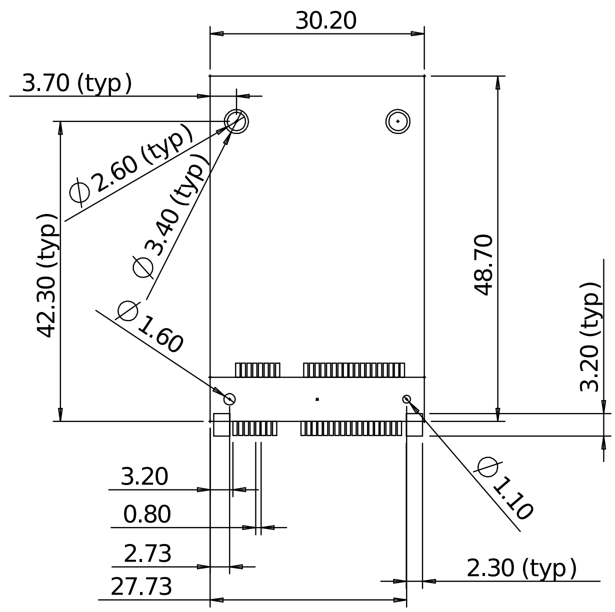
RX sensitivity

Max:	-96	dBm
Min:	-100	dBm

Range

Indoors:	100	ft
Outdoors:	300	ft

Recommended PCB Footprint



(dimensions in mm)

Eagle .lbr

Suggested connectors:

1.7mm (0.68 in) clearance:

Connector:

JAE	MM60-52B1-B1-R***
Mouser	656-MM60-52B1-B1-R

Standoff:

JAE	NT1R3000
Digikey	670-2481-1-ND

3.6mm (0.141 in) clearance:

Connector:

Molex	48338-0065
Mouser	538-48338-0065

Standoff:

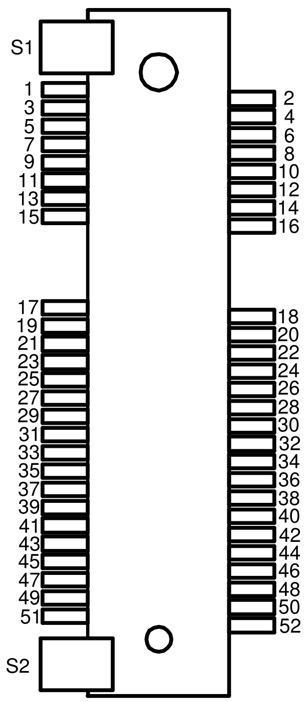
JAE	NT1R3000
Digikey	670-2481-1-ND

Screws:

M2 x 4mm:

McMaster-Carr	92005A016

Pinout



S1 and S2 are GND or NC

Number	Name	Number	Name
1	ADC0	2	VREF2H
3	ADC1	4	VREF1H
5	ADC2	6	VREF1L
7	ADC3	8	VREF2L
9	ADC4	10	ADC5
11	ADC6	12	ADC7/RTCK
13	TDO	14	TDI
15	TCK	16	TMS
17	U2RTS	18	U2CTS
19	U2RX	20	U2TX
21	U1RTS	22	U1CTS
23	U1RX	24	U1TX
25	I2C_SDA	26	I2C_SCL
27	TMR3	28	TMR2
29	TMR1	30	TMR0
31	SCK	32	MOSI
33	MISO	34	SS
35	SSI_BTCK	36	SSI_FSYN
37	SSI_RX	38	SSI_TX
39	KBI7	40	KBI6
41	KBI5	42	KBI4
43	KBI3	44	KBI2
45	KBI1	46	KBI0
47	RESERVED	48	GPIO50
49	GPIO43	50	RESET
51	GND	52	VBATT

Essential Pins

Power Pins

VBATT	POWER	2.1V - 3.6V	The MC13224v will operate correctly when VBATT is between 3.6V and 2.1V. Applying voltages above 3.6V to any pin could result in permanent damage to the device.
GND	POWER	Ground	

Bootloader Pins

Reset	INPUT	Resets MC13224v	A low voltage on this pin resets the MC13224v. Upon leaving reset, the MC13224v begins execution in the bootloader.
VREF2H VREF2L	INPUT INPUT	External ADC2 reference and internal flash erase	Normally VREF2H and VREF2L are the HIGH and LOW references for ADC2 respectively. If, however, VREF2H is LOW and VREF2L is HIGH after reset, then the bootloader will erase the internal flash. This process takes less than 2 seconds to complete. After erasing the flash, the MC13224v must be reset again to perform any other function.
U1RTS	INPUT	UART 1 Ready-to-send input.	If held low on RESET, the bootloader will use UART1 to load a program if there is not a valid image in internal flash. See the Bootloader Appendix in the MC13224v reference manual for more details about programming with UART1. Several software tools exist that can interface with the serial bootloader. ◦ mc1322x-load.{pl,c}: simple command-line tools with many programming features. ◦ Freescale TestTool: windows based GUI that can only be used to program the internal flash
U1TX	OUTPUT	UART 1 transmit output.	
U1RX	INPUT	UART 1 receive input.	

UART 1 & 2

U1RTS	INPUT	UART 1 Ready-to-send
U2RTS	INPUT	UART 1 Ready-to-send
U1CTS	OUTPUT	UART 1 Clear-to-send
U2CTS	OUTPUT	UART 1 Clear-to-send
U1TX	OUTPUT	UART 1 transmit
U2TX	OUTPUT	UART 2 transmit
U1RX	INPUT	UART 1 receive
U2RX	INPUT	UART 2 receive

The MC13224v has two independent UART peripherals. They only support 8-bit data and can generate any multiple-of-2 baud rate between 1.2 kbaud and 1,843.2 kbaud.

Example Code

Libmc1322x provides the following examples for using the UARTs:

uart1-loopback.c reads a character from UART1 and echos it back.

u1u2-loopback.c mirrors UART1 to UART2. Characters sent to UART1 are then passed along to UART2. Characters received by UART2 are then echoed by UART1.

ADC

ADC0-7	INPUT	Analog input	
VREFH (1,2)	INPUT	Full-scale voltage reference	
VREFL (1,2)	INPUT	Zero-scale voltage reference	

The MC13224v has two independent 12-bit Analog-to-digital converters. They can run up to 300ksamp/sec and can be synchronized.

The maximum usable code range is approximately 0 to 3900; above 3900 and the conversion saturates (at about 200mV below the full-scale reference)

Typical gain error is +/- 2.8%

Typical offset error is 8 codes.

Interesting Features

Absolute Reference: ADC1 contains an extra channel that reads an internal 1.2V reference. By reading this channel, you can solve ADC codes for absolute voltages even when running from an unregulated supply such as batteries. You can also use this as a measure of Vbatt by solving for the absolute voltage of full-scale.

Sleep mode monitoring: The ADCs can be configured to continue to sample channels while the CPU core is in low-power sleep mode. They can be programmed with a high and/or low comparison value to generate an interrupt and wake the CPU when the voltage has changed.

Example Code

adc.c reads from all ADC channels and outputs the values to UART1 with printf.

TMR

TMR0-3	INPUT/ OUTPUT	Timer / Capture / PWM pins

The MC13224v has four 16-bit counter modules that are very configurable. They can be used to create various waveforms as well as measure or trigger from external sources.

The counters can share the 4 available external pins and they can also be cascaded.

Timer Example

tmr-ints.c sets TMR0 up as a periodic interrupt source and toggles an output pin accordingly.

PWM Example

pwm.c demonstrates PWM function.

KBI

KBI0-3	OUTPUT	Keypad outputs
KBI4-7	INPUT	External interrupt inputs

The MC13224v has four external inputs that can trigger interrupt: KBI4-7. Additionally, these pins can be paired with KBI0-3 to make a 16 switch keypad scanner that operates while the MC13224v is in SLEEP mode; the KBI4-7 can be used to wake-up from SLEEP.

For more details about using the KBI pins for low-power wakeup see Section 3.4 Using KBI Signals as Keypad/ Pushbutton Interface of the MC13224v Reference Manual.

SPI

MISO	INPUT/ OUTPUT	Master In, Slave Out
MOSI	INPUT/ OUTPUT	Master Out, Slave In
SCK	INPUT/ OUTPUT	SPI Clock
SS	INPUT/ OUTPUT	Slave Select

The SPI controller runs at a maximum of 12 MHz and can be programmed as either a Master or a Slave.

Typically SPI is used to interface with external peripheral chips. The SPI controller relieves some computational burden from the CPU when working with such chips.

Booting from SPI

The M12 can boot over SPI from the external dataflash included in the module. The M12 includes a pullup resistor to signal the bootloader to check the external flash for a valid image. If a valid image is present then it will be used.

Additionally, the SS pin is multiplexed between the external flash and the card-edge connector. To enable the SS pin on the card-edge connector, GPIO63 must be pulled HIGH.

SSI

SSI_BTCK	INPUT/ OUTPUT	Bit Clock
SSI_FSYN	INPUT/ OUTPUT	Frame Sync
SSI_TX	INPUT/ OUTPUT	Transmit
SSI_RX	INPUT/ OUTPUT	Receive

The SSI controller is a fast and flexible serial protocol engine. It can be used to interface to CODECS, DSPs, and chips that implement I2S. It can also be configured to do SPI.

Its maximum clock rate is 24MHz (2x faster than the SPI controller) and it also has a two 8x24 bit FIFOs for both transmit and receive.

I2C

I2C_SCL	INPUT/ OUTPUT	Clock
I2C_SDA	INPUT/ OUTPUT	Data

I2C is a simple and efficient two-wire communication interface widely supported by many peripherals. The I2C controller implements all of the features necessary for working which such chips.

JTAG

TDO	OUTPUT	Test Data Out
TDI	INPUT	Test Data In
TMS	INPUT	Test Mode Select
TCK	INPUT	Test Clock
ADC7/ RTCK	OUTPUT	Adaptive Clock

The JTAG interface can be used to monitor and debug the CPU while it is running. JTAG debugging hardware, such as an FT2232H USB debugger, is connected these pins, and the CPU is controlled via host debugging software such as OpenOCD. OpenOCD provides a debug interface to general code debuggers such as GDB which are in turn, often used by code IDE's such as Eclipse.

GPIO

GPIO43	INPUT/ OUTPUT	General Purpose only
GPIO50	INPUT/ OUTPUT	General Purpose only

All of the previously listed pins can also be used as general purpose input and output pins. GPIO43 and GPIO50, have no other special function and can only be used for general purpose input and output.

Each GPIO pin has two bits dedicated in the FUNC_SEL register which enables its peripheral function or general purpose function.

All GPIO pins have configurable pull-ups or pull-downs, input hysteresis, and retained state in low power mode.

Buck Controller

The M12 module contains all the necessary components to use the integrated buck controller in the MC13224v. This allows for more efficient run time operation for Vbatt voltages above 2.5V.

Without the buck controller, Vbatt is regulated to the core voltage of 2.0V by an on-chip LDO regulator. By using a switching buck regulator, the core voltage is generated more efficiently. The benefits of the buck are lost, however, under 2.5V and it should not be used.

For Vbatt = 3.6V, the buck converter reduces power consumption by 15.2%.

For Vbatt = 2.5V, the savings are 5.7%.

With the Contiki Operating System, control of the buck converter is automatic. The MC13224v will probe for the necessary components and enable the buck if appropriate. Vbatt will also be monitored and the buck will be enabled and disabled accordingly.

Sleep Modes

The MC13224v has a flexible system of sleep modes. The two primary modes are Doze and Hibernate. Doze provides an accurate time base when a 32kHz crystal is not present, but uses significantly more power. Since the M12 module has a 32kHz on board, Hibernate mode should always be used.

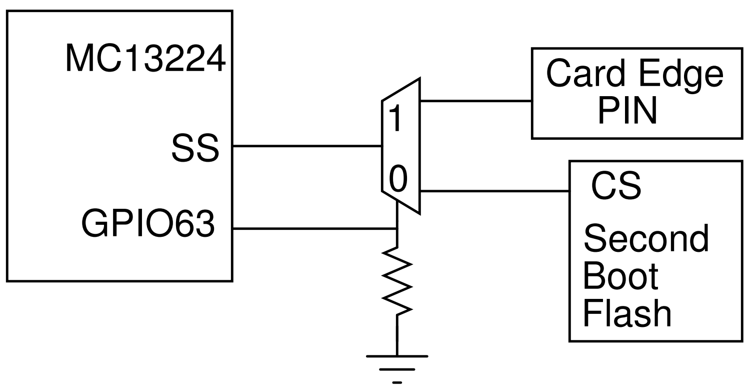
Current	Mode
2 uA	Base hibernate, RAM page 0 retained
+ 8 uA	+ retain CPU state
+ 2 uA	+ retain RAM page 1 or 2
+ 2 uA	+ retain GPIO

Note however, that when retaining GPIO state, extra current maybe used depending on what is connected to the GPIO pins.

SPI Multiplexer

The M12 contains a secondary boot flash to facilitate over-the-air reprogramming. This flash is connected to the MC13224v SPI controller.

To allow for the M12 user to also use all of the features of the SPI bus, the SS line is multiplexed between the second boot flash and the pin on the card edge connector; a pull down resistor ensures that the secondary flash is selected at boot time.



The multiplexer can be switched by driving GPIO63. Application code should drive this pin HIGH if the SS pin is to be used.

FCC Certification

The M12 has a certification from the FCC to be used a modular transmitter. Devices that include the M12 must state on the label that it "Contains FCC ID: QP0-M12"

FCC Statement

This device has been tested and found to comply with part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in aparticular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Note: Modifications to this product will void the user's authority to operate this equipment.

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