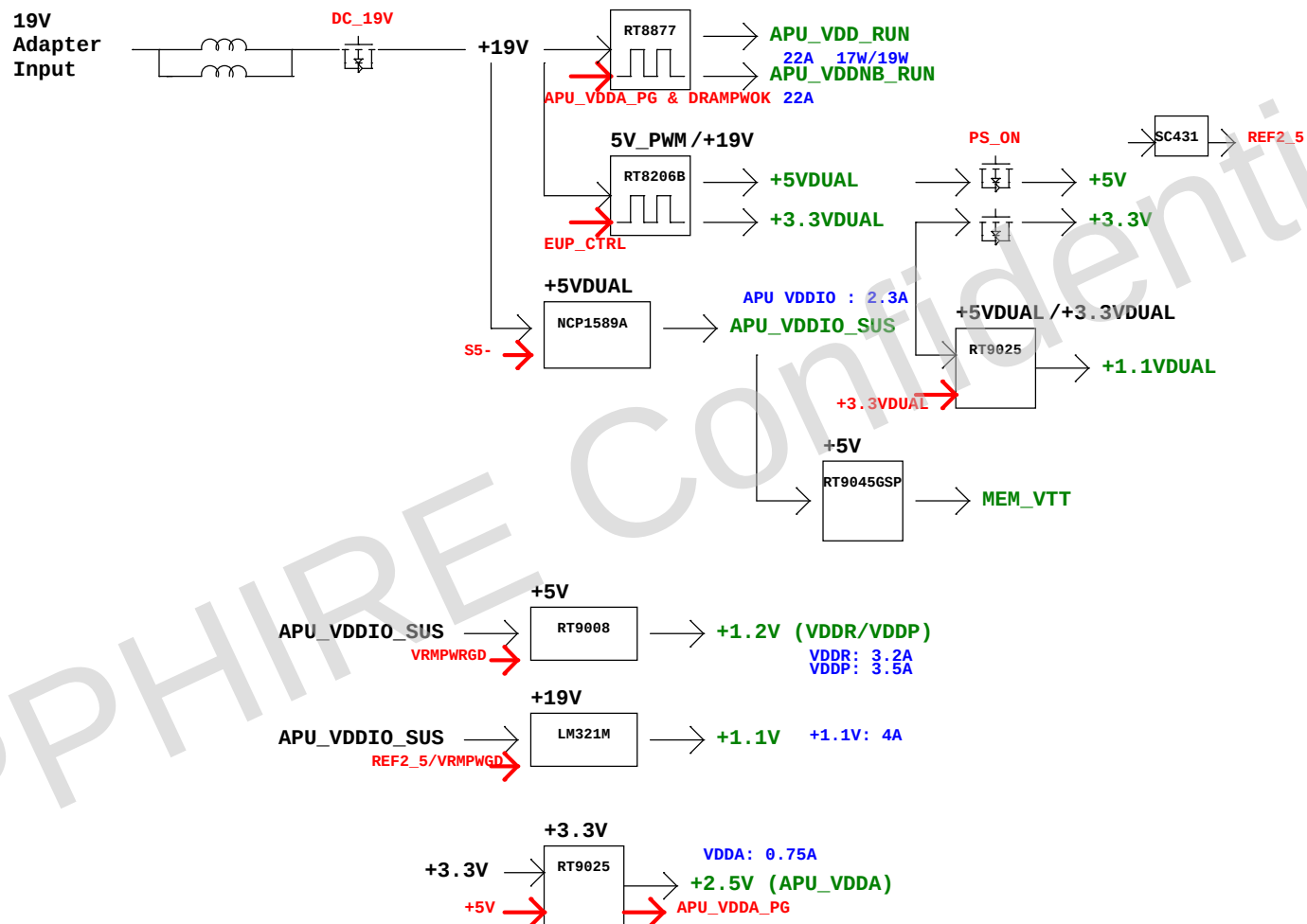




Edge-FP2M3 V1.0

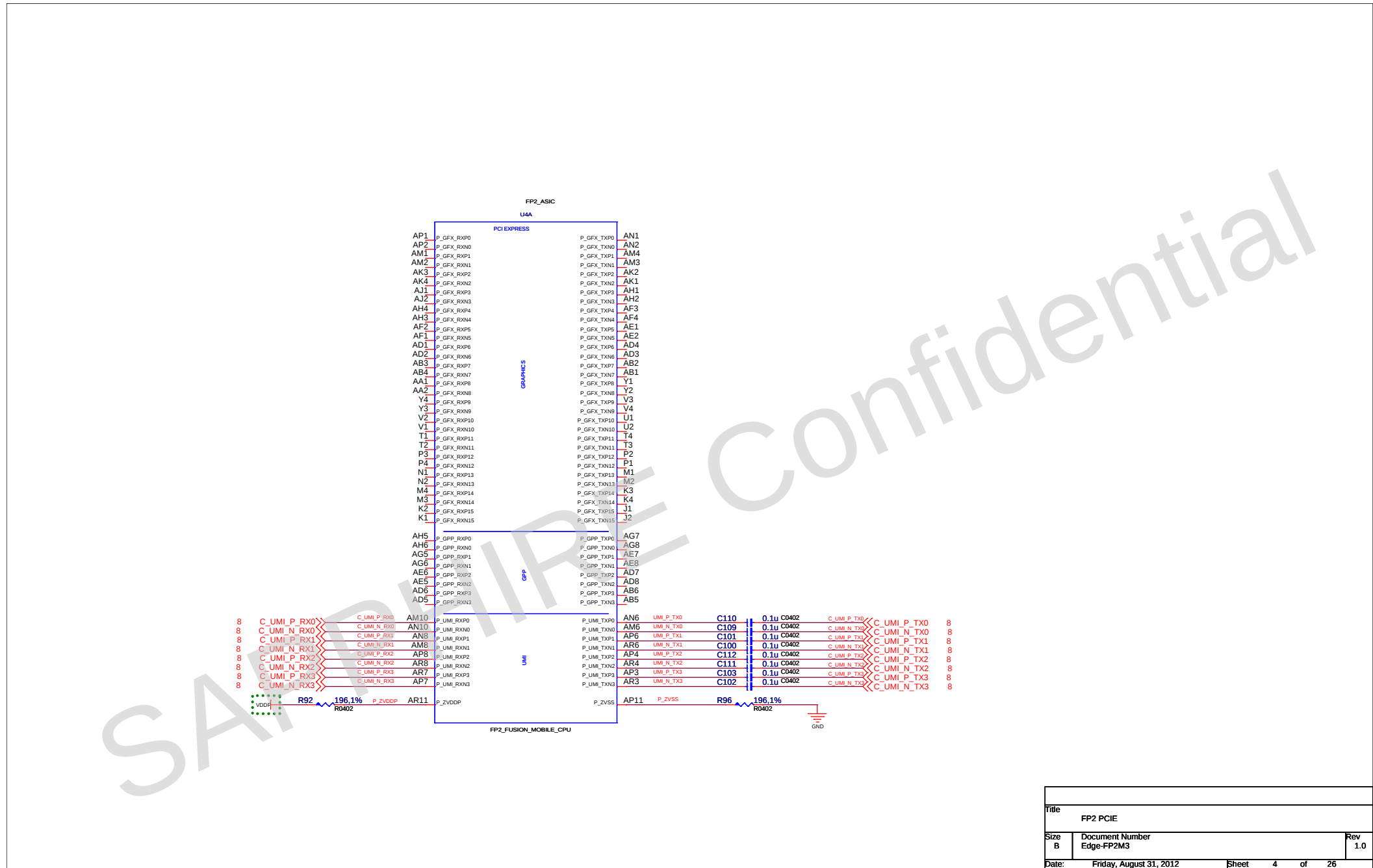
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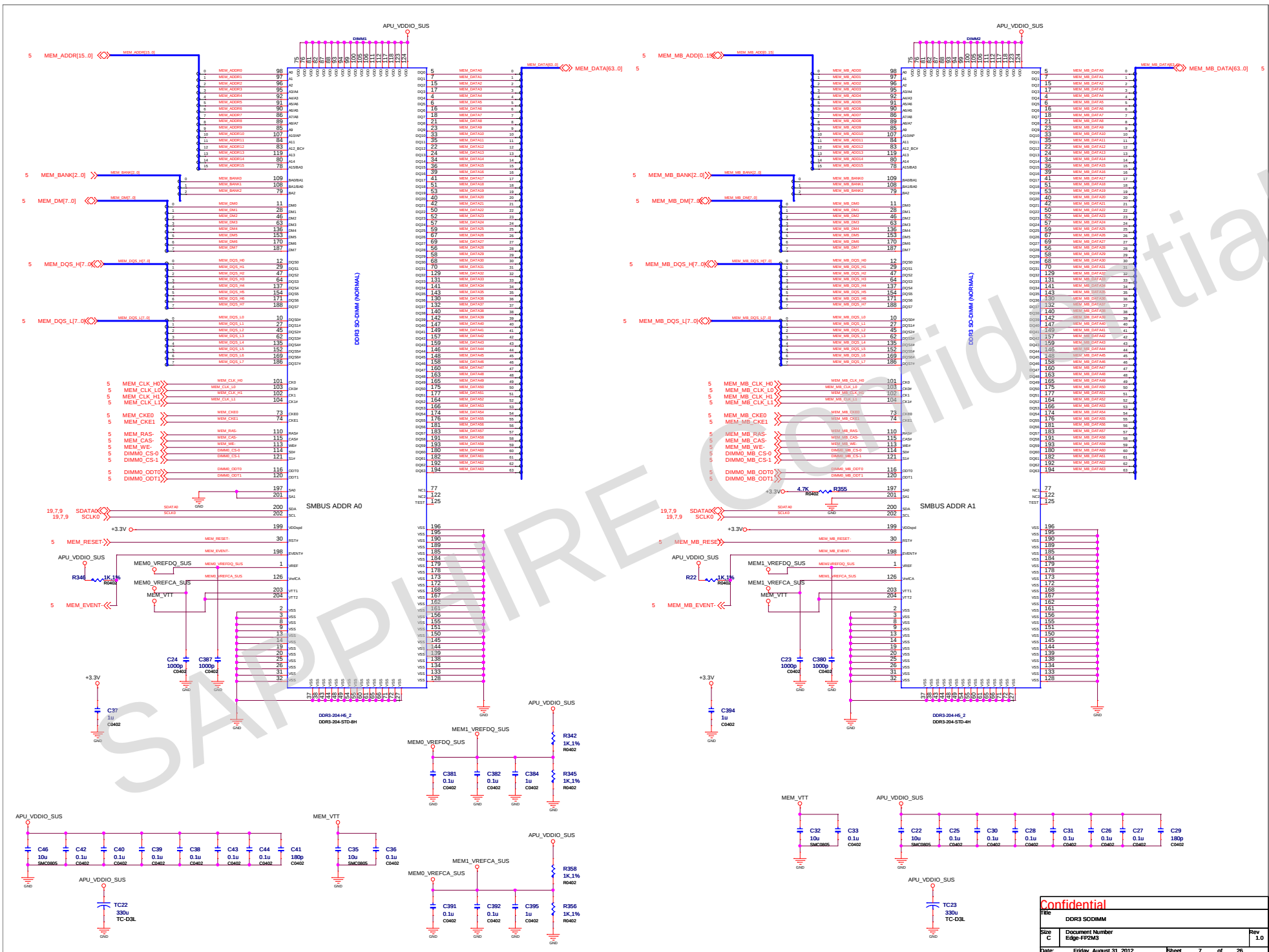
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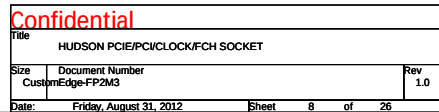
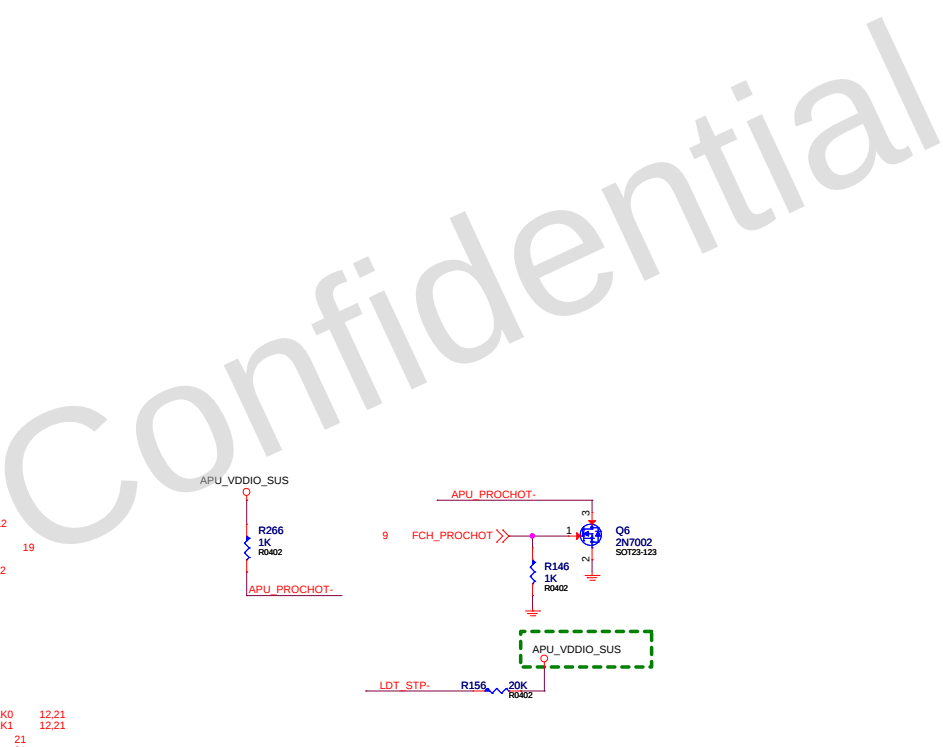


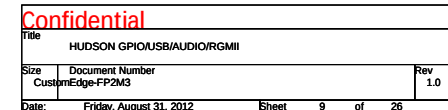
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FP2_PCIE			
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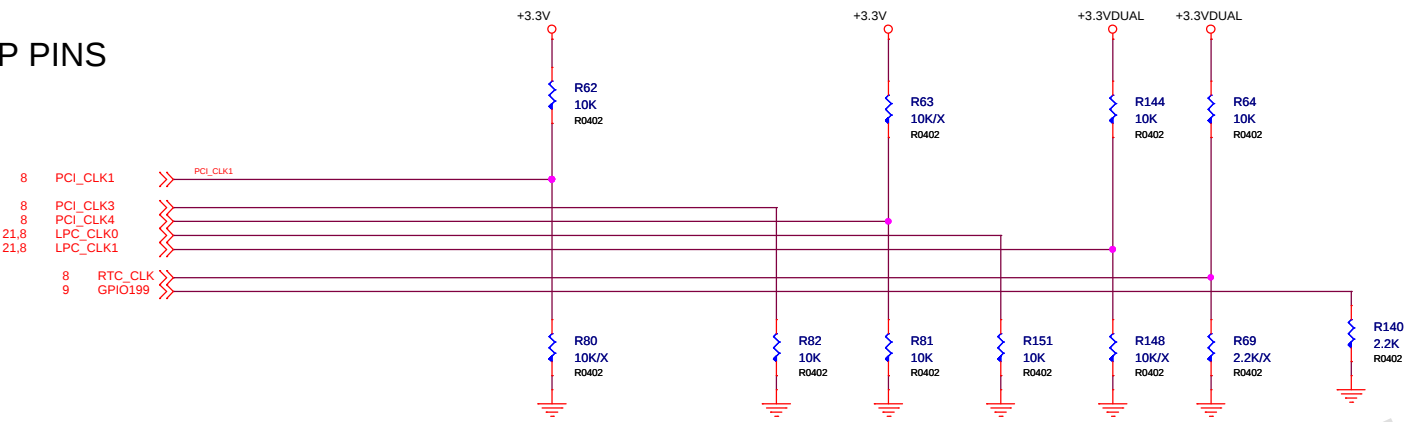


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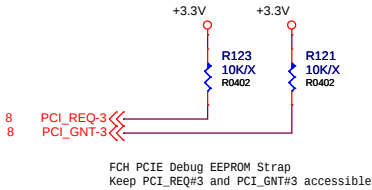




STRAP PINS



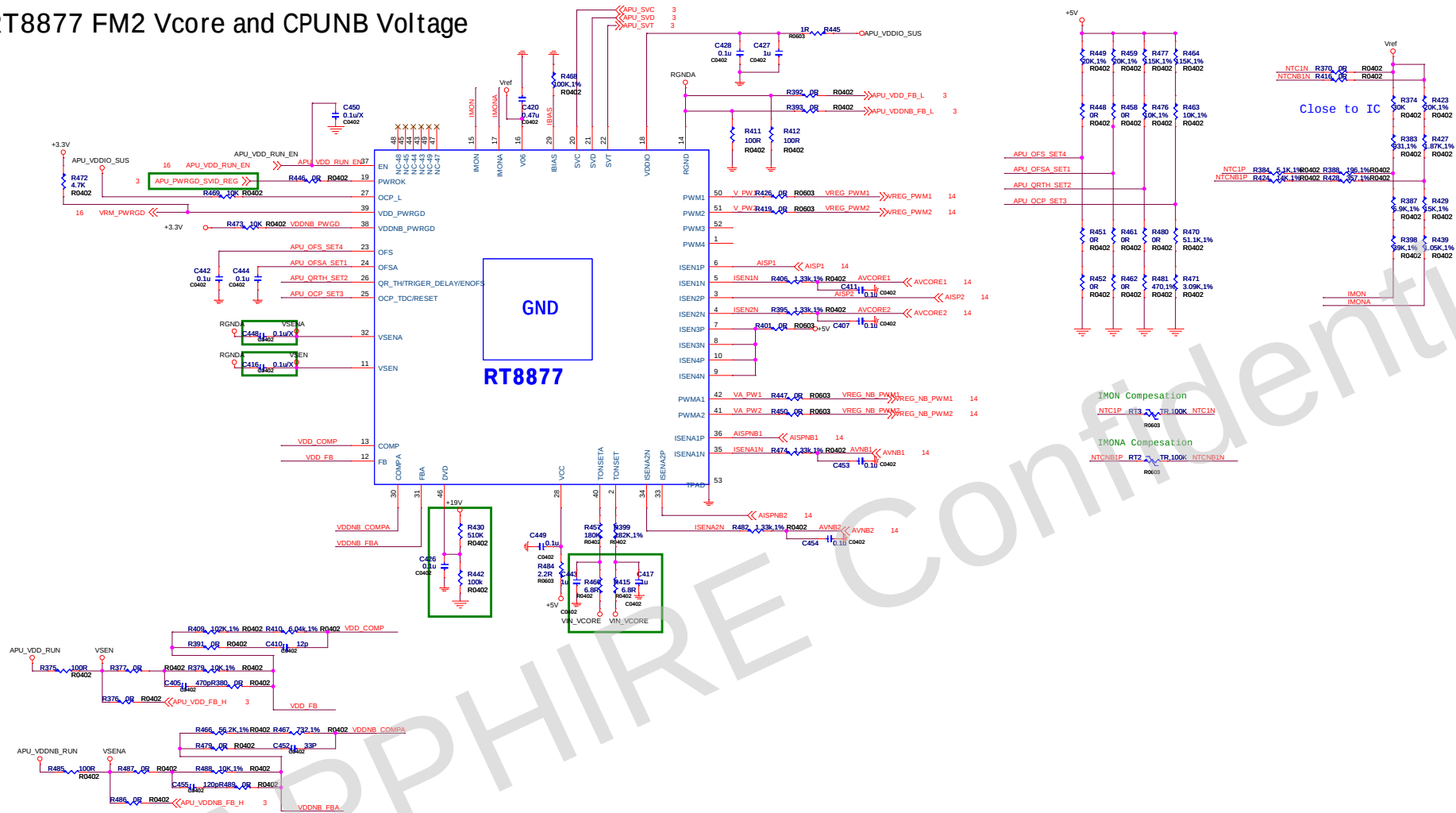
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	GPIO199
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON-FUSION APU CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	SS+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	FUSION APU CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SS+ ENABLE	L = SPI ROM DEFAULT



FCH PCIE Debug EEPROM Strap
Keep PCI_REQ#3 and PCI_GNT#3 accessible

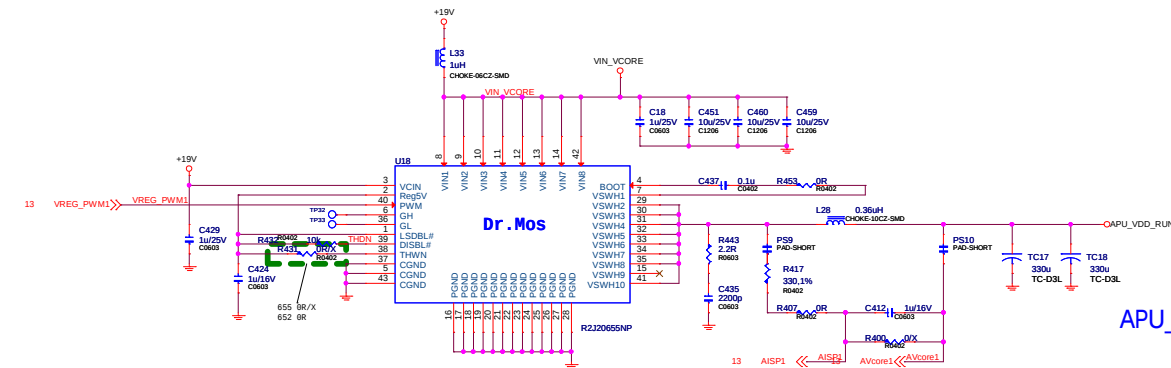
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

RT8877 FM2 Vcore and CPUNB Voltage

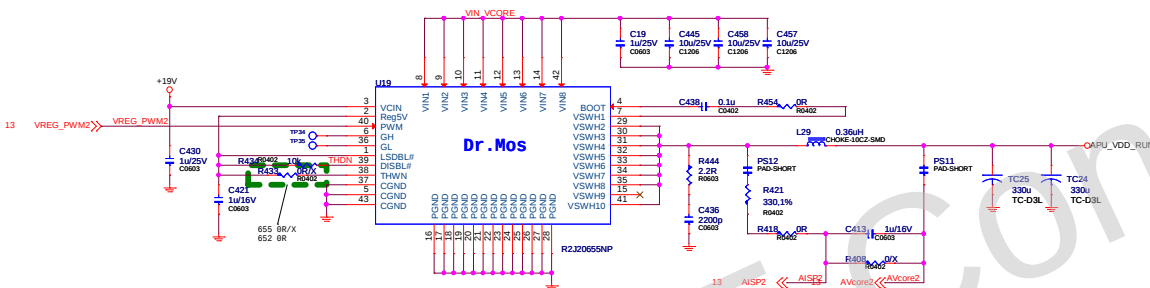


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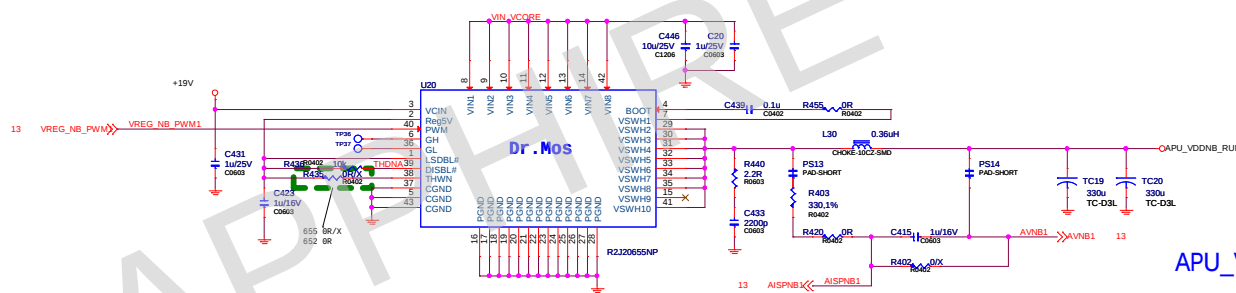
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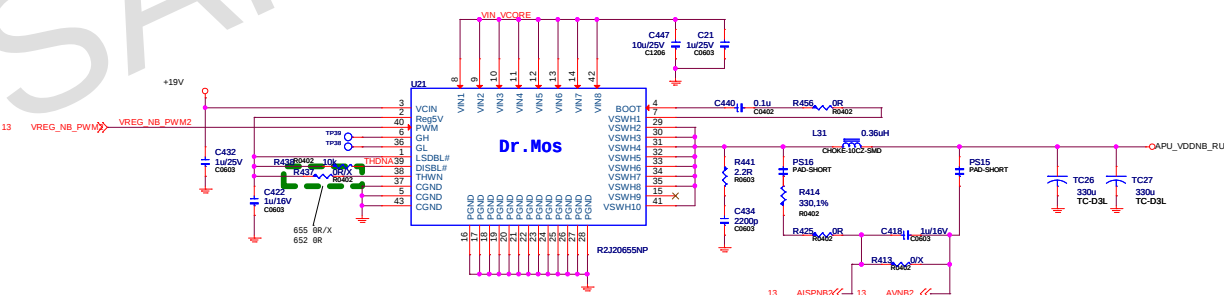
APU_VDD_RUN : TDC 22A



APU_VDD_RUN : TDC 22A



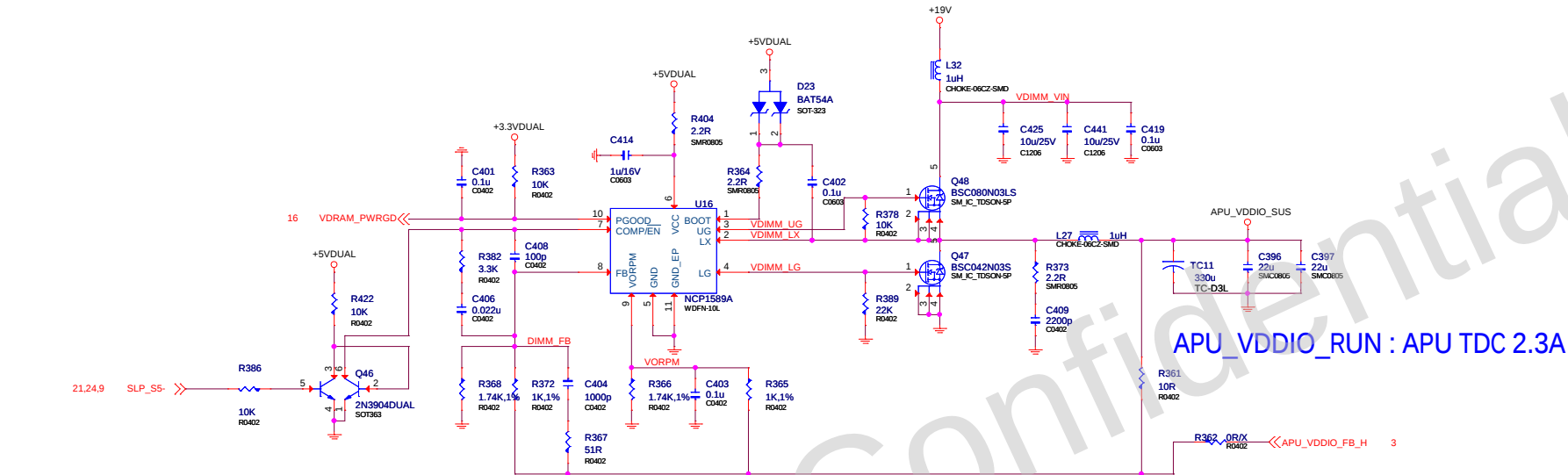
APU_VDDNB_RUN : TDC 22A



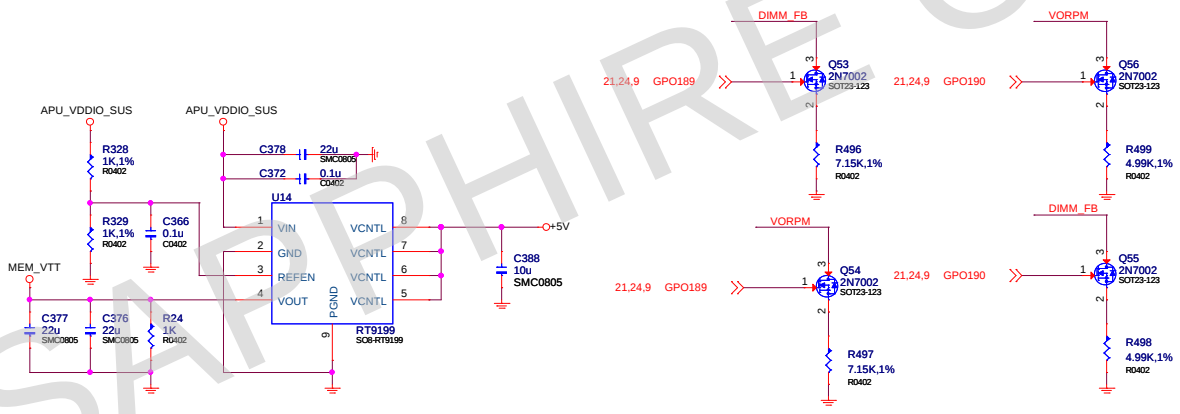
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File	CPU POWER PHASE		
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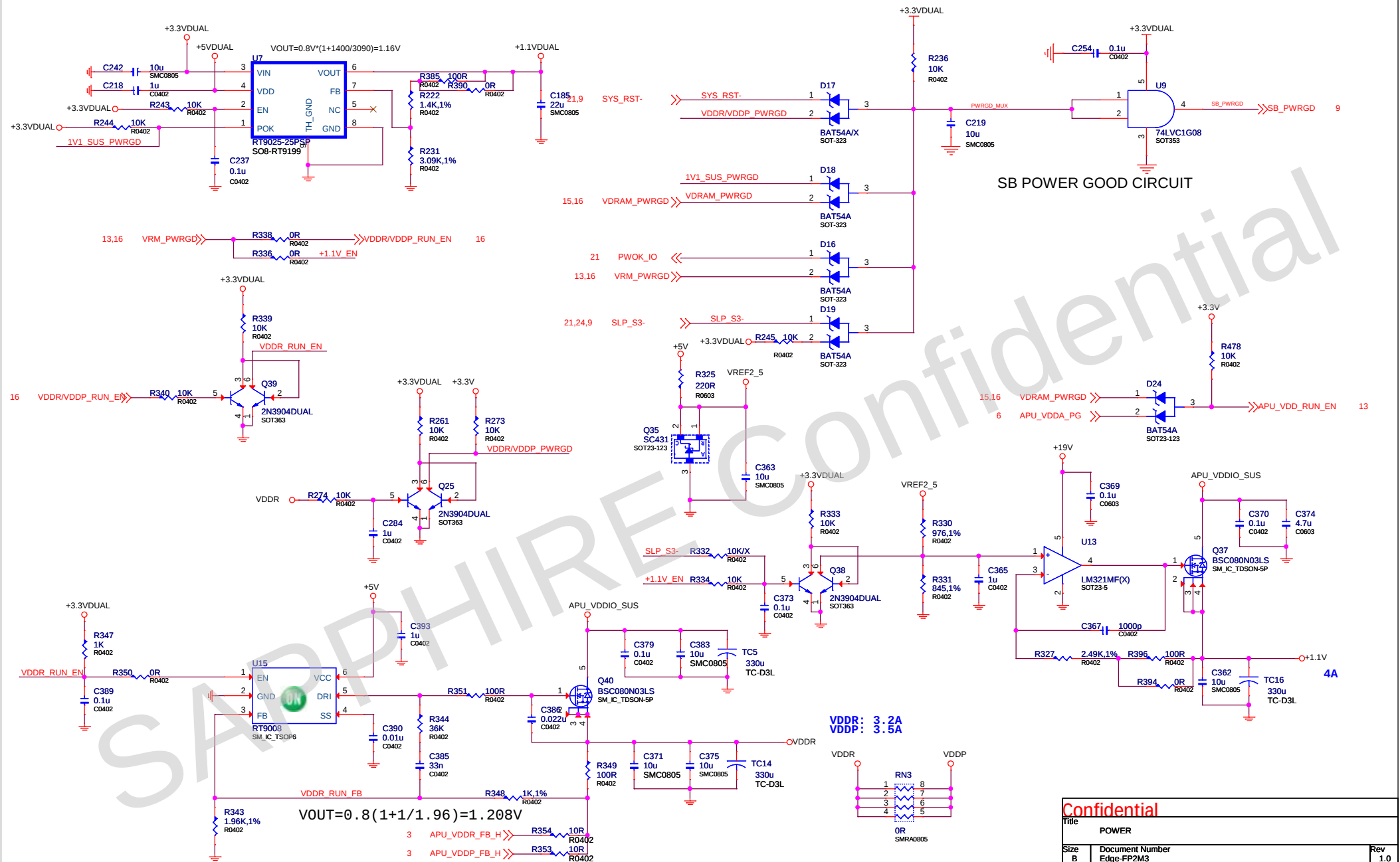
CPU_VDDIO_SUS@ 20A
CPU_VTT_SUS@ 2A

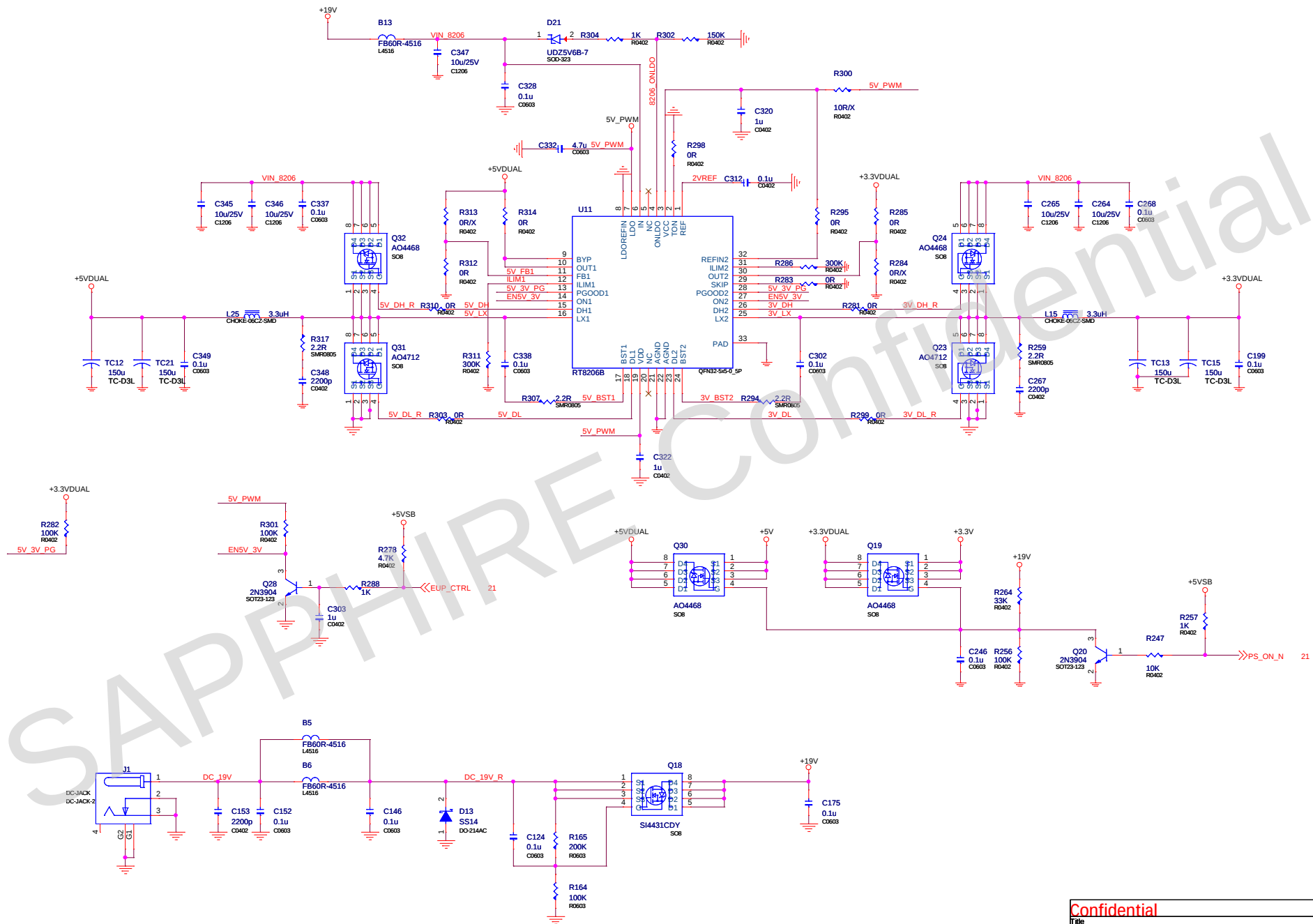


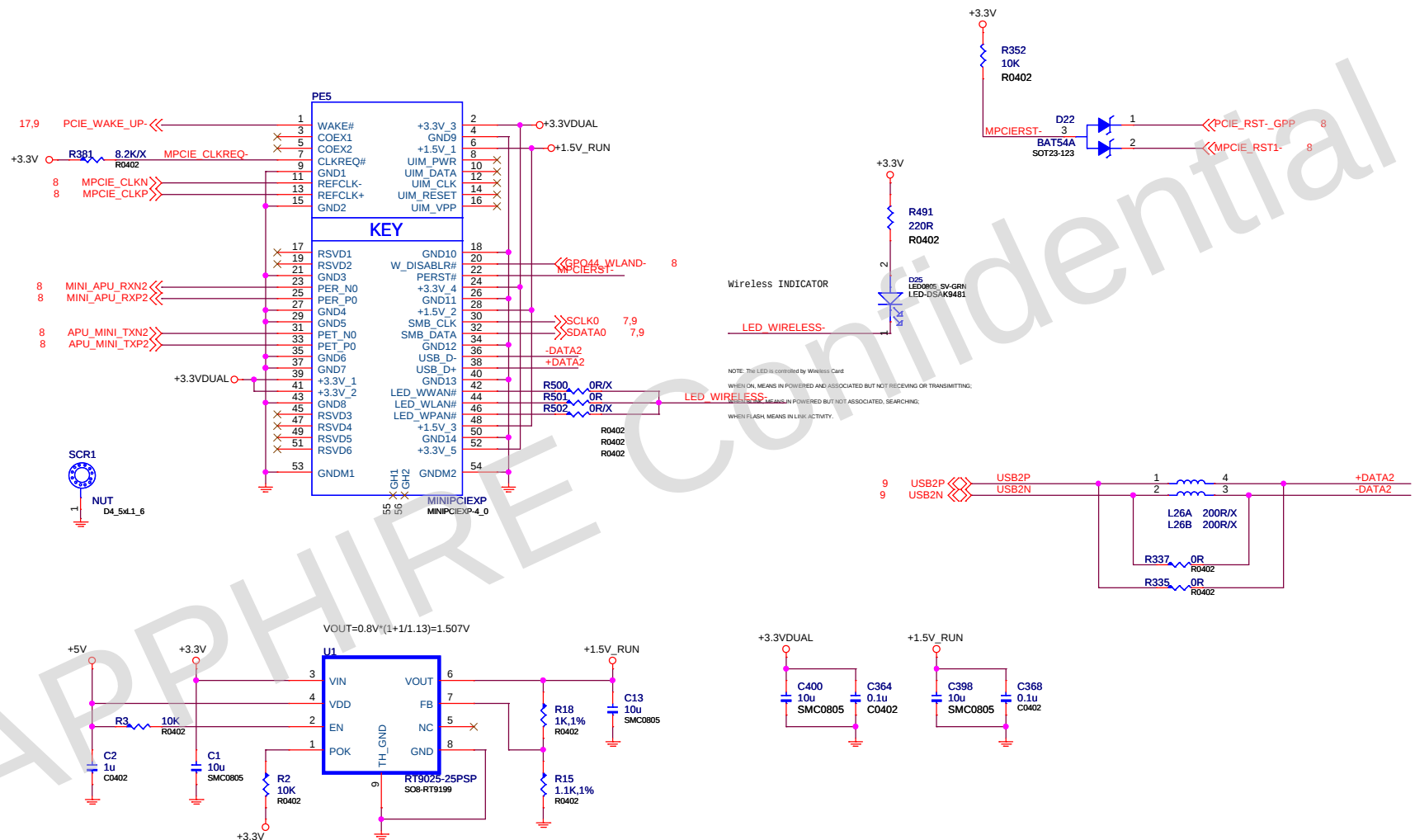
APU_VDDIO_RUN : APU TDC 2.3A

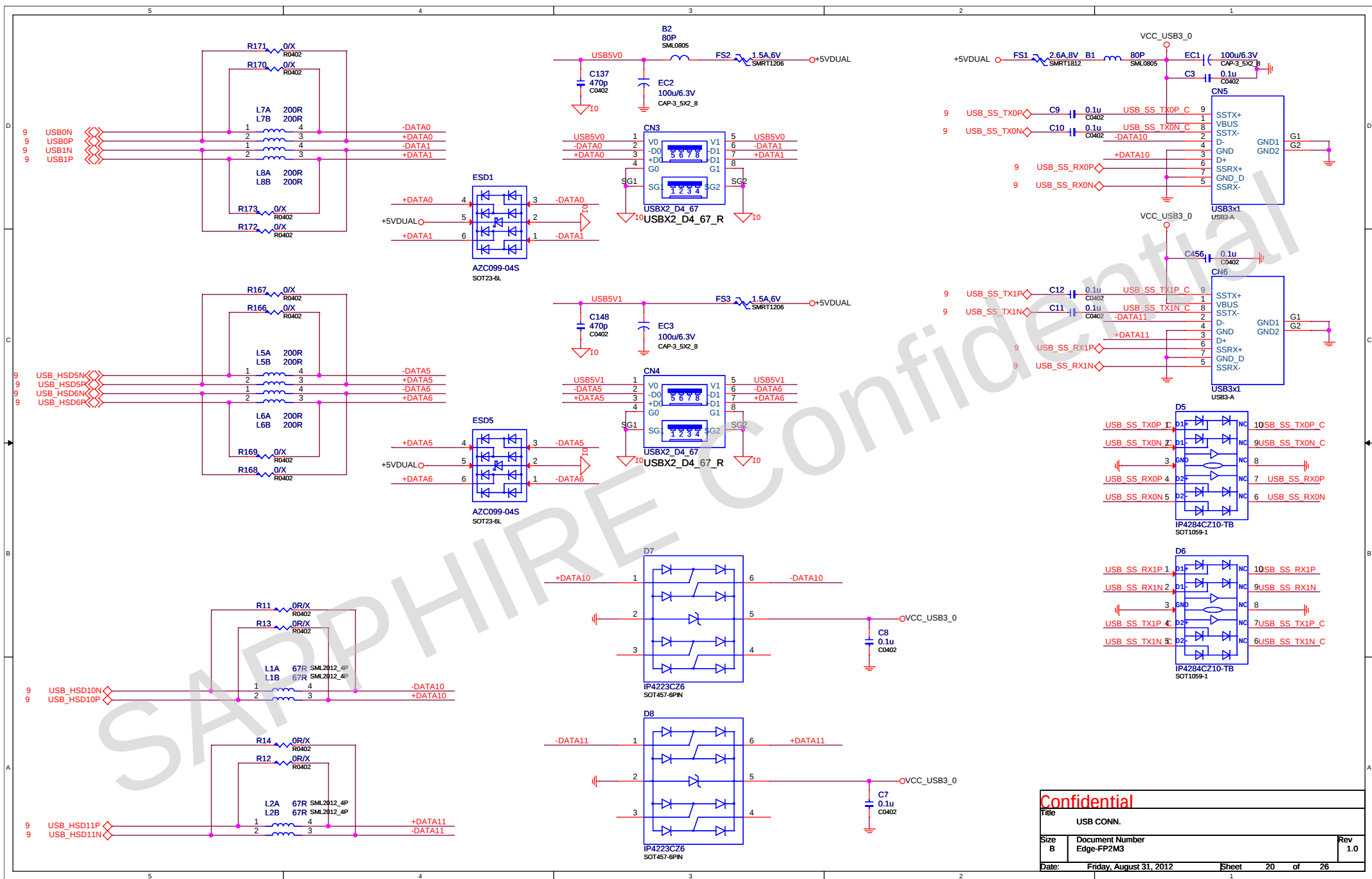


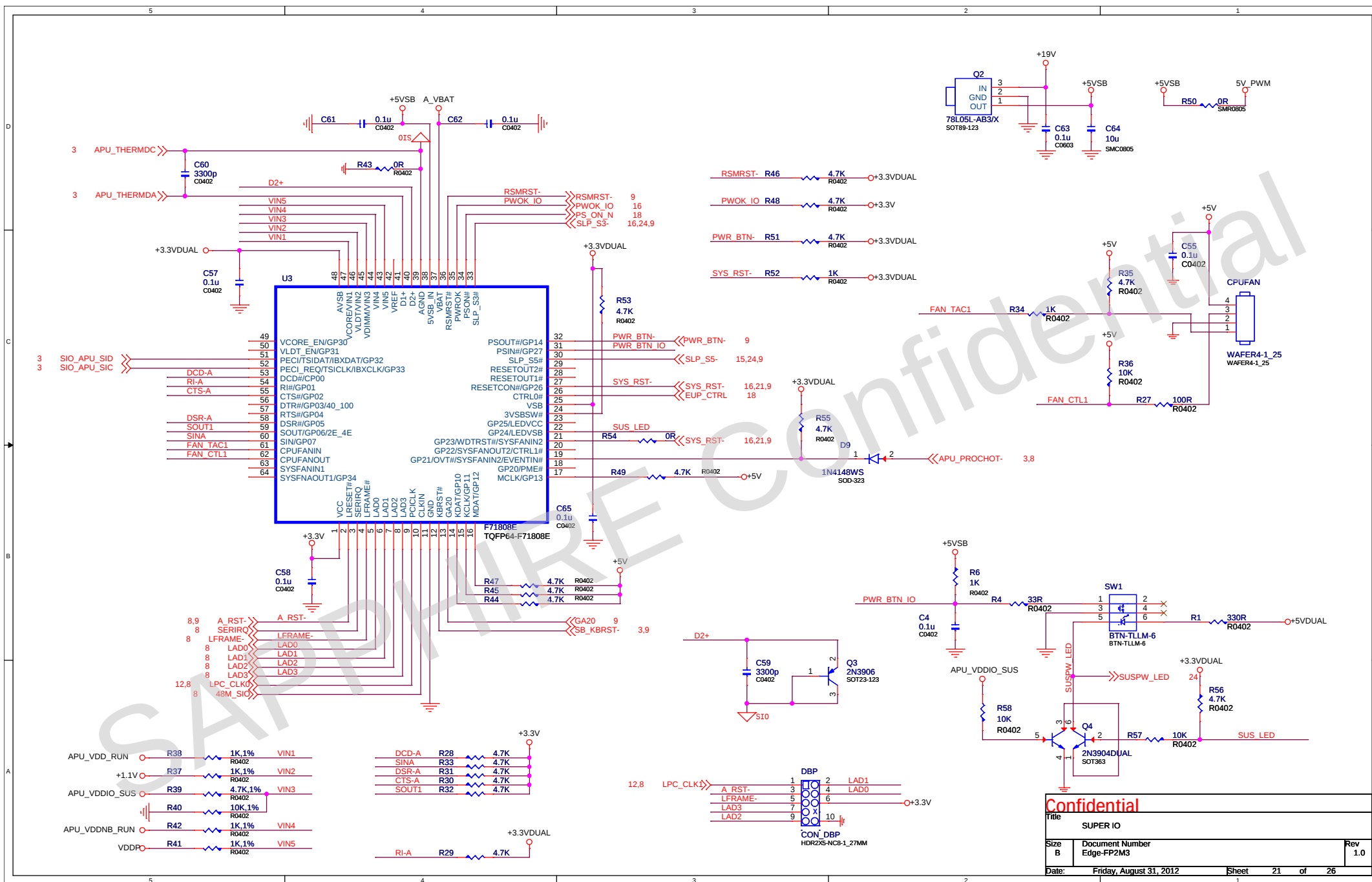
	+1.5V	+1.35V	+1.25V
GPO189	1	1	0
GPO190	1	0	0

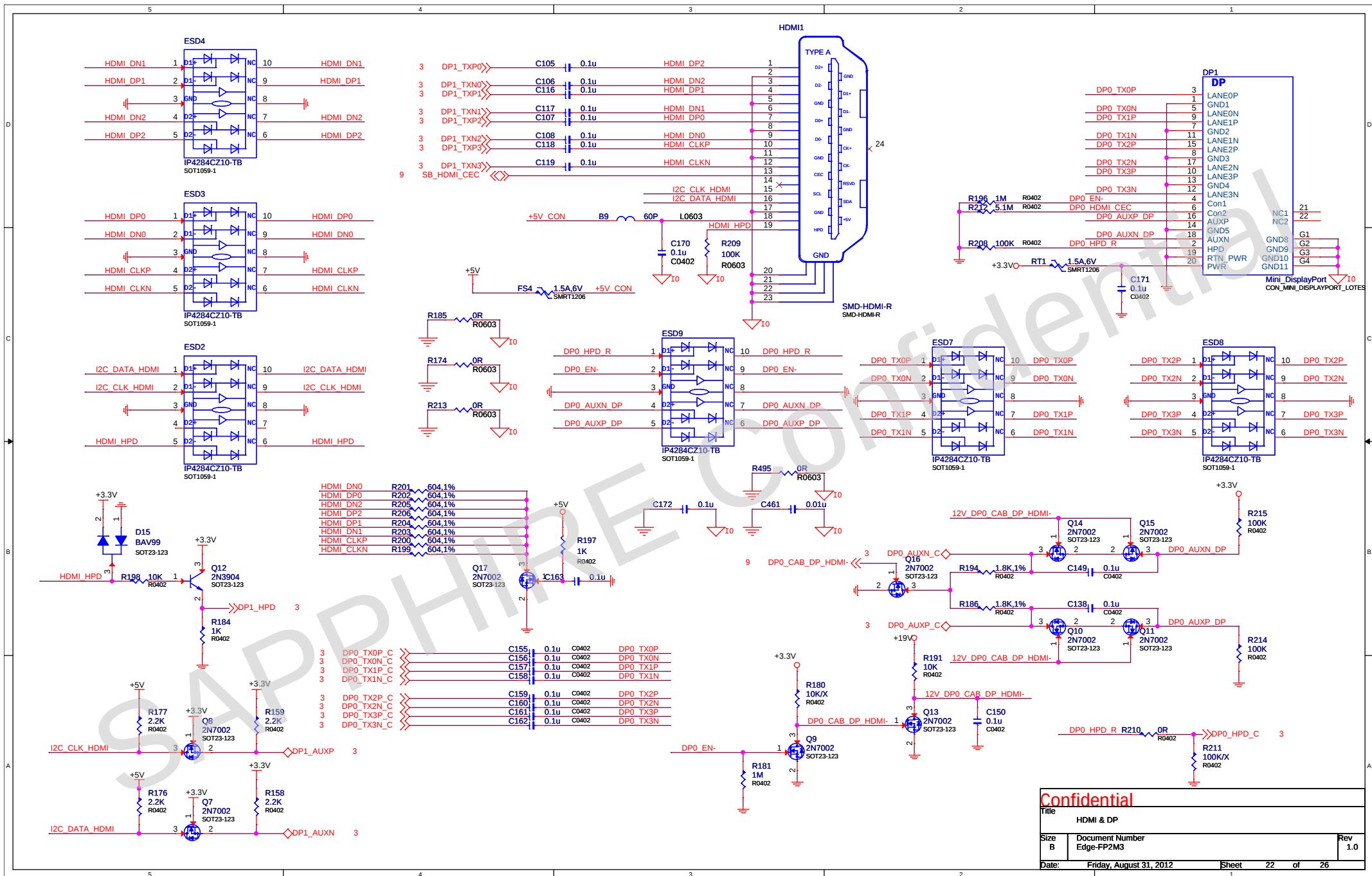












9 AZ_RST_CD >>> AZ1
9 AZ_SDATA_OUT_CD >>> AZ2
9 AZ_SYNC_CD >>> AZ4
9 AZ_BIT_CLK_CD >>> AZ5

9 AZ_SDATA_IN3 <<< R230 33R R0402 AZ3
Place near to CODEC

+3.3VDUAL

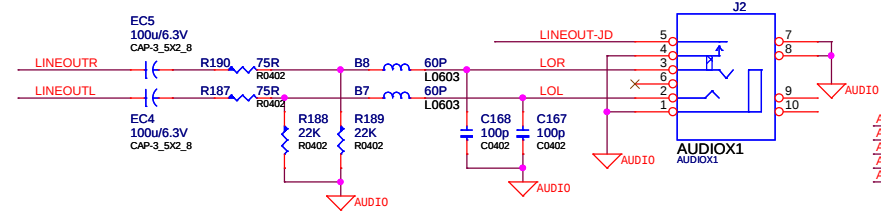
VCC5A

+5VDUAL

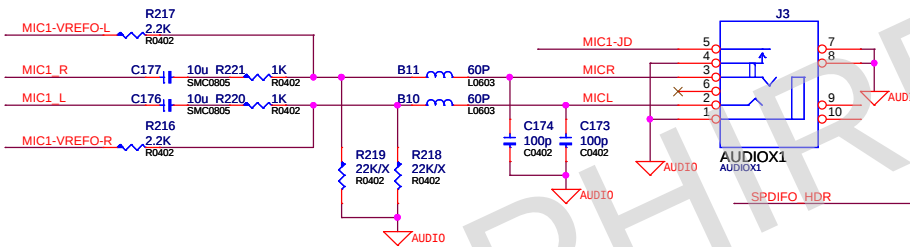
VCC5A

5V_PWM

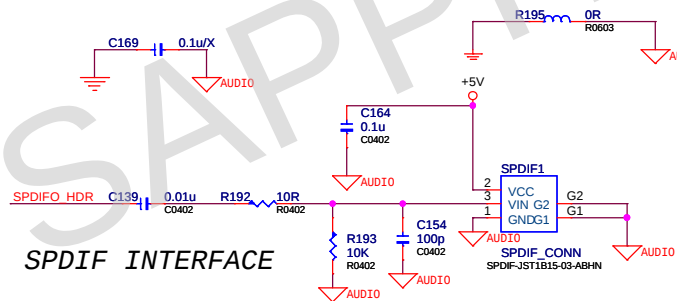
LINE OUT



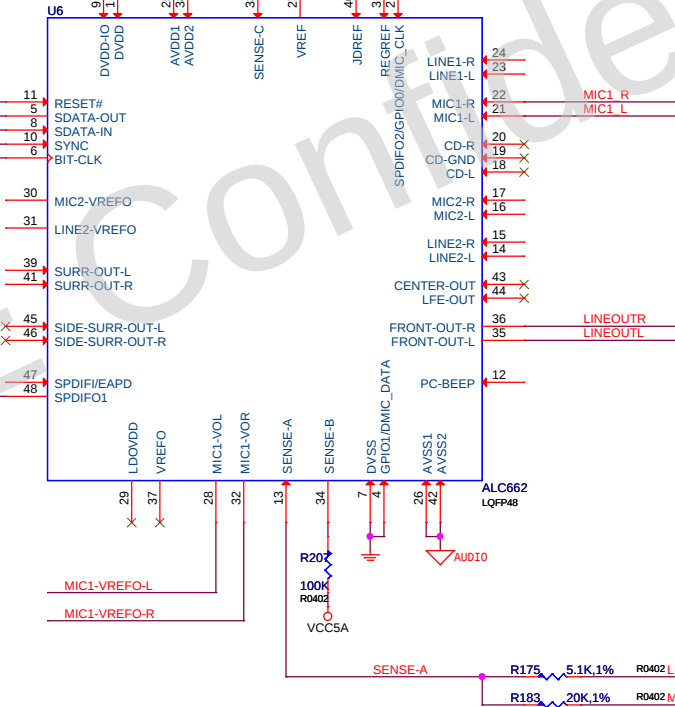
MIC IN



SPDIF INTERFACE

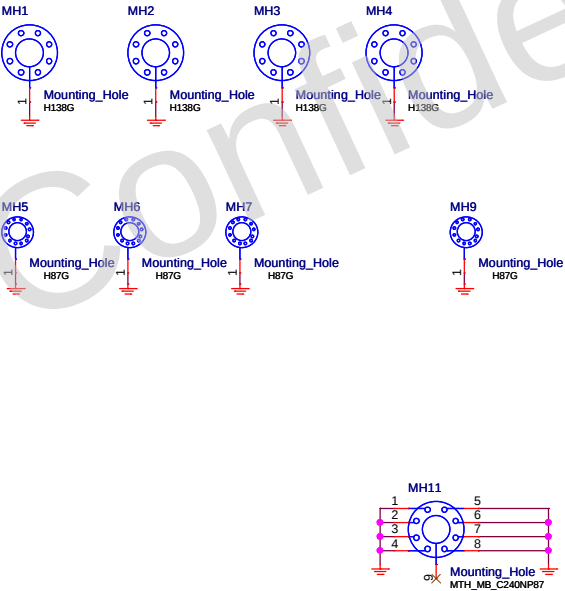


AZ1
AZ2
AZ3
AZ4
AZ5



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