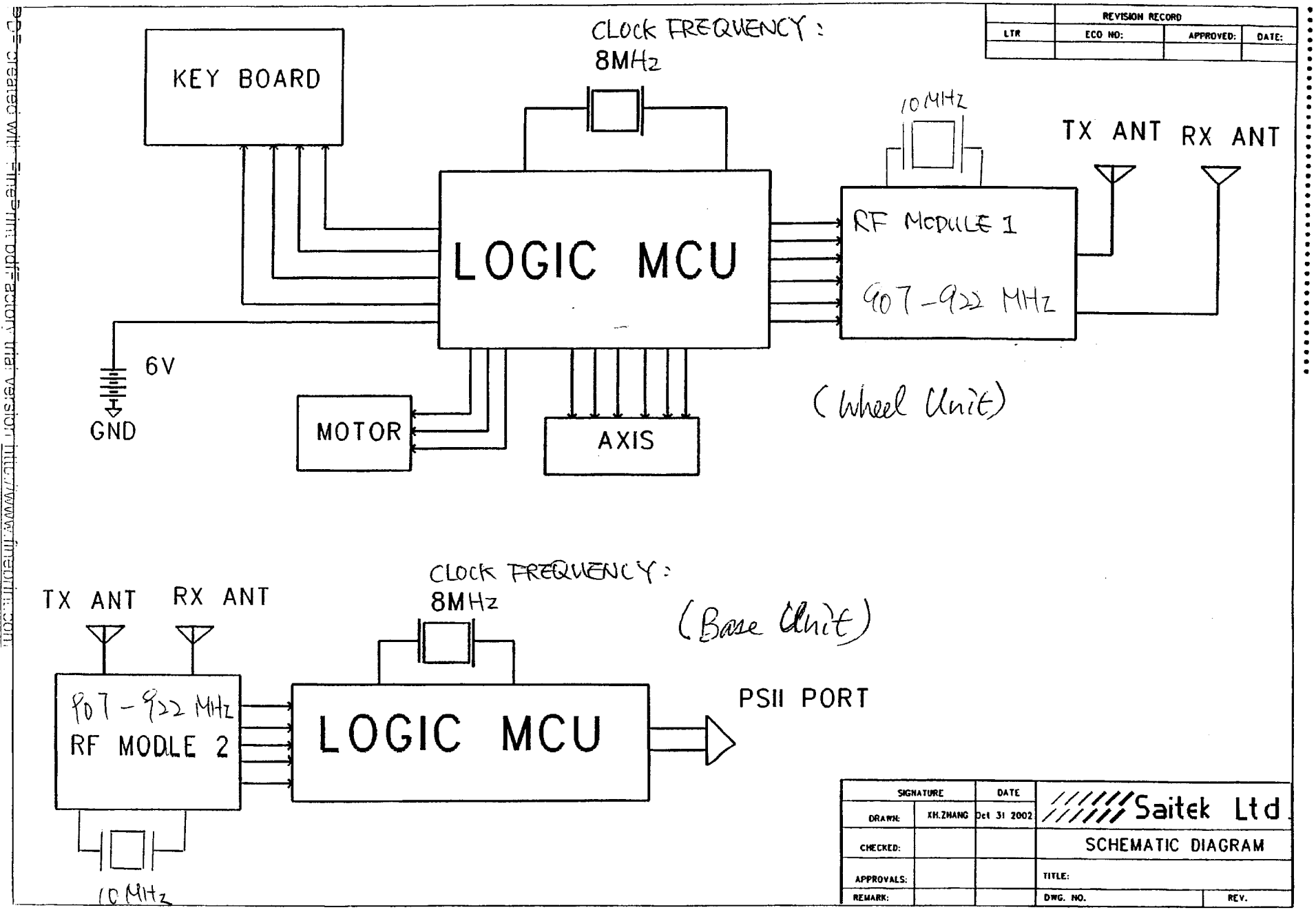
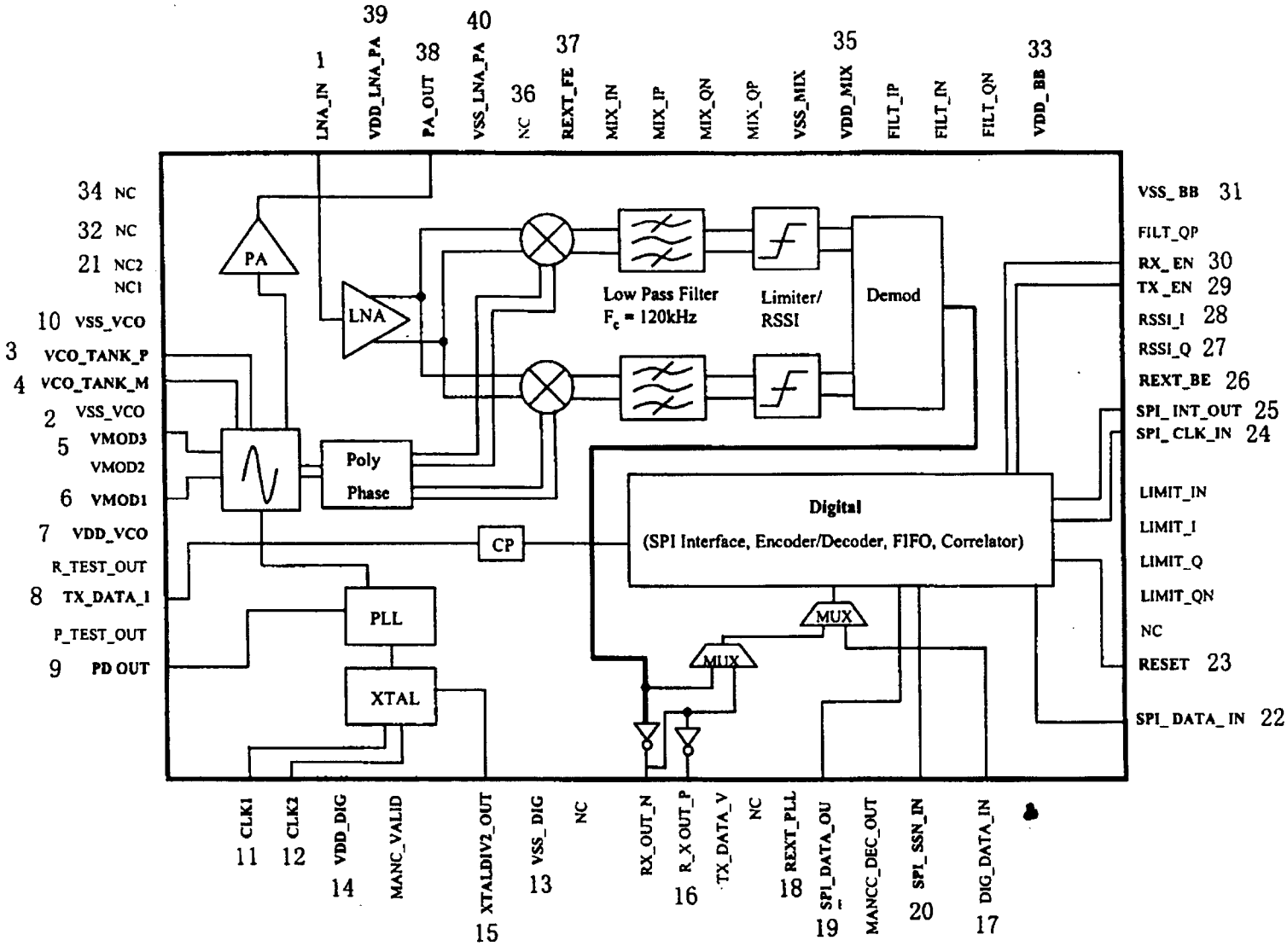


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SIGNATURE		DATE	Saitek Ltd
DRAWN:	XH.ZHANG	Oct 31 2002	
CHECKED:			SCHEMATIC DIAGRAM
APPROVALS:			TITLE:
REMARK:			DWG. NO. / REV.

4.0 Architectural Overview

The basic architecture of the Direct-Conversion Narrowband FSK Transceiver ASIC is shown in Figure 1 below. Bold names represent potential signals for a 32 pin package.



The ASIC main sections are a digital data interface, frequency synthesizer, transmitter (Tx) and receiver (Rx). The digital and frequency synthesizers both interface the Tx and Rx. To complete the transceiver function, several off chip components are required. The off chip components include:

- Crystal (which can be shared with the application's microprocessor – the transceiver will drive the tolerance of the crystal)
- Transmitter and Receiver LC impedance matching and filtering components,
- LC tank circuit for tuning the PLL/VCO
- Capacitors for filtering supply noise
- Passive components for controlling bias points and loop filtering
- Separate transmit and receive anntennas or a tx/rx switch and a single antenna
- Regulated DC power source