

A vertical number line with arrows at both ends. It is labeled with the numbers 2, 3, and 4. A point is marked with a dot and labeled 2.5.



Notes :

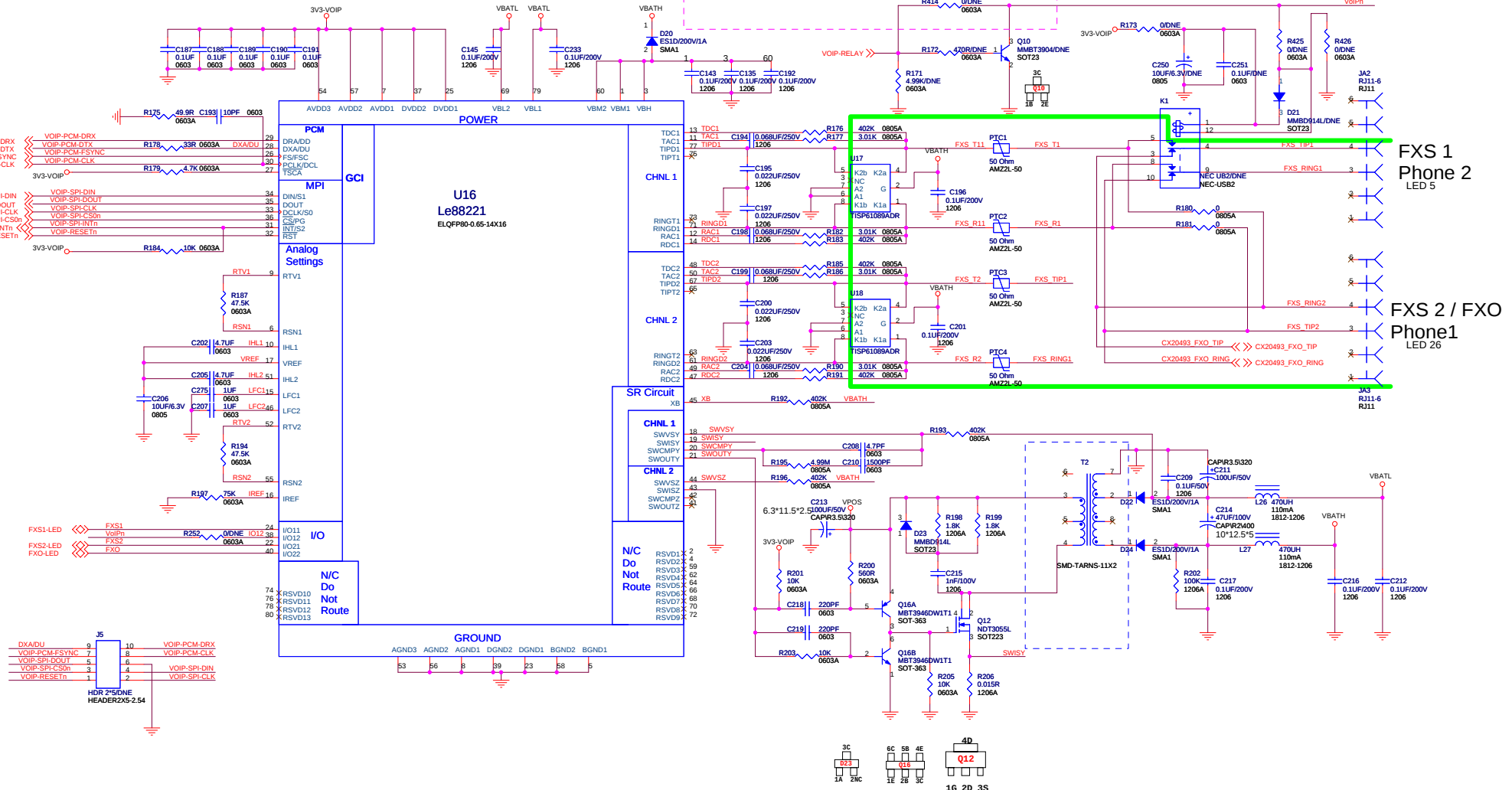
Item	Function	System Power	Logic for net VOIP-RELAY	Logic for pin 12 of K1 relay	K1 Relay path through	Status			Do not populate	Signal paths	Signal to CO or PSTN
						ADSL	FXS	FXO			
1	ADSL+2FXS	ON	No function	No function	No function	Working	Working	No function	FXO ckt and K1 relay	Line 1 - FXS / CH 1 - CPU - AFE - CO Line 2 - FXS / CH 2 -	Data
2	ADSL+FXS+FXO	OFF	No function	No function	pin 3 - pin 4 pin 10 - pin 9	No function	No function	No function	CH 2 of U16 FXS ckt R180, R181	Line 1 - K1 Relay - Line 2 - PSTN	Voice
3	ADSL+FXS+FXO	ON	High	Low	pin 5 - pin 4 pin 8 - pin 9	Working	Working	Working	CH 2 of U16 FXS ckt R180, R181	Line 1 - FXS / CH 1 - CPU - AFE - CO Line 1 - FXS / CH 1 - CPU - FXO - PSTN	Data Voice
4	ADSL+FXS+FXO	ON	Low	High	pin 3 - pin 4 pin 10 - pin 9	No Link	Working	No Link	CH 2 of U16 FXS ckt R180, R181	Line 1 - K1 Relay - Line 2 - PSTN	Voice

VOIP OPTION

2FXS : populate R180,R181,R185,R186,R190,R191
C199,C200,C201,C203,C204
PTC3,PTC4,U18
omit K1,R171,R172,R173,C250,C251,D21,Q10

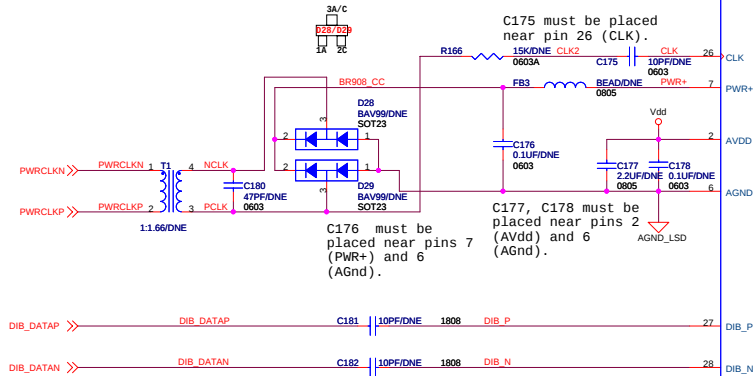
FXS+FXO : populate R171,R172,R173,R425,C250,C251
D21,Q10,K1
omit R180,R181,R185,R186,R190,R191
C199,C200,C201,C203,C204
PTC3,PTC4,U18

Special Note : Do not populate R414 in any case unless the logic of the net VOIP-RELAY can not be controlled by software.



For FXO only

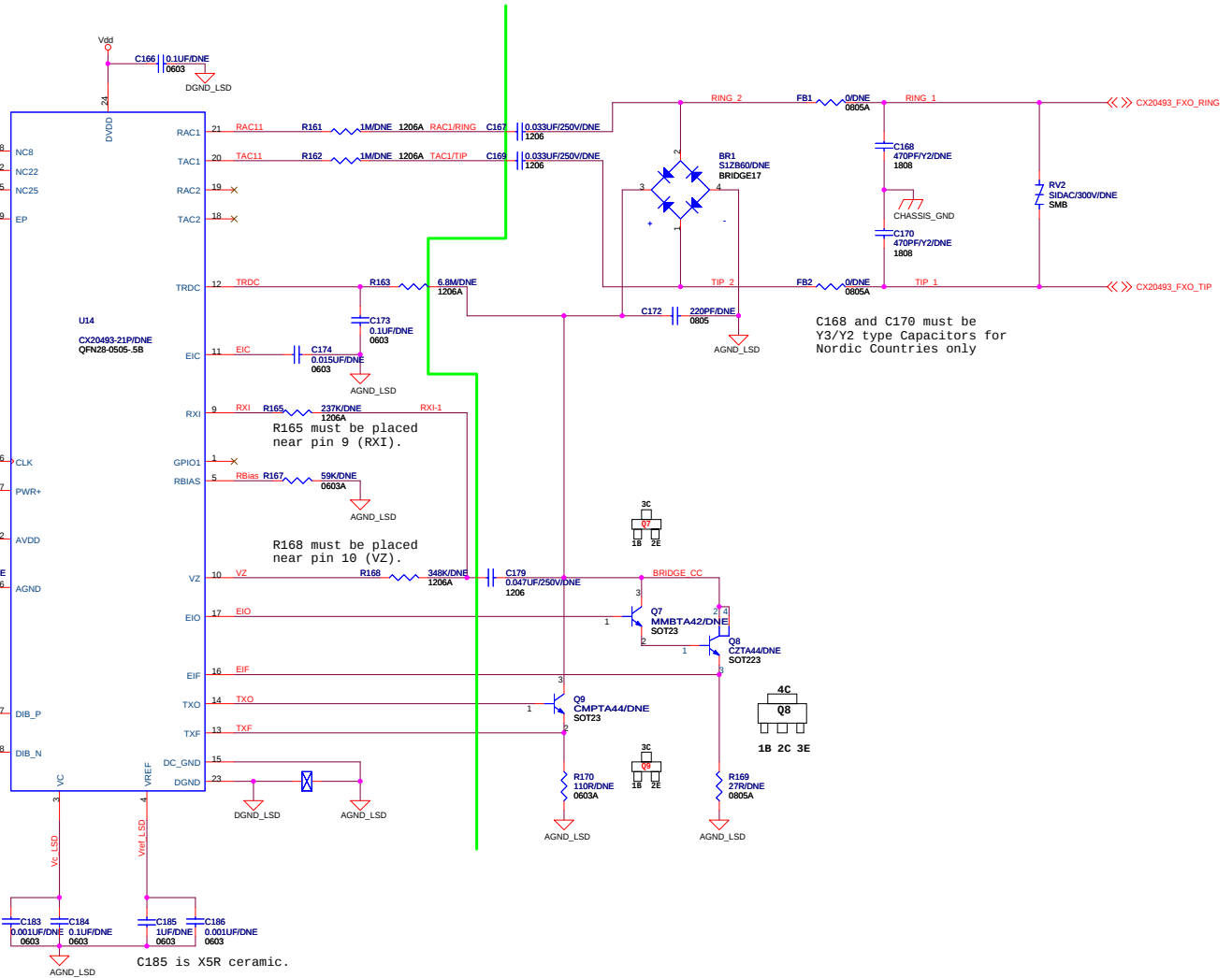
FXO - CX20493



Depending of the design target and DIB length, DIB components can be:
 -C181/C182 10pF
 -C181/C182 47pF (Validation in progress)

C181, C182, C168, and C170, must be Y3 type Capacitors in order to comply with Nordic Countries deviations of IEC60950 2nd and 3rd ed. Y3 type capacitors must also be certified for a 2.5KV impulse test. This must be checked in vendors' specifications (see AVL).

Circuit traces for C181 and C182 should be less than 2 inches.



POWER

DIAG

USB

LAN

Phone 2

Phone 1

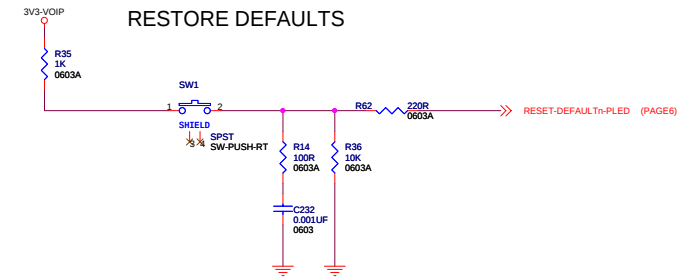
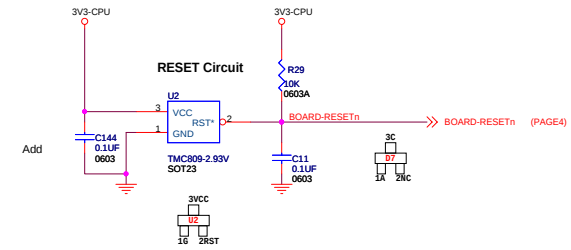
DSL

WLAN

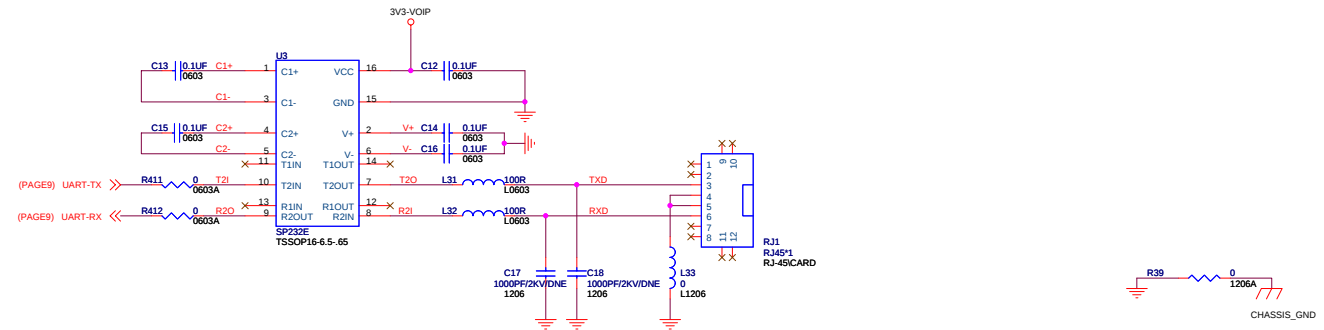
VoIP LED OPTION

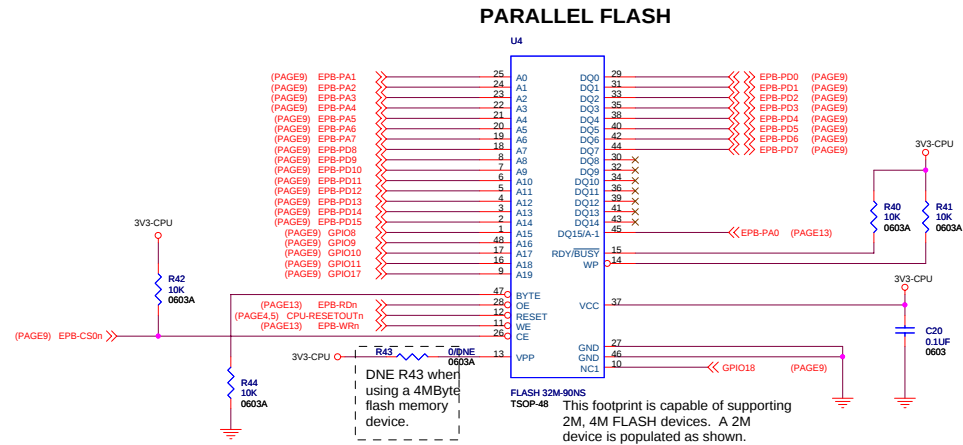
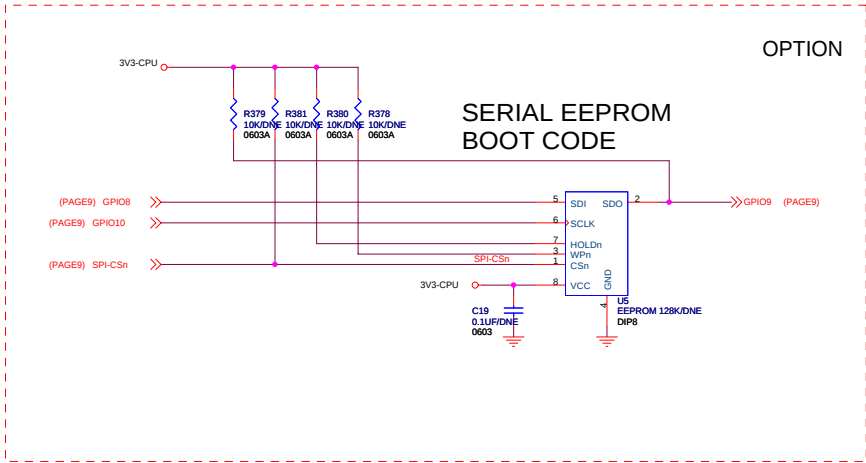
2FXS : populate R27,R331 / omit R332,R432

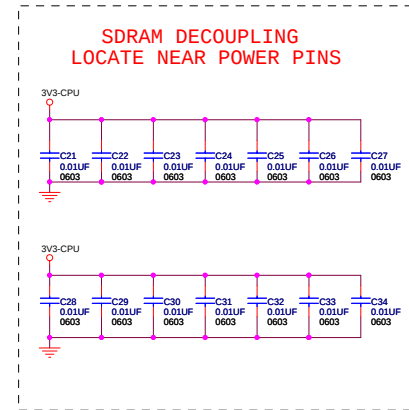
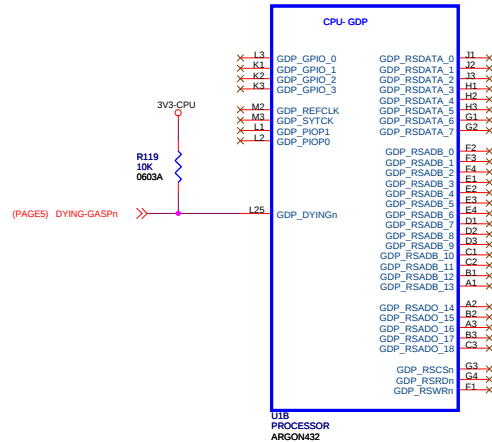
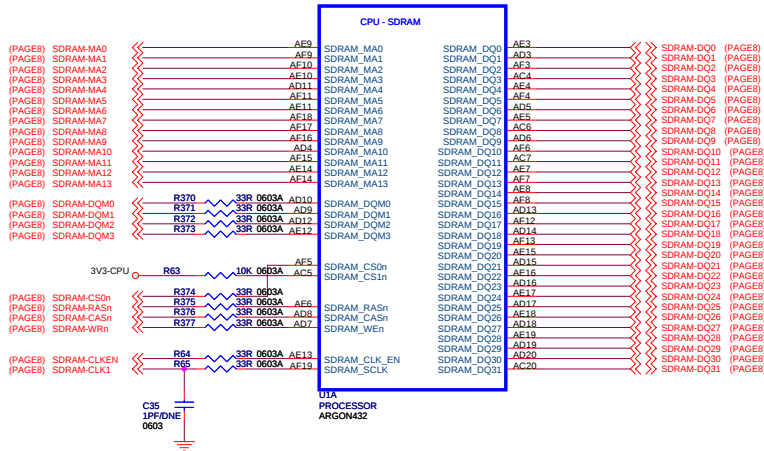
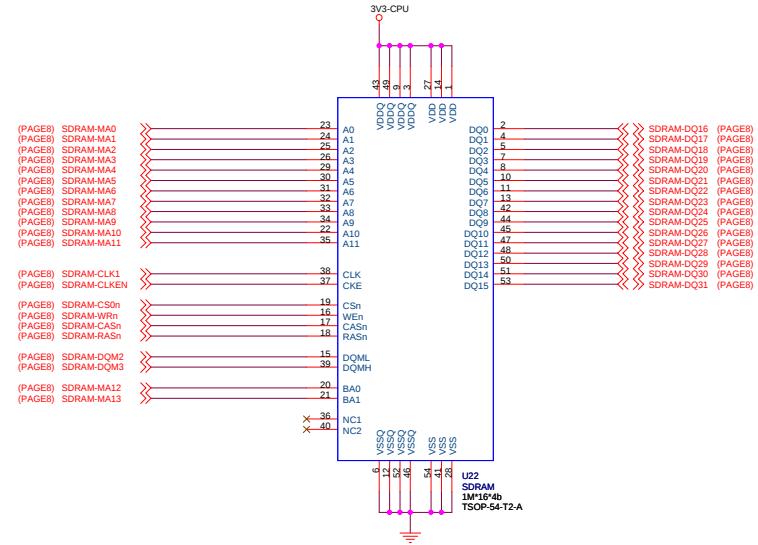
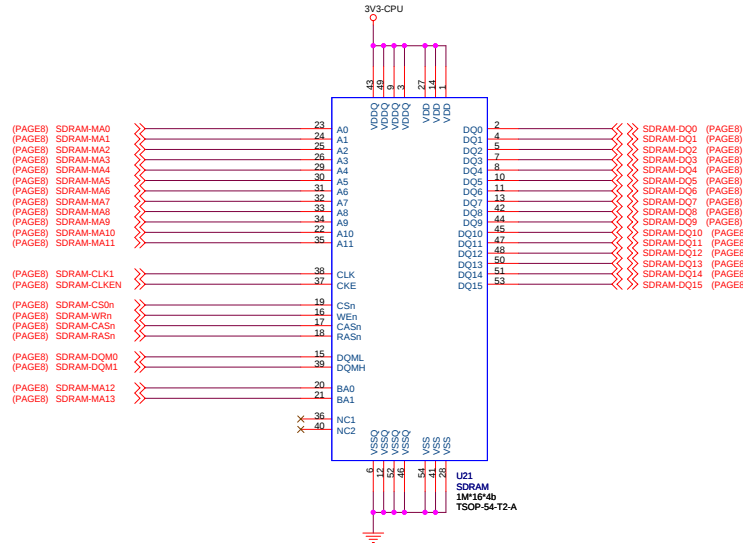
FXS+FXO : populate R332,R432 / omit R27,R331

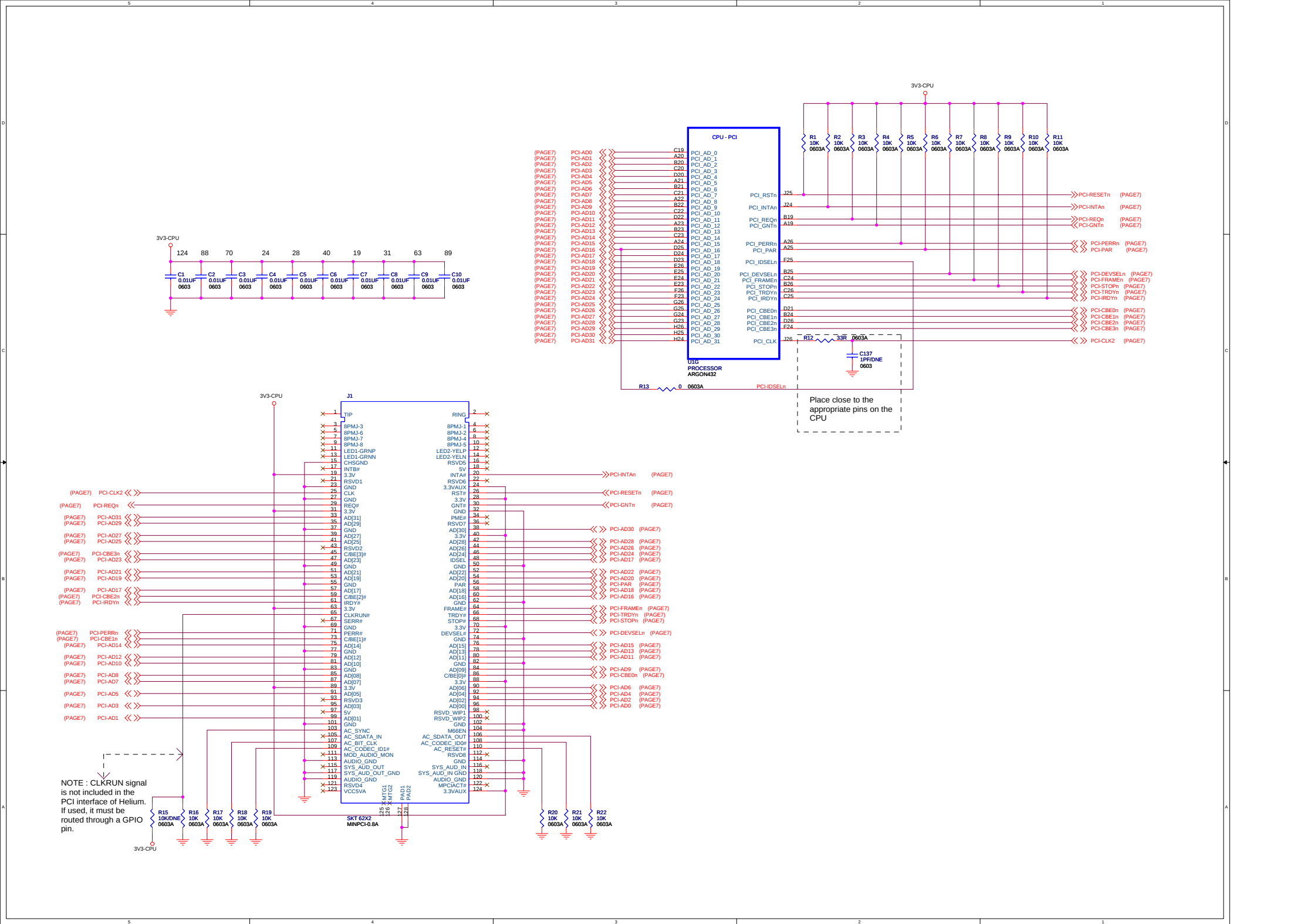


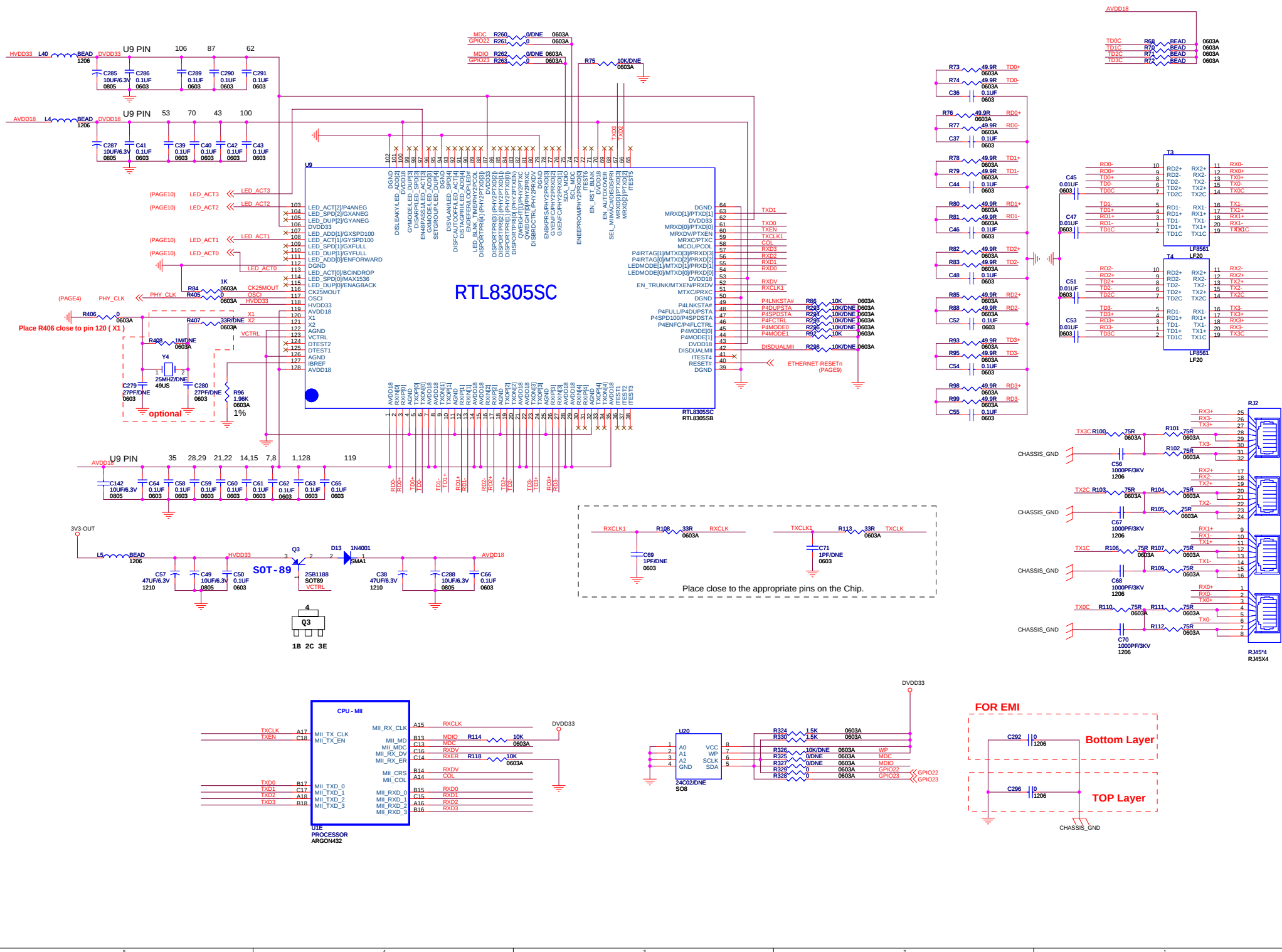
CPU SERIAL PORT

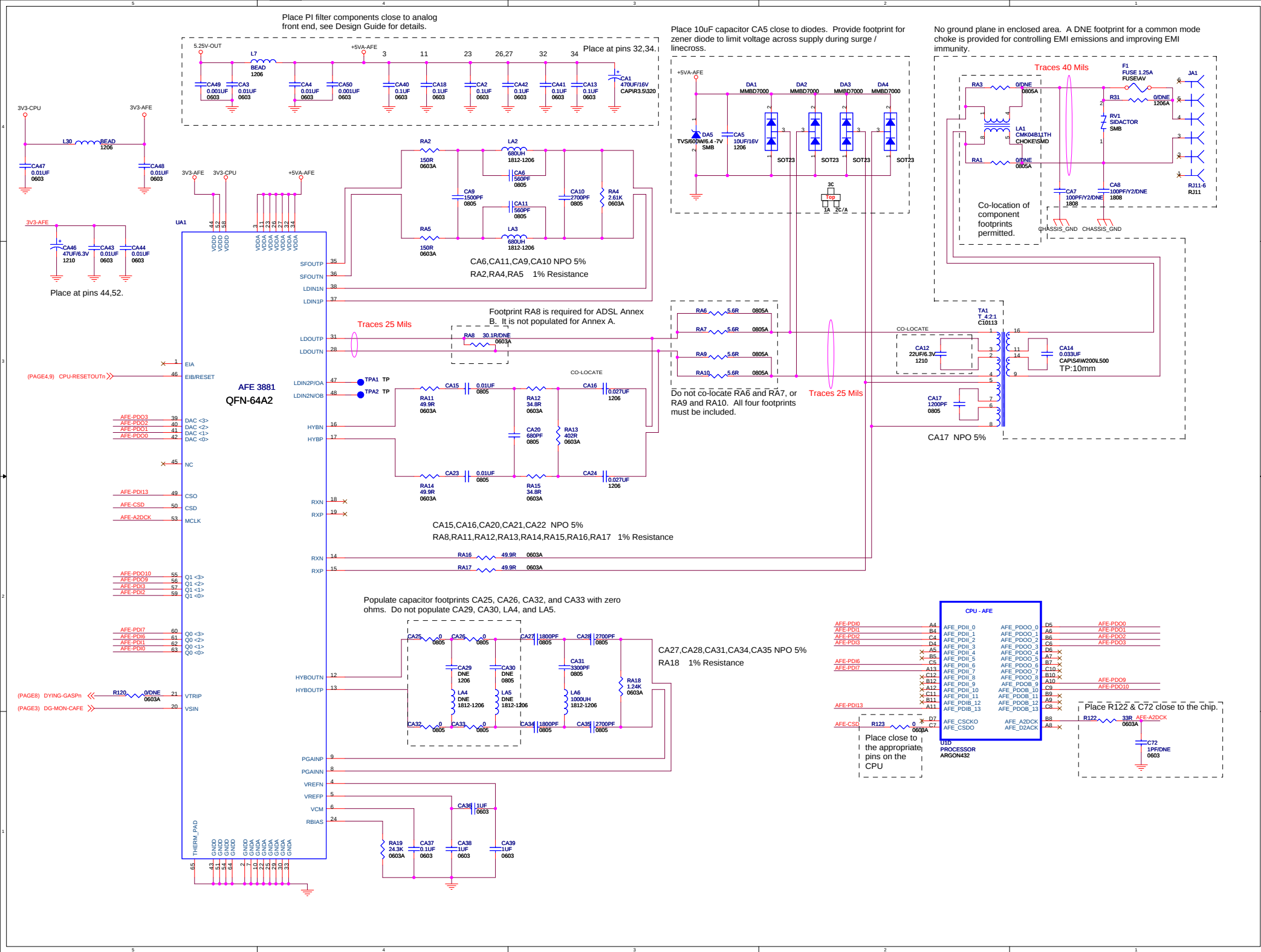


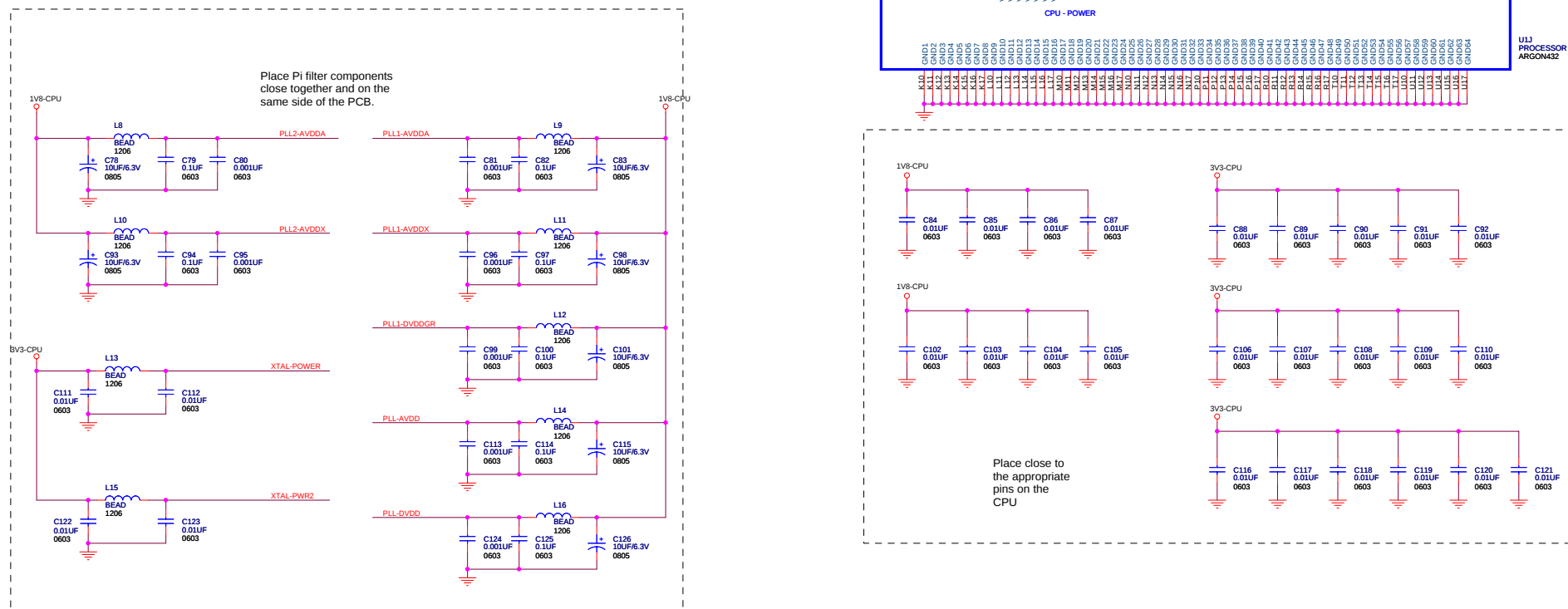
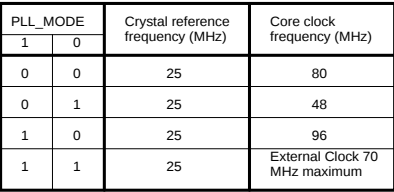








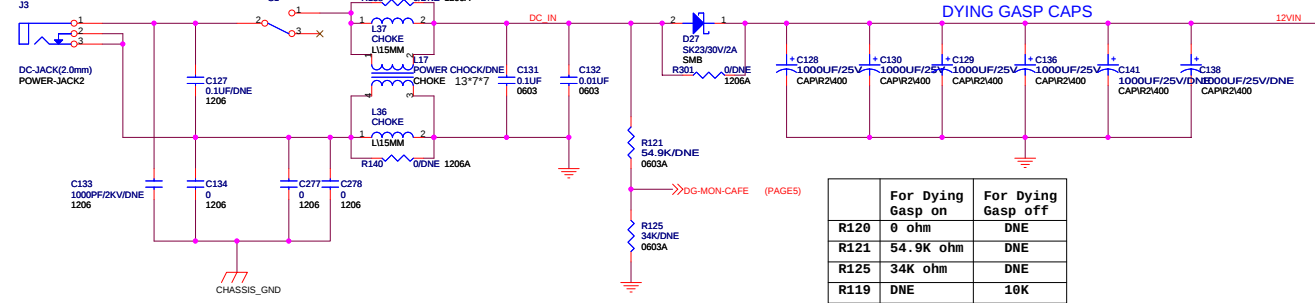




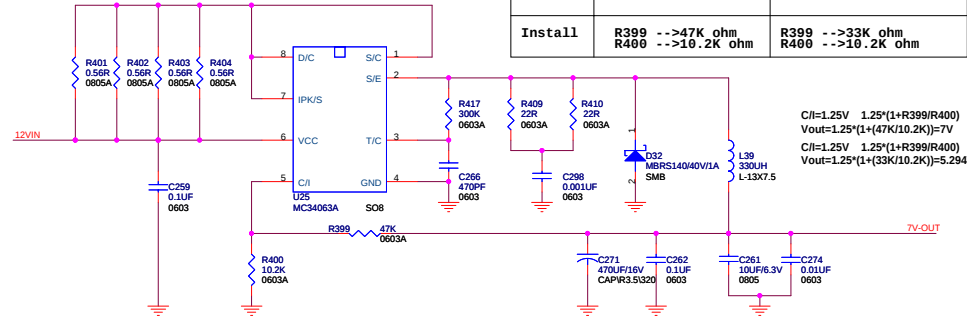
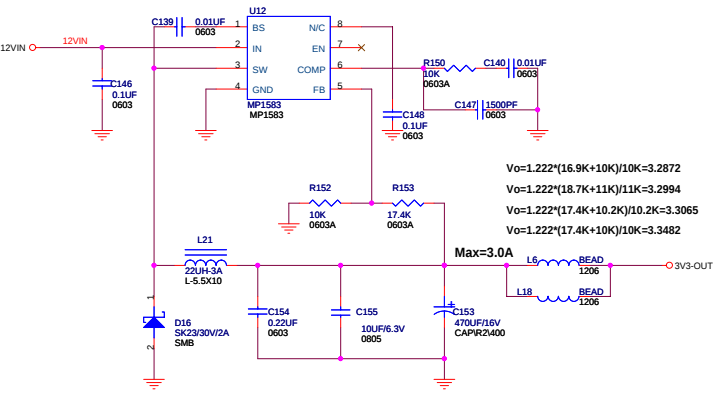
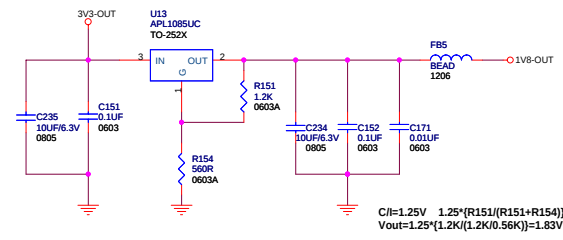
12V1.25A DC INPUT

POWER SYSTEM

DYING GASP CAPS

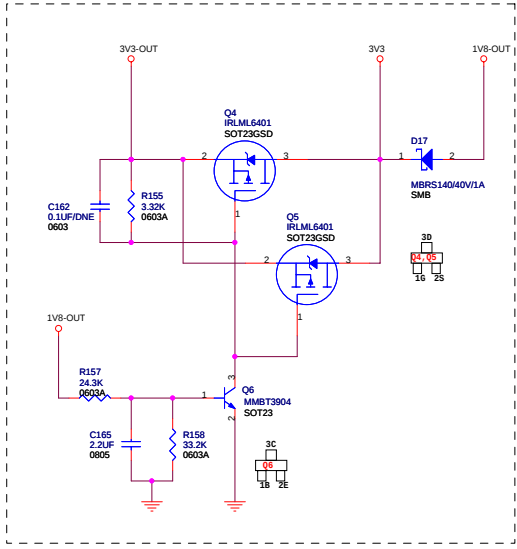


	For Dying Gasp on	For Dying Gasp off
R120	0 ohm	DNE
R121	54.9K ohm	DNE
R125	34K ohm	DNE
R119	DNE	10K



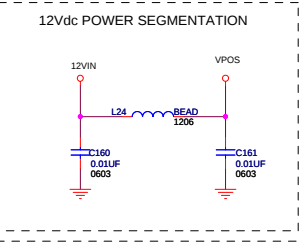
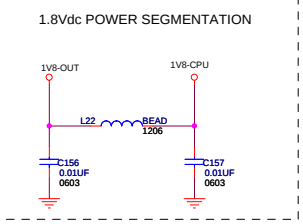
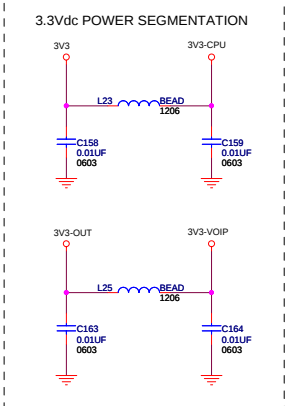
	U25 Power Out -->7V	U25 Power Out -->5.25V
Install	R399 -->47K ohm R400 -->10.2K ohm	R399 -->33K ohm R400 -->10.2K ohm

Power sequencing circuitry. Place components close to 1.8V regulators. Please refer to application note DO-400569-AN.

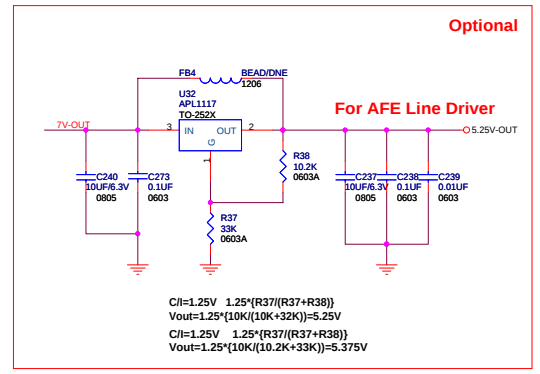


Place Pi filter components close together and on the same side of the PCB.

3.3Vdc POWER SEGMENTATION

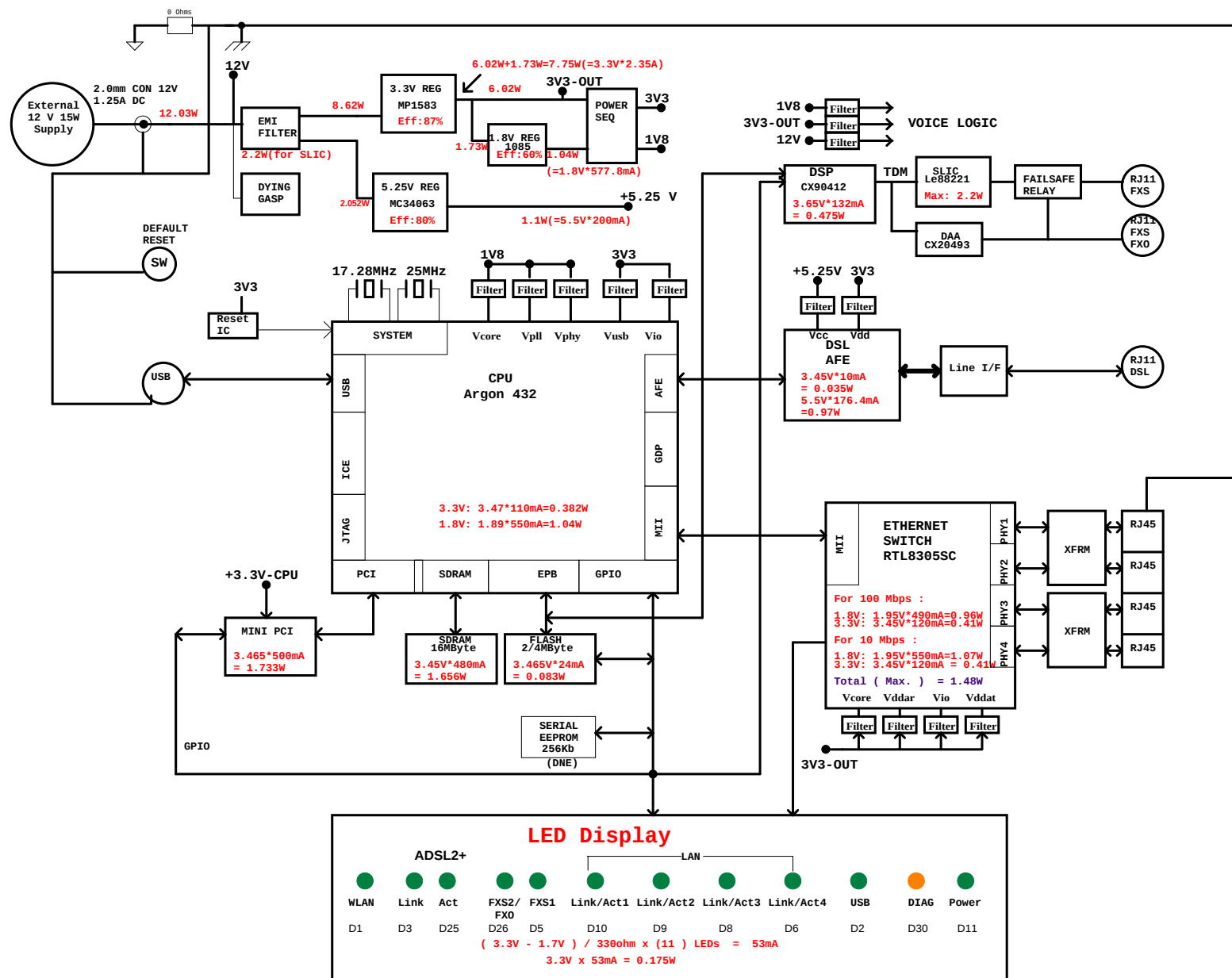


Optional



CHASSIS GROUND





VDR824G Schematic

Table of Contents

Sheet	Description
1	Revision History
2	Block Diagram
3	POWER 5.25V/3.3V/1.8V
4	CPU CLOCKS/JTAG/POWER
5	AFE BAZ3881
6	Ethernet / RTL8305SC
7	MINI PCI CONNECTOR
8	SDRAM
9	MEMORY / EEPROM / USB
10	LEDs / Reset/Serial Port
11	CX20493/DNE
12	LE88221/2FXS
13	CX90412-11