3. Circuit Description

In this section, the description for functional blocks of each PBA is explained. Though NeoTel-811 consists of independent PBA's such as main board, keypad, and sub-key board, PBA's are connected via various cables with one another. Main board is connected to keypad board with 30-pin FPC cable. Keypad board is connected to LCD module with 16-pin connector, and keypad board is connected to sub-key board with 6-pin cable. Main board adopts a pair of 60-pin connectors to connect with CDMA module. CDMA module consists of two boards, which are CDMA baseband module and RF module. CDMA baseband module and RF module are inter-connected with 60-pin connector.

3.1 Main Board

The block diagram of a main board is shown in Figure 3. Each block is explained in the subsequent sections. The speaker phone block is included in the main board, however components are not assembled currently. It can be modified according to the customer 's request.

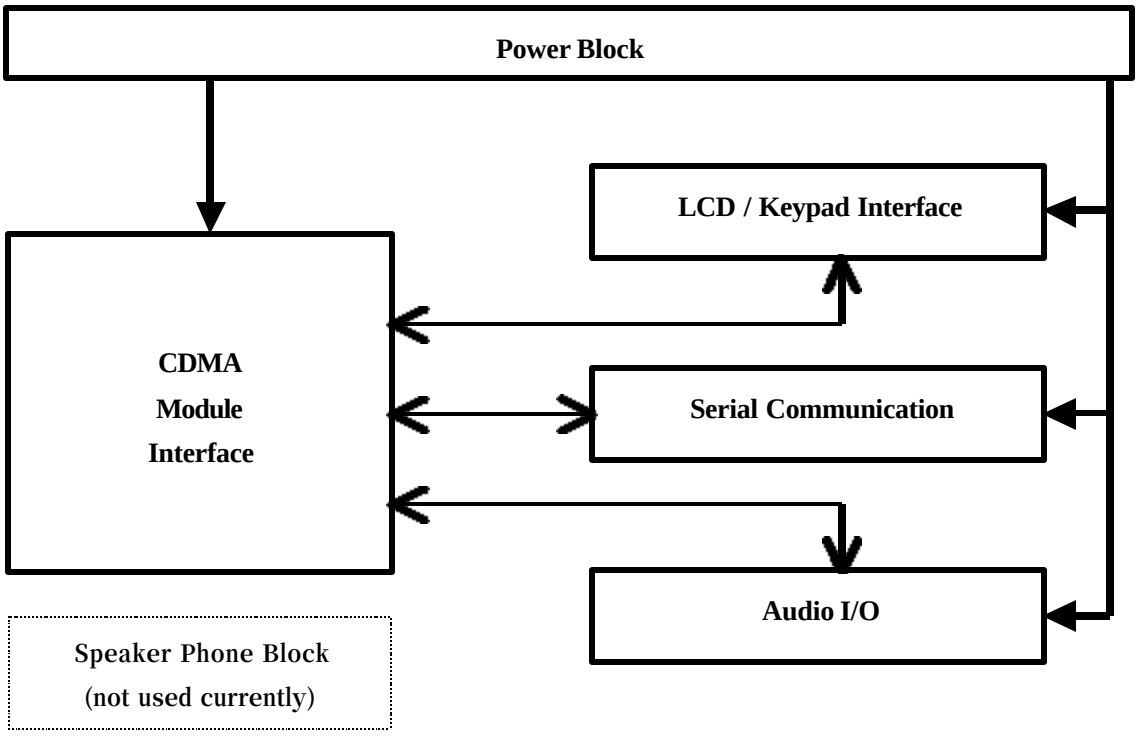

Figure 3. 1. Block Diagram of Main Board.

3.1.1 Power Block

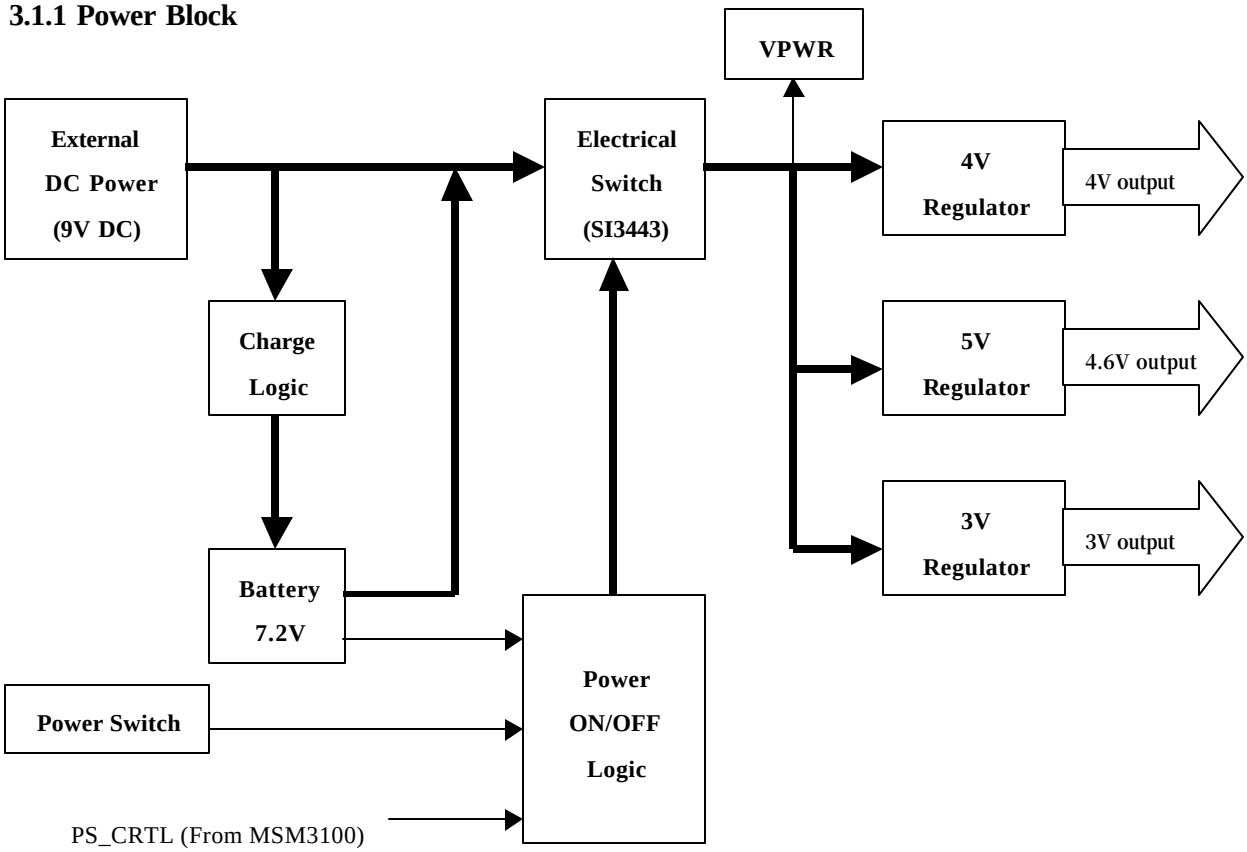

Figure 3.2. Power Block Diagram of Main Board.

The block diagram of a power block is shown in Figure 4. Main board supplies all the power used in NeoTel-811. Main board uses DC 9V/1.5A from SMPS as a main power and 7.2V battery as a backup power. The power block consists of charging circuitry, power on/off circuitry, VPWR, 4V output, 4.6V output, and 3V output.

Battery is rechargeable Ni-Cd cells with 7.2V/900mAh capacity. Battery can be replaced to Ni-MH cells with 7.2V/1600mAh in order to enhance time for usage. Battery is continuously charged when the SMPS is plugged in AC voltage regardless of the status of power switch. If failure occurs in the main power from SMPS, the power is changed to backup battery.

The power switch has three modes of operation, which are OFF, Powering OFF, and ON. When the power switch is on ON state, PS_CTRL signal from MSM3100 controls terminal to ON state. When the terminal operates with battery, MSM3100 controls PS_CTRL signal to turn out the power of terminal in case of failure of battery power.

VPWR is used for circuitry of serial communication with PC. The regulator for 4V output is used for CDMA module. The regulator for 46V output is used for audio interface and LCD/LED driving logic.

Finally, the regulator for 3V output is used for power logic driving and serial communication line driving.

3.1.2 LCD / Keypad Interface

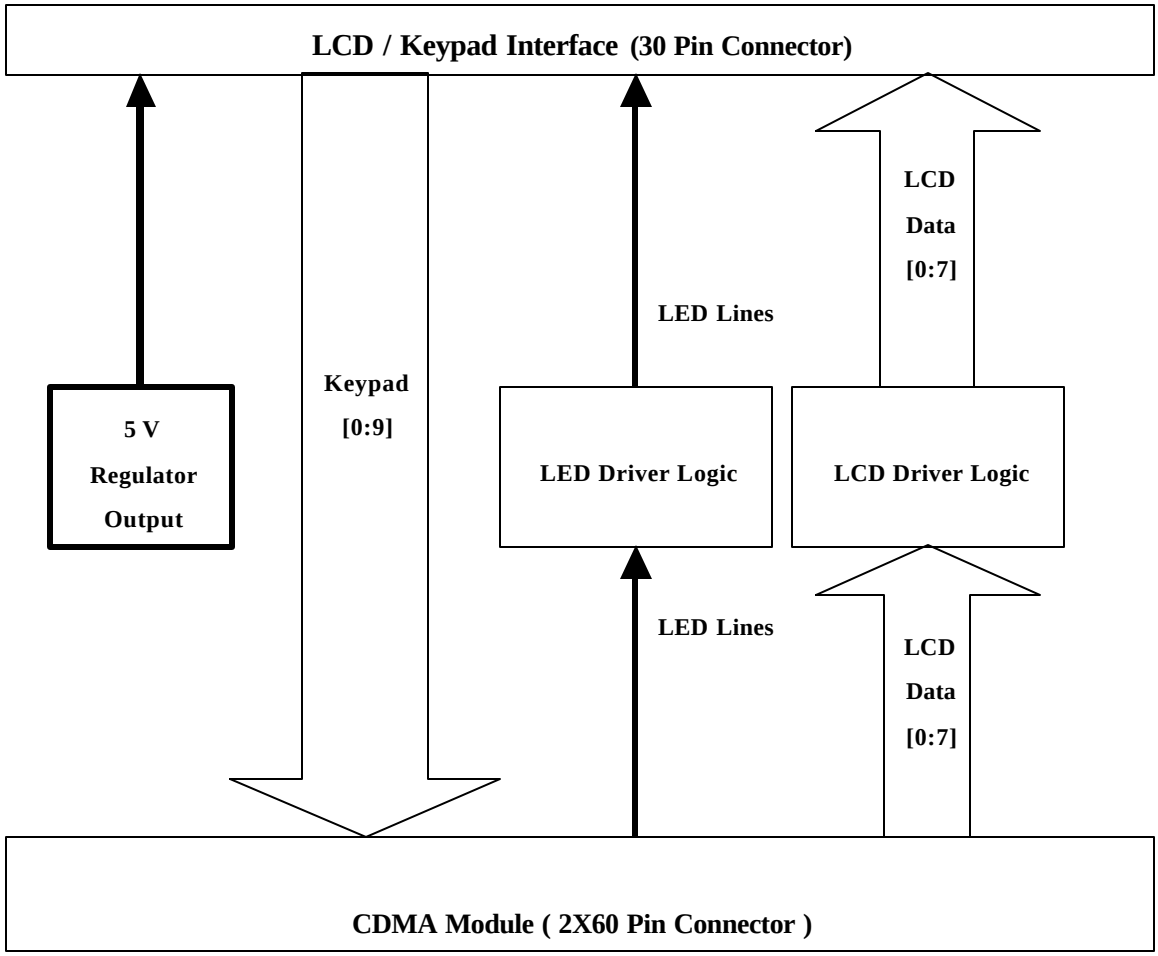

Figure 3.3. Block Diagram of LCD / Keypad Interface.

The block diagram of LCD/Keypad interface is shown in Figure 5. Though LCD/keypad interface has no relation with CDMA module, it controls almost UI (User Interface) functions.

LCD/keypad interface consists of 30 signals for keypad, sub-key board and LCD. The signals comprise 10 lines of keypad data, 7 lines of LED drive, 3 lines of LCD drive, and 8 lines of LCD display data.

The input power for LCD/keypad interface is 4.6V from 5V regulator in power block of main board. MSM3100 senses key input using key-sense block and GPIO signals. The control signals for LED's are as follows: two lines for RSSI level, two lines for battery level, and one line for message indication. The LED for RSSI level shows three levels of signalstrength such as green, yellow, and red. The LED for battery level also shows three levels of remaining battery level such as green, yellow, and red. The LED for message

indication is ON when new message is received. All the LED's are controlled by LED driver logic on main board.

Three lines of LCD driving signal and one line of LCD backlight enable line are directly controlled by MSM3100 through LCD/keypad interface on main board. Eight lines of LCD display data are controlled by LCD driving logic pulled-up to 4.6V on main board. The enable line for LCD backlight can be controlled to ON/OFF by electric switch on keypad board.

3.1.3 Serial Communication : UART, DM

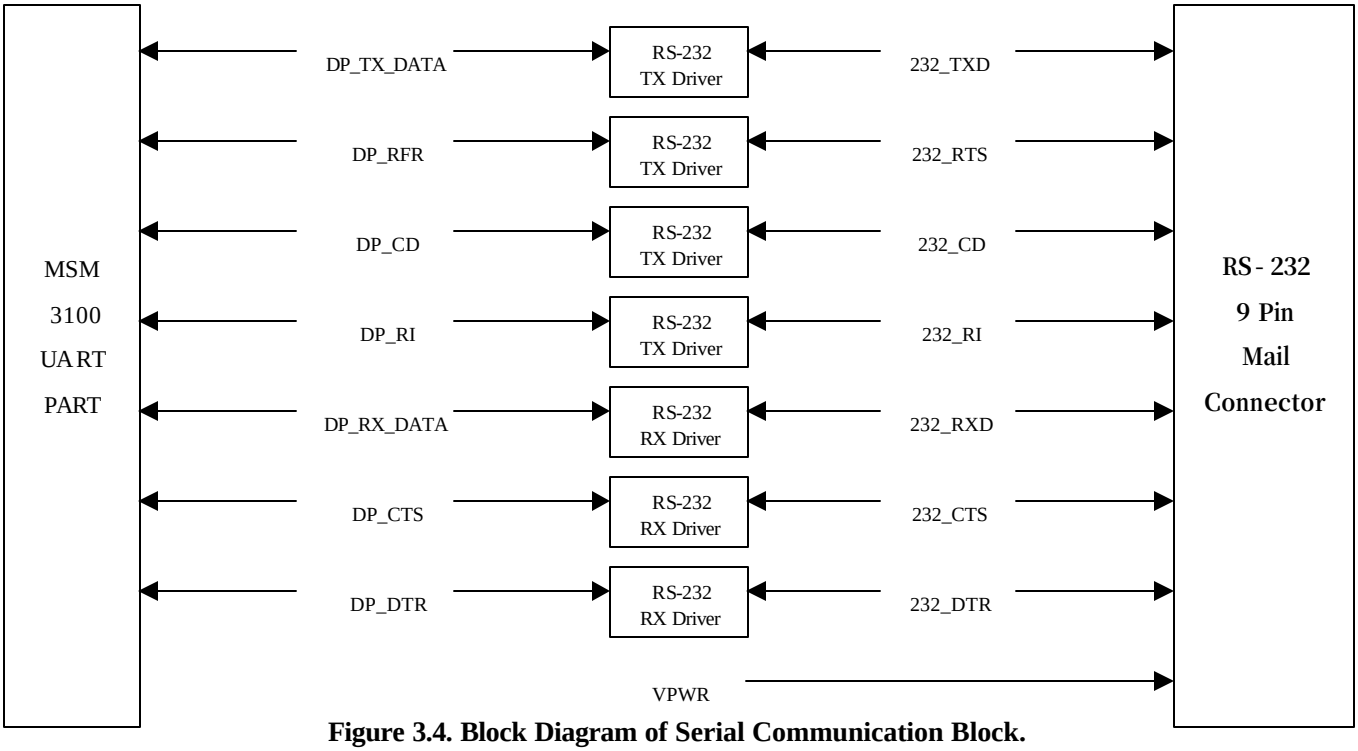

Figure 3.4. Block Diagram of Serial Communication Block.

The block diagram of serial communication block is shown in Figure 6. The serial communication block provides interface for data communications, which uses UART part inside MSM3100 and some GPIO signals. This block is designed to convert logic signals inside MSM3100 to RS-232 level, which can be connected to PC through RS-232 9-pin connector.

3.1.4 Audio Input/Output: Microphone and Earphone Interface, Speaker Phone Interface

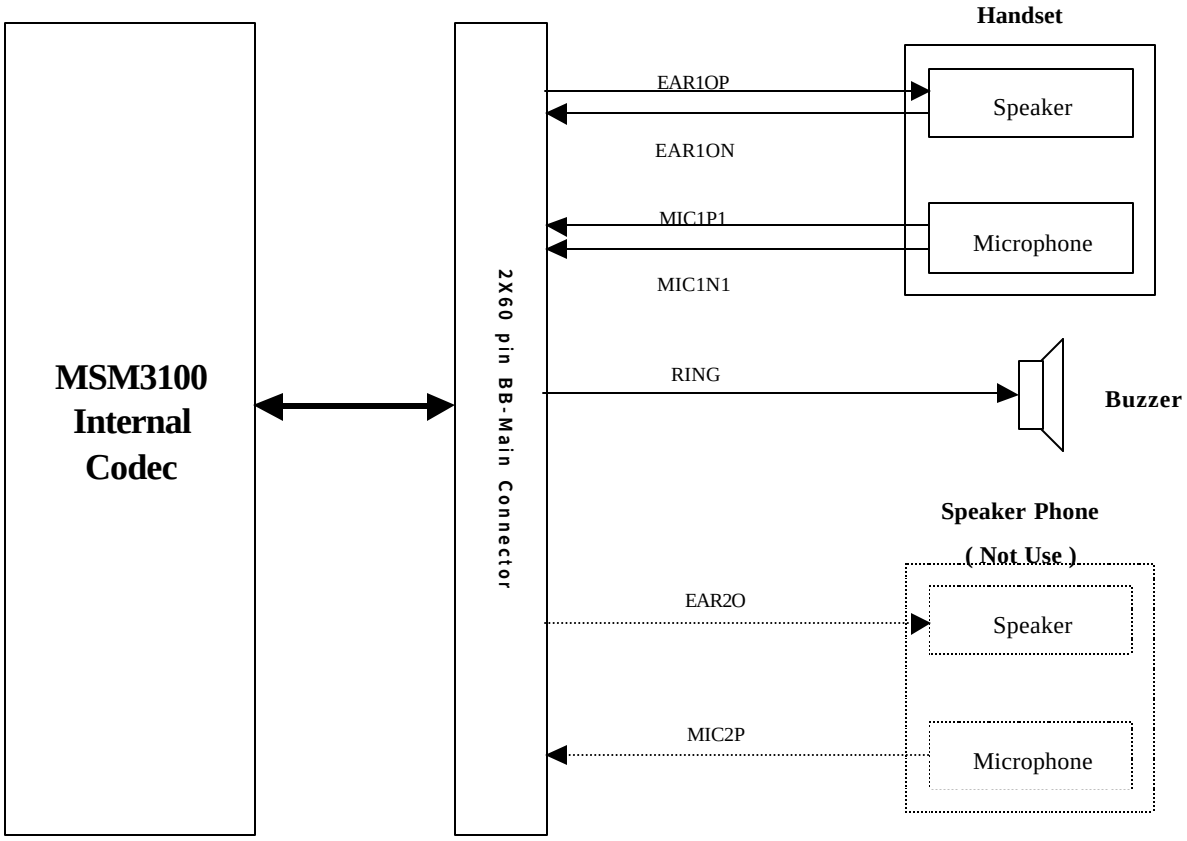

Figure 3.5. Block Diagram of Audio Input/Output.

The block diagram of audio input/output is shown in Figure 7. This block interfaces vocoder block and internal Codec inside MSM3100, which enables the user's communicating with handset. The audio I/O block interfaces internal Codec inside MSM3100 with microphone and speaker in the handset. The speaker-phone function is implemented in circuitry, however the components are not assembled currently. The speaker-phone function can be provided in case of customer's request. The RING signal drives buzzer using a ringer signal from DTMF tone generator inside MSM3100.

3.1.5. Keypad, Sub-key and LCD

Keypad, Sub-Key LCD PBA module ,
Main Board . Main Board
, Keypad Sub-key Board LCD
.

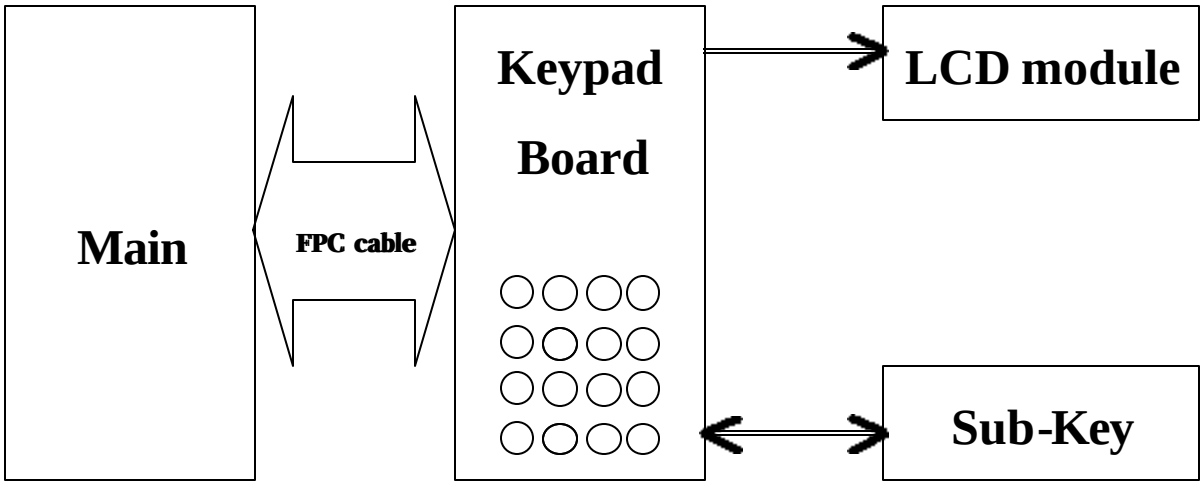

Figure 3.6. Block Diagram of Keypad, Sub-key and LCD.

The block diagram of keypad, sub-key and LCD block is shown in Figure 8. The keypad board is connected to main board via 30 lines of FPC cable. The signals for keypad interface comprise 9 lines for keypad sensing, 6 lines for LED driving, 7 lines for LCD data, LCD backlight enable line, and some control signals for LCD. The sub-key board is connected to keypad board via 6-line cable. The interface signals comprise power line for sub-key LED and 4 lines for keypad sensing. The control signal for LCD backlight and LED power should be within the range of 3.9V~4.5V. If the input range for LCD control is lower than the required range, the operation of LCD backlight will be abnormal. If the input range for LCD control is higher than the required range, damage will occur in the LCD module.

The LCD module is connected to keypad board via 16-pin connector. The interface signals comprise power line, operating voltage for LCD driving, control signals for LCD backlight, and some control and data signals for LCD display. The timing diagram of LCD module is shown in Figure 9.

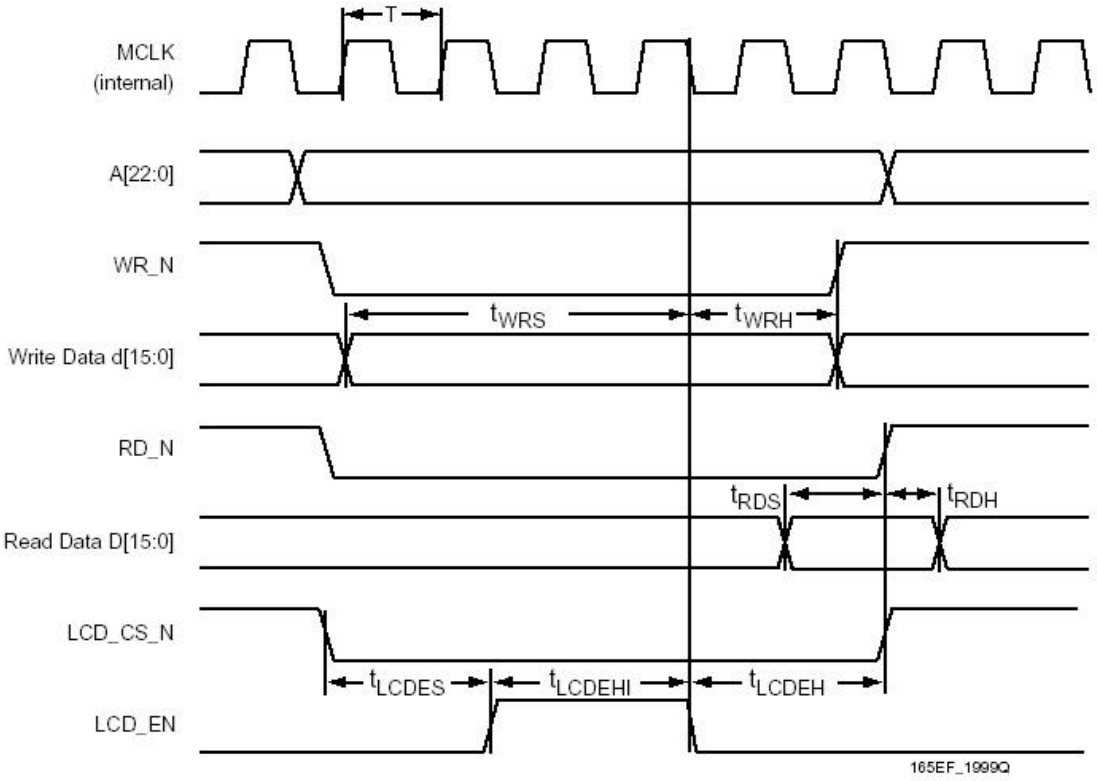

Figure 3.7. Timing Diagram of LCD Module.

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3.2. CDMA Module

NeoTel-811 contains CDMA Module for CDMA cellular operation, which consists of baseband module and RF module. It covers CDMA baseband signal processing and RF signals.

Baseband module contains the main processor, MSM3100, to support the CDMA signal processign and support typical phone application functions. It has digital control signals and analog interface signals for phone functions including audio interface, keypad/LCD interfaces, serial communications with PC in main board and CDMA 800MHz band RF module. The RF module demodulate the RF signal input from antenna to baseband CDMA signal and modulate the CDMA baseband signal to RF signals to BTS.

The CDMA module, which consists of Baseband module and RF module, needs typically min 3.8 / max 4.2 DC power from main board. The regulated +4.0 V DC must be supplied to the CDMA module uninterruptedly. The CDMA module only, excluding main board and LCD, consumes about 30 mA in sleep mode and max 600mA with maximum Tx power.

The CDMA module power is controlled by a signal PWR_ON that comes from the main board with power switch turned on and the PS_HOLD signal of its own.

3.2.1. Baseband Module

Baseband module contains MSM3100(Mobile Station Modem 3100) ASIC, Combination RAM(16Mbit Flash + 4Mbit SRAM), 256kbit serial EEPROM, 32.768kHz Sleep crystal, and 3V LDO Voltage regulator with reset, etc. The most important parts of BB module are MSM3100 for baseband CDMA digital signal processing, and memory.

MSM3100 CDMA ASIC, main processor of BB module, performs the overall CDMA call processing and NeoTel-811 typical phone interface.

3.2.1.1. Power & Reset

BB Module main power is supplied by the 4V regulator in Main board, it was supplied through 60 pin BB-Main connector. The main voltage regulator in BB module, LP2988-3.0, which was low vlotage dropout[LDO] 3V voltage regulator with reset, supplies power for MSM3100 and other baseband part peripherals. It regulates the input voltage from the main board to 3.0V with small tolerance for BB module chipsets, including MSM3100, memory, etc. LP2988 also generates reset signal for power-on-reset operation of MSM3100.

The main 3V baseband power line is seperated by several beads to reduce the interference between digital and analog power of MSM3100 and other components in the baseband

module.

3.2.1.2. MSM3100

MSM3100 in baseband module is the central interface device of the CDMA module, it sends and receives information to and from most of the other internal components of the NeoTel-811 WLL phone. The MSM3100 performs baseband digital signal processing and executes the phone system software. It provides interfaces and control signals to the RF and baseband section, signals to the audio circuits, a glue-less memory interface, and the required user interfaces for phone applications. The MSM3100 also contains complete digital modulation and demodulation systems for CDMA standards, as specified in IS-95-B.

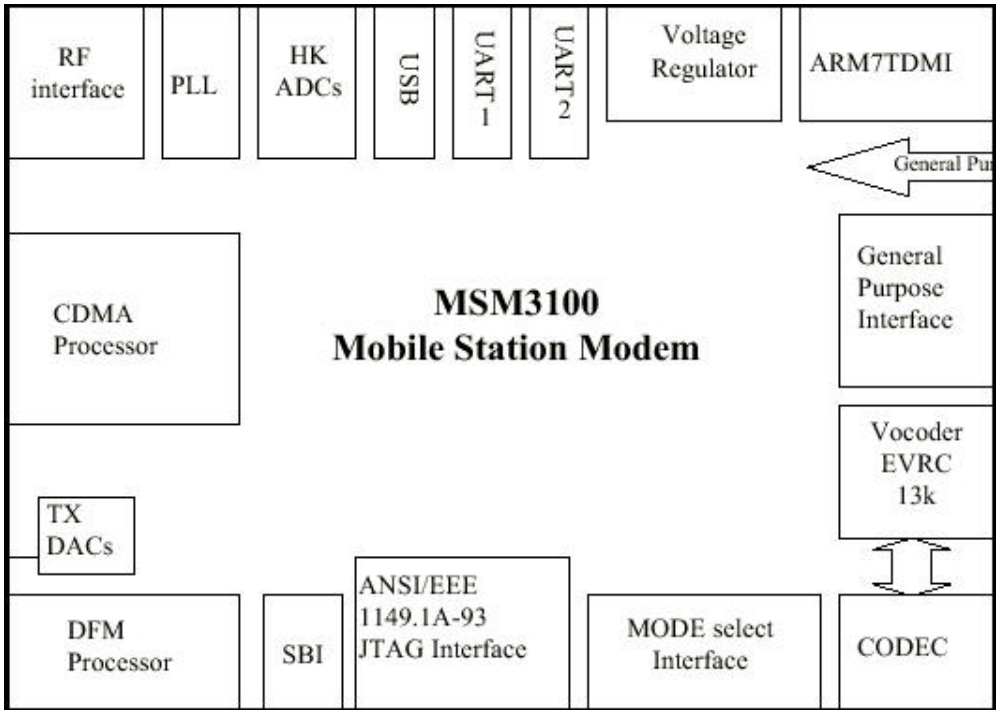


Figure 3.2.1. MSM3100 Mobile Station Modem ASIC Internal Functional Diagram

Within the MSM3100, a CDMA processor, a multi-standard Vocoder, an integrated CODEC with earpiece and microphone amplifiers, general-purpose ADC for system monitoring, an ARM7TDMI microprocessor, and RS-232 serial interfaces supporting data communications with the PC.

The internal Vocoder supports EVRC, QCLEP 13K Vocoders and DTMF generation and detection, Advanced Noise Suppression, audio AGC control, and automatic volume control

(AVC).

The MSM3100 integrates a voice band audio CODEC into the Mobile Station Modem (MSM). The CODEC supports two differential microphone inputs, one differential earphone output, one single-ended earphone output, and a differential analog auxiliary interface. The CODEC integrates the microphone and earphone amplifiers into the MSM3100, reducing the external component count to just a few passive components. The microphone (Tx) audio path consists of a two-stage amplifier with the gain of the second stage set externally. The Rx/Tx paths are designed to meet the ITU-G.712 requirements for digital transmission systems.

The NeoTel-811 WLL Phone system software is executed by an ARM7TDMI embedded microprocessor in MSM3100 and controls most of the functionality of the CDMA module and the user interfaces including the keypad, LCD display, and ringer. These are under the direct control of the MSM3100 without other processor.

MSM3100 supplies the Forty-eight general-purpose I/O pins for interconnecting some peripherals for typical phone application including external keypad interface, parallel LCD interface, The function of these GPIO pins can be controlled by the various software releases.

Serial Bus Interface (SBI) that controls the other QUALCOMM ASICs in the subscriber unit. And It supports three spare Pulse Density Modulated (PDM) outputs for user-defined analog control in addition to those PDMs dedicated to the RF interface, general-purpose programmable M/N counter output, programmable ringer output.

MSM3100 in BB module supports the RF interface. The RF Interface communicates with the Mobile Station's external RF, IF, and analog baseband circuits. Signals to these circuits control signal gain in the Rx and Tx signal path, control DC baseband offset errors, and maintain the system's frequency reference.

Through a generic Serial Bus Interface (SBI) the MSM3100 configures and controls the functionality of the RFT3100, IFR3000. Using the Serial Bus Interface, the IFR3000, RFT3100 can be configured for different operating modes and configured for minimum power consumption, extending battery life in standby mode.

3.2.1.3. Memory

Memory in BB module consists of Comb. RAM and EEPROM. The used Comb RAM, LRS1331 of sharp co.ltd., contains 16Mbit Flash memory and 4Mbit SRAM.

Flash memory stores the main programs of the NeoTel-811 WLL phone, including programs for call processing, user interfaces(UI), service programming, test program, etc.

SRAM stores system variables which is used during the call processing. And It is used for data buffers to store the temporary data.

EEPROM stores system parameters such as ESN(Electronic Serial Number), NAM(Number Assignment Number), Phone books, and RF calibration data including temperature compensation, channel dependent offset values.

3.2.1.4. Two Main board – BB board 60 pin Connector functional description

The two 60 pin connectors, which intercennects the main board and baseband CDMA moduel, performs the control of signals for the phone application interface signals in main board and supplies power from main board to CDMA module and makes a ground effects.
The interfaces supplied by connectors between main board and baseband CDMA module are Power control, JTAG, UART, LCD, Keypad, Audio, LED, etc.
The signals name and its functional descriptions are shown as in table 4.2.1.(a) and (b).

Table 3.2.1. (a) Main board- baseband CDMA module connector J1 descriptions

60 pin connector J1					
CON #	CON pin NAME	DESCRIPTION	CON #	CON pin NAME	DESCRIPTION
1	MIC+	Handset Mic +	60	TDO	J-TAG
2	MIC-	Handset Mic -	59	TCK	J-TAG
3	NC	NC	58	TMS	J-TAG
4	EAR+	Handset Speaker +	57	TDI	J-TAG
5	EAR-	Handset Speaker -	56	TRST*	J-TAG
6	GND	GND	55	GND	GND
7	NC	NC	54	NC	NC
8	SPK+	N/A (for speaker phone)	53	RING	Ring signal to Buzzer in main board
9	GND	GND	52	ON_SW_S*	Power switch status sensing
10	NC	NC	51	HOOK_SW	Phone hook switch status monitoring
11	NC	NC	50	GND	GND
12	GND	GND	49	RESIN*	Reset input from main board
13	KYPD0	Keypad sense	48	NC	NC
14	KYPD1	Keypad sense	47	TMODE*	MSM3100 mode select
15	KYPD2	Keypad sense	46	4V	4V
16	KYPD3	Keypad sense	45	4V	4V
17	KYPD4	Keypad sense	44	NC	NC
18	KYPD5	Keypad sense	43	NC	NC
19	KYPD6	Keypad sense	42	NC	NC
20	KYPD7	Keypad sense	41	NC	NC
21	KYPD8	Keypad sense	40	NC	NC
22	KYPD9	Keypad sense	39	NC	NC
23	GND	GND	38	GND	GND
24	NC	NC	37	MSM_DP_DCD*	RS-232 interface
25	NC	NC	36	MSM_DP_CTS*	RS-232 interface
26	NC	NC	35	MSM_DP_RI	RS-232 interface
27	NC	NC	34	MSM_DP_RFR*	RS-232 interface
28	NC	NC	33	MSM_DP_TXD	RS-232 interface
29	NC	NC	32	MSM_DP_RXD	RS-232 interface
30	NC	NC	31	MSM_DP_DTR*	RS-232 interface

Table 3.2.1. (b) Main board-baseband CDMA module connector J2 descriptions.

60pin Connector J2					
CON #	CON pin NAME	DESCRIPTION	CON #	CON pin NAME	DESCRIPTION
1	LED_BAT0	BATTERY LED control signal	60	BAT_SENSE	Battery Level monitoring signal
2	LED_BAT1	BATTERY LED control signal	59	NC	NC
3	NC	NC	58	NC	NC
4	GND	GND	57	NC	NC
5	NC	NC	56	NC	NC
6	NC	NC	55	GND	GND
7	NC	NC	54	B_EN	LCD Backlight ON signal
8	NC	NC	S	LCD_DATA_SEL	LCD INSTRUCTION/DATA monitoring
9	NC	NC	52	NC	NC
10	GND	GND	51	NC	NC
11	LCD_R/W	LCD Read / Write control signal	50	NC	NC
12	GND	GND	49	NC	NC
13	D0	LCD data 0	48	NC	NC
14	D1	LCD data 1	47	EXDC_ALIVE*	SMPS external DC alive monitoring signal
15	D2	LCD data 2	46	NC	NC
16	D3	LCD data 3	45	NC	NC
17	D4	LCD data 4	44	NC	NC
18	D5	LCD data 5	43	PS_HOLD	Control signal for Powering Off registration
19	D6	LCD data 6	42	GND	GND
20	D7	LCD data7	41	GND	GND
21	GND	GND	40	NC	NC
22	MSG_LED0	Message LED control signal	39	GND	GND
23	NC	NC	38	NC	NC
24	LCD_CS*	LCD select signal	37	NC	NC
25	LCD_EN	LCD data Enable signal	36	NC	NC
26	4v	4v	35	NC	NC
27	4v	4v	34	NC	NC
28	NC	NC	33	PS_CTRL	Power status Control : ON/ST-BY/OFF
29	NC	NC	32	LED_RSSI0	RSSI LED control signal
30	GND	GND	31	LED_RSSI1	RSSI LED control signal

3.2.1.4.1. JTAG

The MSM3100 complies with the ANSI/IEEE 1149.1A-1993 feature list. The JTAG interface can be used to test digital interconnects between devices within the mobile station during manufacture. The JTAG Interface aids in Mobile Station board-level testing, and debugging. The JTAG Interface is accessed through the Test Access Port (TAP). The TAP includes the following input and output (I/O) pins.

Table 4.2. 2. JTAG interface signal descriptions

Signal Name	Signal Description
TDO	test data output
TDI	test data input
TMS	test mode select input
TRST_N	test reset input
TCK	test clock input
TMODE	Test mode select

3.2.1.4.2. Keypad & LCD

Typically mapped 10 key inputs [4 keysense pins + 6 GPIOs] and LCD control signals and LCD data d[0:7] are supported including LCD_CS/ in MSM3100.

10 key interface signals form keypad and sub-keypad board are input to MSM3100, the combination of which constructs the key matrix for specific key functions.

The key map diagram are shown as in figure 4.2.2.

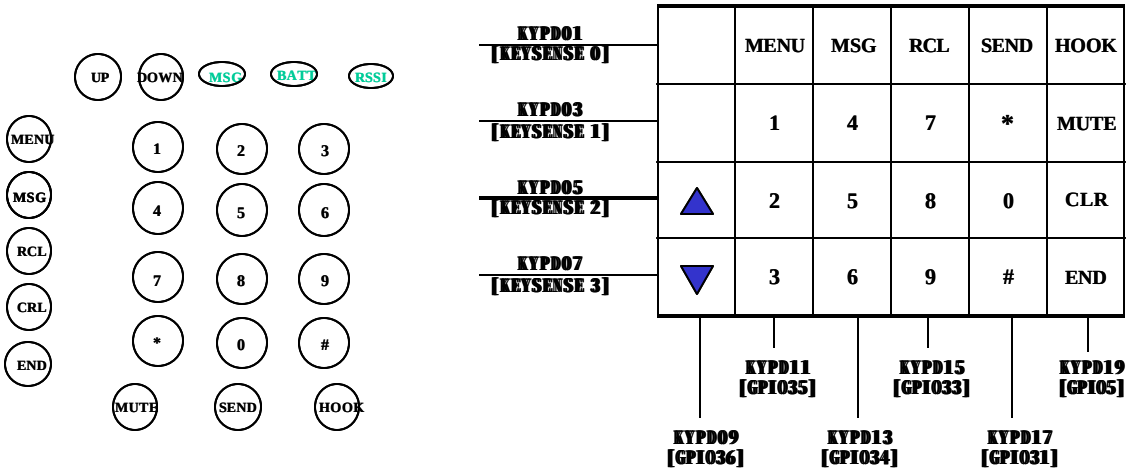


Figure 3.2.2. Keypad MAP diagram and Key Matrix

The control signals for LCS are LCD_CS/, LCD_Enable, Backlight_Enable, LCD_instruction/data select signal, LCD_read/write signal, and 8bit data lines for LCD.

The GPIO signals of the MSM3100 are assigned to the LCD control signals.

3.2.1.4.3. UART[Serial communication port] interface

The NeoTel-811 phone communicates with serial data that conforms to the standard RS-232 interface protocol. UART(universal asynchronous receiver/transmitter) signal transceiver is implemented on the main board.
The BB module provides the digital UART signals, and is 3.0V CMOS level signals. The glue logic for level converting for PC serial communication interface are implemented in main board.

Table 3.2.3. UART serial communication interface signals descriptions

Signal Name	Signal Description	Characteristic	Direction
DCD	Data Carrier Detect	Network connectedfrom the modem	DCE to DTE
RXD	Receive Data	Input data from the host to modem	DTE to DCE
TXD	Transmit Data	Output data from the modem to host	DCE to DTE
DTR	Data terminal ready	Host ready signal	DCE to DTE
DSR RFR[RTS/]	Data set ready Request to send	Modem ready signal to host Ready for receive from modem to host	DTE to DCE DCE to DTE
CTS/	Clear to send	Modem output signal	DTE to DCE
RI	Ring indicator	Output to host indicating coming call	DCE to DTE
GND	Ground	Common ground	

* DTE : HOST DCE : MODEM

3.2.1.4.4. Audio Interfaces

The BB module supports the analog audio interface signals, which are intended for very simple audio interface. The BB module provides typical handset audio interface and car kit microphone inputs and speaker outputs. The car kit audio interface are designed, but not implemented yet.

- Primary analog audio signals

The analog audio interface supported by the BB module is typically used for direct interface with usual handset of phone. It doesn't need glue logic.
The output power for the differential EAR1 output is typically 35 mW for a full-scale +3 dBm0 sine wave into a 32 Ohm speaker. NeoTerl-811 handset meets this spec.

Table 3.2.4. Analog Audio interface signals for Handset

Signal Name	Signal Description	Characteristic
MIC+	Mic input +	Primary Differential Analog input
MIC-	Mic input -	Primary Differential Analog input
EAR+	Handset Speaker +	Primary Differential Analog output
EAR-	Handset Speaker -	Primary Differential Analog output

- Secondary analog audio signals for Car-kit audio

The output power for the single-ended EAR2 output is typically 8.8 mW for a full-scale +3 dBm0 sine wave into a 32 Ohm speaker. It was typically used for typical headset application. Some glue logic including audio power amplifier was needed for speaker phone. It was already designed in main board, but It is not assembled yet.

Table 3.2.5. Analog Audio interface signals for speaker phone.

Signal Name	Signal Description	Characteristic
MIC2+	Mic input +	Secondary Differential Analog input
MIC2-	Mic input -	Secondary Differential Analog input
EAR2+	Handset Speaker +	Secondary Differential Analog output
EAR2-	Handset Speaker -	Secondary Differential Analog output

3.2.1.4.5. LED interface

There are 3 LEDs in main board, Battery LED, RSSI level LED, which are bi-color LED, Message Aarrival Indication LED, which is green LED. They are controlled by BB module, which controls the LED via GPIO programming by SW.

Table 3.2.6. LED control signals and status

LED control signal combination		Color	Status
Battery LED 0	Battery LED 1		
0	1	Green	Enough Charged state
1	1	Yellow	Medium charge
1	0	Red	Needs Charge
RSSI LED 0	RSSI LED 0		
0	1	Green	Receved signal strength is good
1	1	Yellow	Receved signal strength is medium
1	0	Red	Receved signal strength is bad
Message LED 1		Green	LED On at the arrival of the new message.

3.2.1.4.6. Miscellaneous signals for typical phone applications

Table 3.2.7 Control signals for some phone application function

Signal Name	Functional Description
PS_HOLD	Power Signal Holding : It is maintained high by MSM3100 till powering off registering performed , when the power swtich sets in stand-by position
ON_SW_S*	Sitch On Status : Main Power switch status monitoring input from main board
HOOK_SW	Hook switch On /Off : Handset Hanging monitoring
RINGER	Ring signal or Key Tone signal output to Buzzer in main board
EXDC_ALIVE	External DC Alive : Informs External SMPS DC are connected, not Battery

3.2.2. RF module

The MSM3100 is the centerpiece of the 3100 chipset made up of the MSM3100 mobile station modem, the RFT3100 analog baseband to RF upconverter, the IFR3000 IF to baseband downconverter ASIC. The interface between the MSM3100 and the RF module in NeoTel-811 begins with the IFR3000 in the Rx signal path and the RFT3100 in the Tx signal path. Because of the mixed-signal integration of the MSM3100, both analog and digital signals go to or come from the MSM3100.

The interface signals, which interconnect the MSM3100 in BB module to RF module components including RFT3100, IFR3000, PLL, etc, are shown as in figure 4.2.3. and the basic RF module block diagram are also shown as in figure 4.2.4.

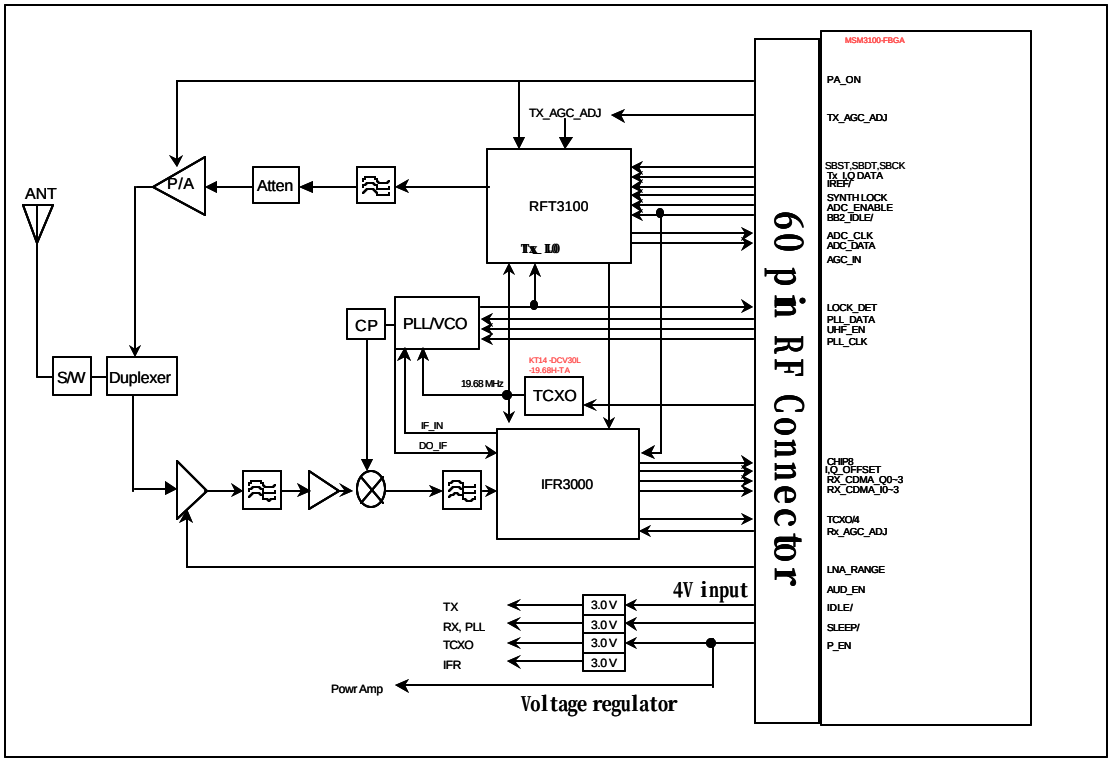


Figure 3.2.3. Interface Signal interconnection BB module to RF module

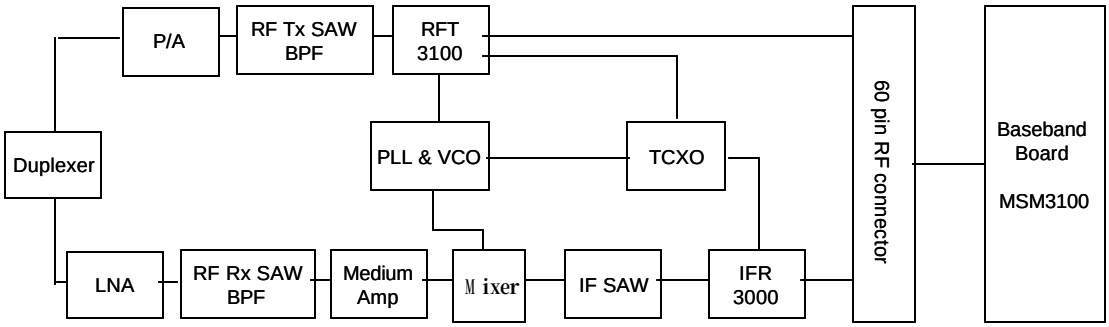


Figure 3.2.4. Basic RF module block diagram

3.2.2.1. Baseband module - RF module 60 pin Connector functional description

The 60 pin connector supplies the control signalsand data for the BB module and RF module. The MSM3100 in BB module controls the peripherals in RF module.

It contains the power, voltage regulator enable signals, PDM signal lines, analog signals such as battry level to ADC in RFT3100, CDMA Tx I/Q analog differntial signals to RFT3100, and CDMA I/Q digital signals from IFR3000.

The interface signals between BB module and RF module are shown as in table 4.2.8. and the functional descriptions for each interfaces are described as follows.

Table 3.2.8. BB module - RF module connector J3 descriptions

BB-to-RF 60 pin Connector J3					
CON #	CON pin NAME	DESCRIPTION	CON #	CON pin NAME	DESCRIPTION
1	GND	GND	60	GND	GND
2	TX_I	Tx differential In-phase signal + to RFT3100	59	TX_I/	Tx differential In-phase signal - to RFT3100
3	GND	GND	58	GND	GND
4	TX_Q	Tx differential Quadrature-phase signal + to RFT3100	57	TX_Q/	Tx differential Quadrature-phase signal - to RFT3100
5	GND	GND	56	GND	GND
6	IREF	reference current signal for RFT3100	55	SYNTH_LOCK	PLL synthesizer lock detect signal
7	PA_ON	Power amplifier On signal	54	TCXO_EN	TCXO enable signal
8	THM_ADC	Thermister voltage input to RFT3100	53	TX_AGC_ADJ	
9	GND	GND	52	GND	GND
10	CHIPX8	ChipX8 signal	51	RX_AGC_ADJ	
11	GND	GND	50	GND	GND
12	PLL_DATA	Data from MSM3100 to PLL	49	TRK_LO_ADJ	
13	PLL_CLK	Clock from MSM3100 to PLL	48	LNA_RANGE0	
14	UHF_EN	PLL SBI Enable signal from MSM3100 to PLL	47	VPWR	4V for power amp drive voltage and RF module voltage regulator input vlotage from main board via baseband module
15	GND	GND	46	VPWR	
16	SBDT	SBI data	45	VPWR	
17	SBCK	SBI clock	44	VPWR	
18	SBST	SBI strobe	43	GND	GND
19	GND	GND	42	TCXO_OUT	TCXO output to MSM3100 clock input [19.68MHz]
20	NC	NC	41	GND	GND
21	GND	GND	40	3.0V	RF module digital components supply voltage from MSM3100 digital voltage Vdd
22	Q_OFFSET	Quadrature-phase Rx input signal offset control	39	3.0V	
23	I_OFFSET	In-phase Rx input signal offset control	38	3.0V	
24	SLEEP/	Sleep signal	37	IDLE/	Idle mode signal
25	GND	GND	36	GND	GND
26	RX_CDMA_Q3	Rx differential Quadrature-phase digital signal from IFR3000	35	RX_CDMA_I3	Rx differential In-phase digital signal from IFR3000
27	RX_CDMA_Q2		34	RX_CDMA_I2	
28	RX_CDMA_Q1		33	RX_CDMA_I1	
29	RX_CDMA_Q0		32	RX_CDMA_I0	
30	GND	GND	31	GND	GND

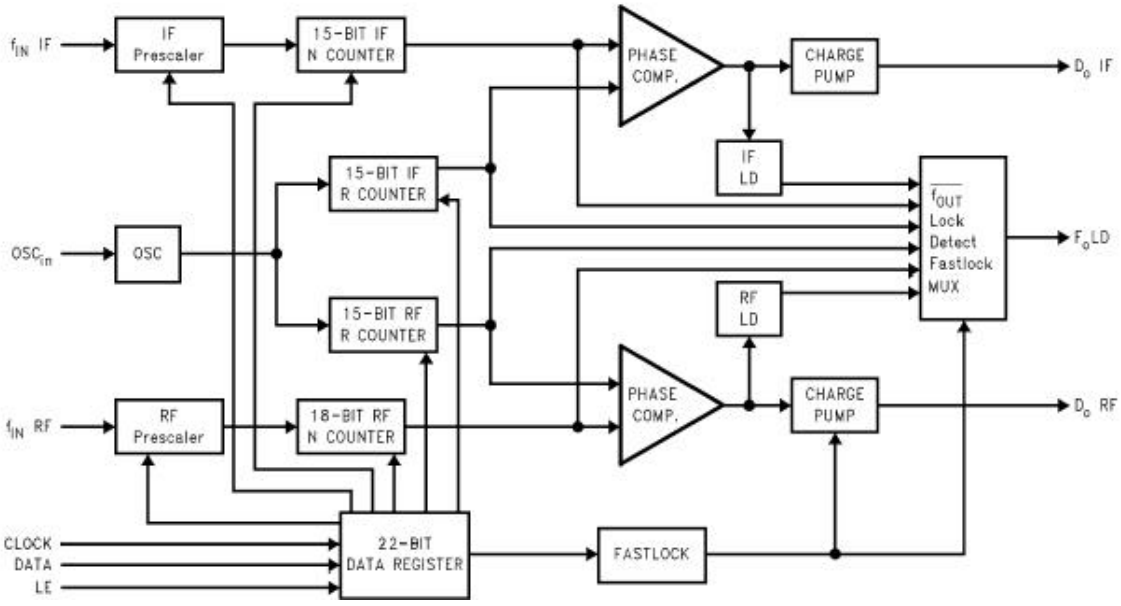
3.2.2.2. PLL

PLLs are designed to be used in frequency synthesizers for programmable and fixed local oscillator generation in RF module.

To complete the subsystem, the PLL IC requires the addition of an external loop filter, Voltage Controlled Oscillator (VCO) and reference source. The reference source can be an external Temperature Compensated Crystal Oscillator (TCXO) or, if the accuracy of the generated carrier is not critical, a simple external crystal. Typical PLL circuit is shown as in figure ??? . and The used PLL in CDMA module of NeoTel-811, LMX2331 of National Semiconductro,. Co.ltd.

Why use PLL as a frequency synthesizer?

- as a local oscillator with a high accuracy and purity.
- to translate the frequency accuracy of a high quality signal source to a tunable signal source
- to translate the noise characteristics of a high quality signal source to a lower quality signal source



3.2.2.3. Tx Path

For the transmit data path (Tx), the MSM3100 modulates, interpolates, and converts the digital signal into an analog baseband before sending it to the RFT3100. The RFT3100 upconverts the Tx analog baseband into RF. The MSM3100 communicates with the external RF and analog baseband to control signal gain in the RF Rx and Tx signal paths, reduce baseband offset errors, and tune the system frequency reference.

The CDMA Tx AGC block controls the mobile station's mean Tx output power, as specified by the equation shown above. The mean Rx input power used by the Tx AGC block, is a filtered version of the RSSI created by the Rx AGC block. The offset power is determined by linearizer calibration procedures and corresponding software interpretation. NOM_PWR - 16 x NOM_PWR_EXT, INIT_PWR, interference correction, and the sum of all access probe corrections are all software-controlled parameters. Closed loop power control corrections are summed by the Tx AGC block circuits.

The Tx AGC block also controls the operating point of a multistate (high efficiency) power amplifier (PA) circuit. The CDMA Tx AGC block supports switching between up to four different PA operating points with programmable levels and temporal hysteresis.

The Tx signal path interface from the MSM3100 is simpler than that of the Rx path because I and Q components are sent to the RFT3100 in analog form. The MSM3100 has differential analog outputs for I and Q components. A 200 pF capacitor is recommended for connection directly between the differential signal pairs (I_OUT, I_OUT_N and Q_OUT, Q_OUT_N) to short out frequency components related to the clock signals on the MSM3100. The 200 pF capacitors are very effective in eliminating clock components and must be mounted on the PC board as close to the MSM3100 as possible. It is also advisable to keep the differential analog traces as short as possible to reduce the chance of other signals from cross-coupling. In addition, a 0.01 F capacitor is required between DAC_IREF and the VDD pin D5.

The RFT3100 performs a dual up-convert function in the Tx signal path. The analog baseband I and Q components from the MSM3100 are upconverted to IF in the first stage of the RFT3100.

The Tx AGC amplifier has its gain controlled via the TX_AGC_ADJ pin of he MSM3100 and a 2-pole RC filter. After the Tx AGC amplifier the signal is upconverted to the UHF frequency using the UHF LO signal from the UHF synthesizer. The output RFT is normally followed by an off-chip SAW filter. Two cellular and two PCS outputs are provided from the RFT3100 to drive the remainder of the Tx signal path.

The VDDM pin of the RFT3100 is intended to bias the RFT3100 digital I/O pins so that they

are voltage compatible with the digital I/O of the MSM3100. The digital I/O of the RFT3100 includes the same SBI interface as found on the IFR3000.

On the transmit side, the RFT3100 accepts analog baseband inputs from the MSM, provides quadrature upconversion to IF, implements IF AGC, then goes off-chip to an IF tank for filtering, upconverts to RF using a single sideband mixer, then amplifies the signal with driver amplifiers. Handset designers generally use the Cellular Output A port only, since it has plenty of output power. Between the RFR3100 and the PA3100 is an RF filter to reduce broadband noise leakage and provide image rejection. The PA output should be isolated from the antenna port using an isolator. This device provides a reasonable load to the PA regardless of the antenna VSWR, assuring PA linearity and ACPR performance.

The isolator also provides reasonable source impedance to the duplexer, helping it meet its performance objectives.

Finally, the transmit signal is routed to the antenna through the duplexer, completing the transmit path. As mentioned earlier, the RFT3100 includes PLL components for the transmit IF LO, requiring only the loop filter and VCO resonator off-chip. The UHF LO is shared between the receiver and transmitter, with the RFR3100 providing a buffer amp that delivers the LO to the RFT. And again, the PM1000 is available for power management functions.

3.2.2.4. Rx Path

For the receive data path (Rx), the RFR3100 downconverts the received RF signal of the intermediate frequency (IF). The IFR3000 converts the modulated IF signal from the IFR3100 into digital baseband data. Finally, the MSM3100 demodulates Rx digital baseband data from the IFR3000.

The purposes of the CDMA Rx AGC block are to measure the mean Rx input power (RSSI) for use by the Tx AGC block, and to use this RSSI information to control the gain in the RF and IF circuits. The total gain in the Rx path is dynamically adjusted by the Rx AGC block in order for the demodulator to properly demodulate the signal. The relative gain between the RF circuits and the IF circuits is dynamically adjusted to reduce the effects of intermodulation distortion (IMD).

The interface from the IFR3000 to the MSM3100 involves CDMA and AMPS digital I and Q component data supplied by the IFR3000. This data is transferred to the MSM3100 using CHIPX8 and RX_FM_CLK clock signals which originate on the MSM3100 and drive the IFR3000. Both clock signals share the MSM3100's CX8_FM_CLK pin.

I_OFFSET and Q_OFFSET PDM signals are RC-filtered and drive the offset adjust inputs of the IFR3000 to keep the incoming I and Q component signals in the center of the IFR3000's analog-to-digital converter input range. The RX_AGC_ADJ PDM on the MSM3100 controls the Rx IF AGC amplifier gain according to the Rx AGC loop circuits on the MSM3100. A standard 3-line Serial Bus Interface (SBI) is the digital control link between the MSM3100 and the IFR3000. Note that a pull-up resistor is required on the SBDT line.

Beginning at the antenna, the duplexer separates the receive path from the transmit path using frequency diversity. The receive path starts with the RFR3100's LNA, then an RF filter for image rejection, a switch that routes the signal for CDMA or FM processing, the downconverter, and IF filtering. The narrowband IF signal, either CDMA or FM, is applied to the appropriate IFR3000 AGC amplifier, then a switch connects the active amplifier output to the quadrature downconverter, baseband lowpass filter, baseband amplifiers, and ADCs.

The CDMA ADCs are higher speed than FM and require a parallel output. The FM output is slow enough that it can be serialized and shares two of the CDMA pins to save I/O on the IFR3000. That completes the Cellular receiver path, but a similar path is used for PCS. The only external components you need are filters (IF & RF), synthesizers, and the VC TCXO reference.

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3.2.2.5. ADC interface

The analog signals from main board are input to ADC in RFT3100, they are battery voltage and thermister voltage level dependent on the temperature of the CDMA module. A/D converter in RFT3100 senses the level of the analog signals from main board and converts it to the CMOS level of the input to MSM3100.

MSM3100 receives the level of the ADC output and controls the status of the related battery LEDs and compensates the RF output level coresponding to the temperature condition.