HOLLEY COMMUNICATIONS

HPN1600
FCC Device Under Test Description

Title	FCC Device Under Test Description
Document Number	
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Last Modified	June 23, 2002
Creation Date	June 11, 2002
Version	0.1
Status	Draft
Vob ID	
Path To File	C:/FCC/HopOn/Equipment Description

1 Description of Equipment Under Test (EUT)

The EUT is a CDMA single-mode Cellular Hand Held Phone (HHP), designed to meet or exceed the TIA/EIA IS-95B Standard. The EUT is capable of operating only in the 800MHz Cellular frequency band.

The technical descriptions included in this section covers the receive (RX) section, the transmit (TX) section, the logic hardware section and the Baseband section of the HHP. The technical descriptions are intended to describe supporting hardware circuits only and are not intended to address firmware or protocol issue except where applicable.

1.1. Description of Circuits and Devices

1.2. RF Receive Path Description

The receive RF section is designed to receive CDMA signals in the cellular 869 – 894 MHz frequency band. The input RF section consist of a internal Antenna and matching network, Rx/Tx SAW duplexer (DU0101), an antenna input switch (J0102), and an Integrated circuit, U0103, which consists of a Low Noise Amplifier (LNA), a mixer and gain control circuitry, SAW filter, FL0201 and Variable Gain Amp, U0201. An optimum match for the RF air-interface is provided by the internal antenna and matching network combination, in addition to providing a matched load for the power amplifier and LNA. The antenna switch provides an external input/output port to test the HHP. The Rx section of the duplexer provides out-of-band signal filtering prior to being applied to the LNA input as well as providing 55 dB of attenuation to the transmitted signal. The LNA is the first gain block in the receive chain and essentially establishes the receiver RF section input noise figure. The chip integrates an RF-to-IF down conversion mixer in addition to 30 dB of gain control. The RF SAW filter (FL0201), provides image rejection and out of band filtering for the RF front-end. A differential variable gain amplifier, U0201, following the SAW filter is a key component in a closed AGC gain loop that functions to maintain a constant power level for the baseband adapter (BBA) chip input with a dynamic range in excess of 80 dB.

1.3. RX Synthesizer Section Description

The synthesizer chip (U0501), consists of a synthesizer chip a VCO (U0502), and second-order loop filter. The Temperature Controlled Crystal Oscillator (TCXO), U0702, provides the input reference frequency to the synthesizer. The synthesizer output provide the local oscillator input for the receive chain.

1.4. TX Synthesizer Section Description

The Synthesizer is shared by both transmit and the receive chains. The synthesizer output also provides the local oscillator (for up-conversion) to the transmit chain.

1.5. Transmitter (TX) Section Description

The transmitter section receives it input from the BBA chip (U0801) and is first received by the variable voltage amplifier (VGA), U0402. The VGA a key gain block forms part of an output power control loop. A SAW filter (FL0401), follows the VGA and provide out-of-band filtering and selectivity to the transmit chain. Following the SAW filter the signal is up-converted to the final transmit frequency by mixer (U0301) which is exactly 45 MHz below the incoming CDMA received signal. Additional filtering is provided by RF SAW filter (FL0301) before the signal is applied to a second VGA (U0361). The two VGA's in the transmit chain collectively function to provide a combined dynamic range in excess of 70 dB. The power amplifier (PA), U0303, further provides signal amplification in the transmit chain. The PA can be rendered inactive by switch (Q0361). The PA is a linear power amplifier. A circulator (U0305) follows the PA and providing the PA output protection from potentially high reflective energy. The PA output is finally routed to the Tx section of duplexer (DU0101) where additional filtering is provided for the PA output such as harmonic or other spurious emissions. The RF test jack, J0102 provides a means to measure the conducted power level prior to being applied to the antenna matching network and antenna. Maximum ERP across the cellular transmit frequency band is realized with a good impedance match to the antenna via the matching network.

1.6. Baseband Section Description

The BBA chip (U0701) and the CDMA+200 (U0801) chips together comprise the baseband analog and DSP sections for the HHP. In the BBA chip, all data conversions, such as the analog to digital (ADC) and the digital to analog (DAC), are provided. In the CDMA+200 chip all digital signal processing (DSP) functionality is provided. Both chips are Philips proprietary chip designs. They also function as the baseband Modem providing the modulation and demodulation for the CDMA receive and transmit signals. The CDMA+200 provides an audio codec that interfaces to external audio from the handsfree adapter.

1.7. LCD

This phone does not use an LCD display.

1.8. CPU Section Description

The CPU is used to provide timing and commands to the RF section and the hardware section. The CPU firmware is stored in FLASH non-volatile memory, U0901.

1.9. Serial Buss Interface Description

Test points, TP0806-TP0811, available through external holes in the plastic case allow the firmware to be loaded or upgraded via a standard RS-232 interface.

1.10. Function of Active Devices

The active devices used in the HHP are listed in Table 1.

Table 1 Active HHP Parts

Philips P/N	QTY	Ref. Designator	Part Number
M2740	1	U0307	IC, M20B
M2742	1	U0302	IC, 1037B
M2746	1	U0502	VCO VC
M2760	4	D0501-4	DIODE, CAPACITIVE
M2763	1	U0501	LMX233XL, IC
M2769	1	U0103	IC,RF2361
M2770	1	U0105	IC, RF2466
M3170	1	U0101	IC, RF2489
M2772	1	U0301	IC, UPC8106TB-E3
M2774	2	U0102 U0104	IC, AA103-72
M2775	2	U0306 U0401	OPAMP, IC, LMV722
M2780	1	U0702	VCO, VC-TCXO-204C1
M2782	1	D0301	DIODE_SCHOTTKY, HSMS-2825
M2784	5	U0601- 5	REG_V_6, IC, TK11233BMCL
M2785	1	U0201	IC, RF2617
M2787	2	Q0101- 2	TRANSISTOR, NPN, DTC115EEA
M2821	1	Q1002	PNP, 2SB624
M2823	2	D1201-2	DIODE, MMBD4148
M2834	1	U0802	IC, S-75V08ANC5
M2836	3	Q1101- 3	TRANSISTOR, NPN, 2SD596
M2847	1	U0901	IC, LRS1348, BGA, 72pin
M2849	1	Q1001	MOSFET Dual, PCHAN, SI6965DQ
M2850	1	U1002	IC, NC7SZ175P6, SC70-6
M2851	1	U1003	IC, NC7SZ66P5, SC70-5
M2853	1	Q0504	TRANSISTOR, PNP, DTA115EEA
M2859	1	U1001	IC, NC7WZ14P6, SC70-6
M2892	2	D1001- 2	DIODE, BAS16W
M2895	1	Q0901	MOSFET, PCHAN, BSH206, SOT363
M2896	1	U0308	IC, ADG704BRM, RM-10
M2902	1	U0701	IC, CXA3303GA, LFLGA, 76 pin
M2903	1	Q0301	MOSFET, Dual NCHAN, PCHAN, SI1553DL
M2909	2	Q1201-2	TRANSISTOR, NPN, BC817

M3023	3	Q0501-3	TRANSISTOR, PN, E68119
M3025	1	U0303	IC, F3105
M3026	1	U0801	IC, DMA+100 BGA
MRNU0202	1	U0202	IC, MV722 VSP8 OPAMP

1.11. Frequency Stabilization

The Frequency stability is established by the TCXO, U0702, which has a stability of 1 ppm at 25°C and 2.5 ppm over the temperature range from -30°C to +85°C. The incoming CDMA signal stability is established by the transmitting base station. The HHP transmit frequency is generated with the HHP and must be 45 MHz ± 300 Hz below the incoming receive frequency for full duplex operation. This frequency is established by the internal frequency synthesizer, which gets its reference frequency from TCXO. The final transmitting frequency is synthesized with a PLL. The closed response of the PLL holds the output frequency to the stability of the reference TXCO's frequency stability.

1.12. Suppression of Spurious Radiation

The suppression of spurious radiation is provided through the use of selectively filtering. The transmit paths (IF and RF) incorporates highly selective SAW filters which have excellent out-of-band rejection characteristics. And finally, the selective SAW duplexer adds band shaping and rejection for the CDMA transmit frequency band. The transmitting RF frequency is synthesized with a PLL. The PLL incorporates a 2nd order loop filter whose design is twofold.

(1) One to provide a loop response to track the TCXO frequency with small frequency error while providing a good phase margin for overall stability:
(2) Secondly, to provide a closed loop response that suppresses the reference sidebands and other spurious products.

The synthesizer closed loop performance will attenuate spurious that might otherwise enter via the Local Oscillator (LO) into the transmit chain.

1.13. RF output Output Limiting

The final output power at the antenna terminal is limited by the calibration table's resident in the firmware within the HHP. The maximum/minimum output power level for the HHP has been calibrated over the range from a minimum of approximately –50 dBm to a maximum of +24 dBm. The HHP Calibration tables resident in the HHP internal FLASH (non-volatile) memory, U0901 are used to limit the maximum transmit power level (in dBm) delivered to the antenna terminals.

1.14. Description of Modulation

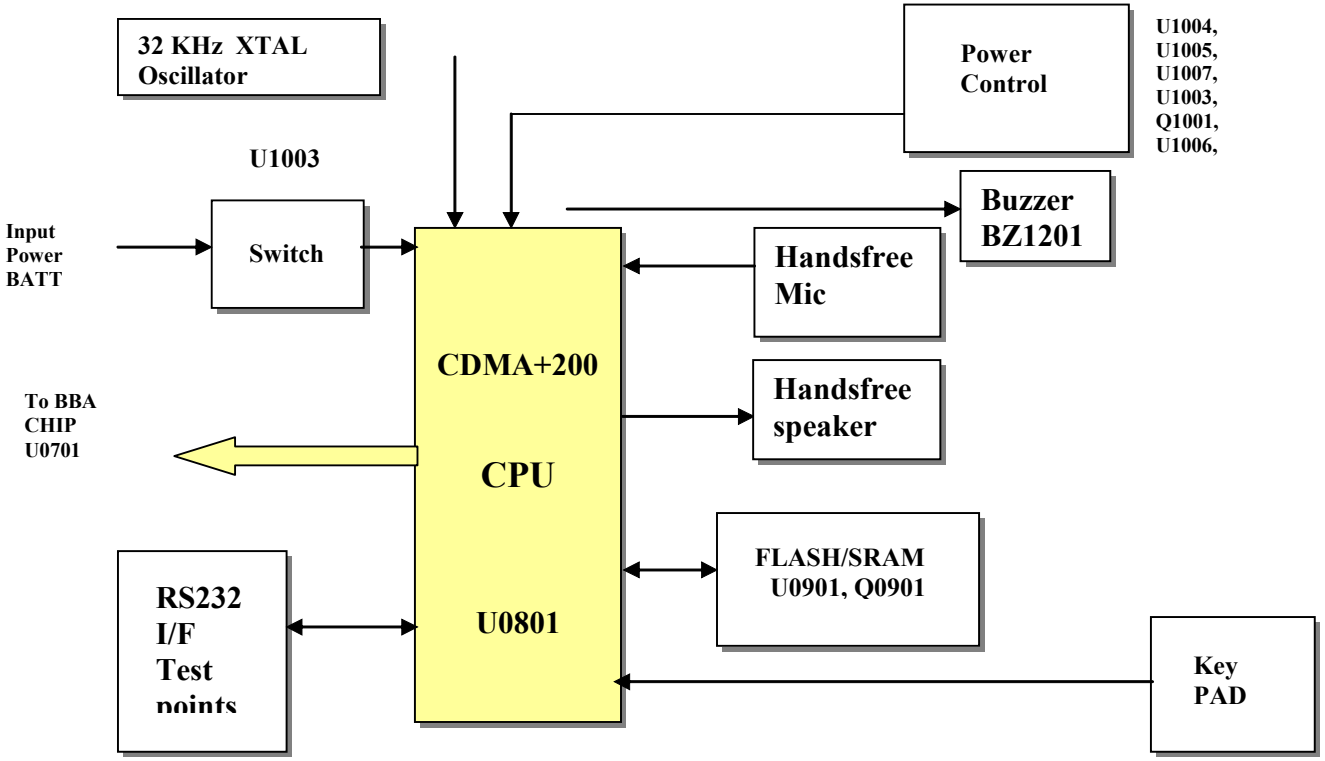
Forward CDMA Channel Modulation (Base Station to the Mobile HHP) Description:

The CDMA signal starts with a basic data rate, say rate 1 (9600 bps), and is spread to a transmitted bit rate or chip rate of 1.2288 MHz. Spreading consist of applying digital codes to the data bits that increase the data rate while adding redundancy. The chips are transmitted from the base station to the mobile handset using Quadrature Phase Shift Keying (QPSK) that has been filtered to limit the transmission bandwidth. This signal is combined at the base station transmitter with all other users in that cell. The QPSK modulated signal is received by the mobile handset where the coding is removed, and de-spread back to the original 9600 bps (in this example). The ratio of the 1.2288 MHz CDMA transmission bandwidth to the 9600 Hz data bandwidth is 128 or 21 dB

Reverse CDMA Channel Modulation (HHP to Base Station) Description:

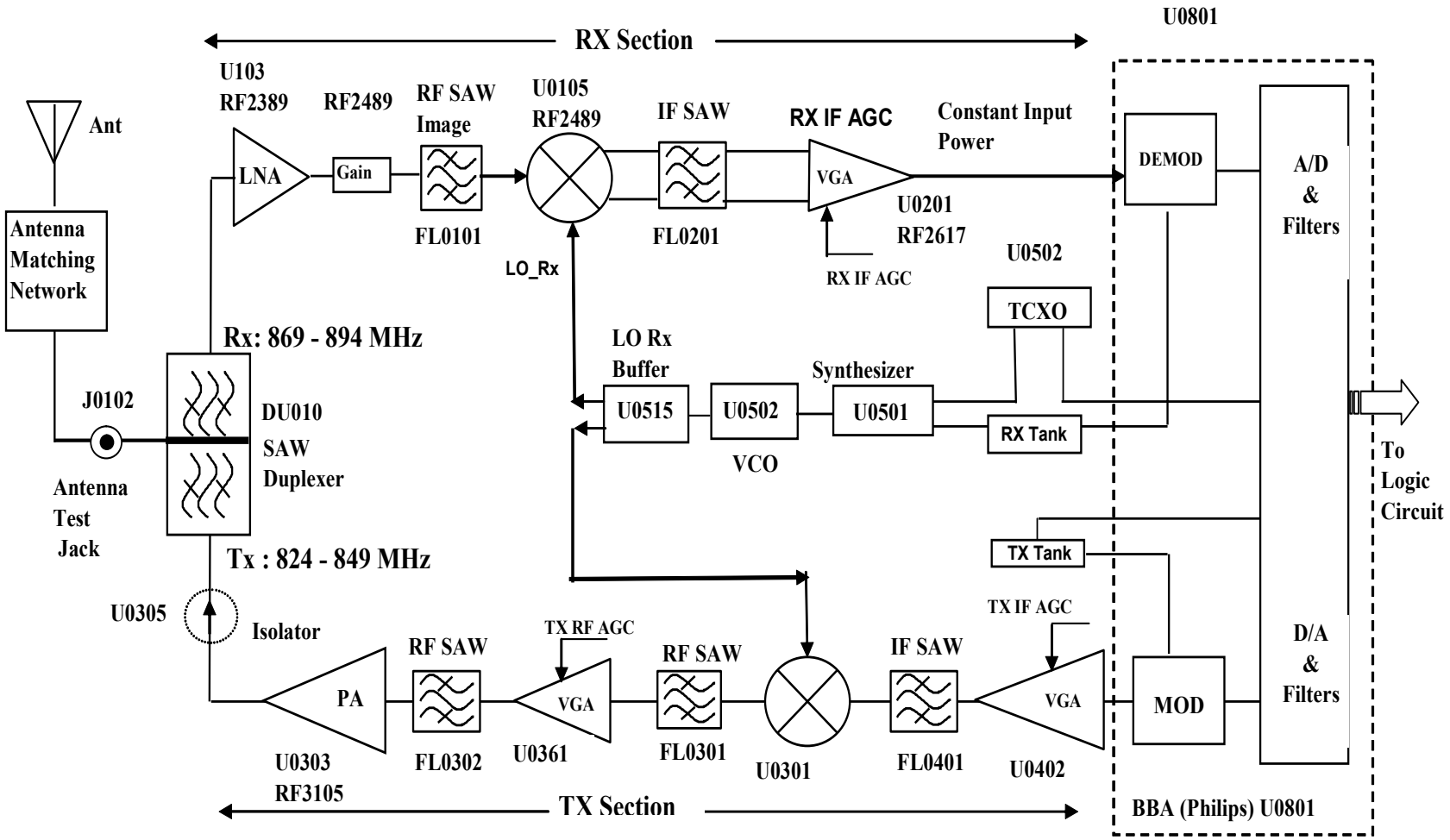
The mobile handset transmits filtered Offset QPSK (OQPSK) to the base station in the reverse channel. The offset is used to avoid the amplitude transients inherent in QPSK. This also allows a simpler design for the output Power Amplifier (PA) in the mobile handset. The capacity is different in the forward and reverse direction due to the difference in Modulation. The forward channel has the phase reference – the pilot signal –as well as orthogonal codes.

1.15. Overall Circuit Schematic

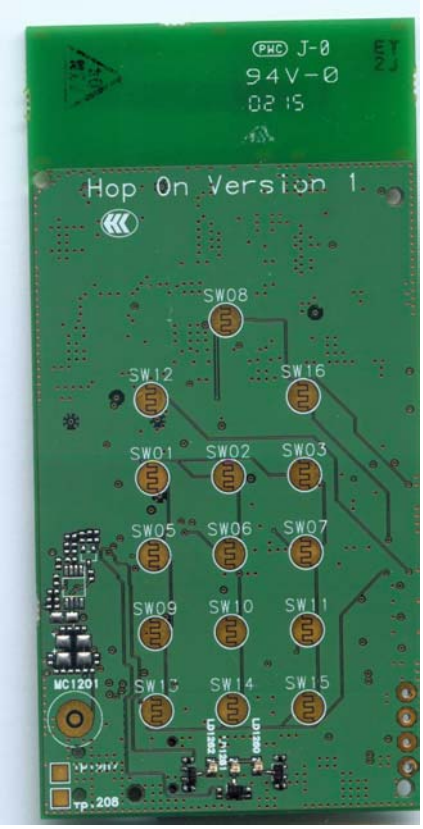


Logic Hardware Block Diagram

RF Block Diagram



1.16. Photos of Printed Circuit Board and Plastic housing.



Back View of PCB

Front plastic cover Bottom plastic cover

FCC label located on bottom half of back cover