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Ph: (403) 347-5400 info@technalogix.ca
Fax: (403) 347-7444 www.technalogix.ca

#4 – 8021 Edgar Ind. Place, Red Deer, AB T4P 3R3

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Application for Certification:
TAV-25L

2.1033(c)(8)

The final amplification stage pallet is a two stage ultra linear class-A linear pallet and has a typical gain of 40dB. These pallets draw no more than 3.0Adc total drain current. The quiescent and drain currents can be measured on the pallet by measuring the voltage drop across the current sense resistor found directly at the DC power supply lead input to the pallet. This resistance is 0.01-ohms, providing a 10mV per ampere ratio.

For the power amplifier that was tested for certification purposes, the final amplification stage draws 1.0A at quiescent power and 2.9Adc at 100% rated power (drain current). The DC supply voltage to all amplification stages in the TAV-25L power amplifier is 30.0Vdc.

2.1033(c)(10)

Determining and stabilizing frequency – There are no frequency determining or stabilizing components found within the TAV-25L power amplifier.

Suppression of spurious radiation – The suppression of spurious radiation is accomplished with the bandpass filter located within the power amplifier enclosure. The passive bandpass filter rejects spurious and harmonic output products and passes the VHF channel RF output. The cavity resonator uses aperture coupling and is a linear resonator design. Typical insertion loss is 0.6 dB to 1.0 dB depending on channel frequency. Average roll off is –33 dBc at a point 4.5 MHz below the peak visual carrier frequency and –30 dBc 9.0 MHz above the peak visual carrier frequency. The filter is DC grounded on both the input and output for additional lightning protection.

Limiting modulation – There are no components or circuitry that limit modulation inside the TAV-25L power amplifier.

Limiting power – The output RF power is limited by taking a sample of the RF output, converting it to a DC voltage proportional to the RF level, and using a microcontroller and analog-to-digital-converter (ADC) to determine if the RF output level is too high. If the level is too high, the power is simply automatically turned back to the proper level. The following schematics depict the circuitry for the shutdown.