Barry Quinlan

From: "Myers, Gary" <Gary.Myers@usa.xerox.com>
To: <certification@curtis-straus.com>
Cc: "Myers, Gary" <Gary.Myers@usa.xerox.com>
Sent: Monday, November 04, 2002 10:31 AM
Attach: Figure3.bmp; Figure1.bmp; Figure2.bmp
Subject: FW: FCC ID: QGMCDW (Clay Delay), Pulse Train Duty Cycle

Barry,

Attached is the pulse train duty cycle information requested by John Curtis for the subject device. The results verify that the Clay Delay passes FCC limits.

Please contact me if any further information is required.

Regards,
Gary Myers

-----Original Message-----
From: Spencer, David H
Sent: Monday, November 04, 2002 8:49 AM
To: Myers, Gary
Subject: FCC ID: QGMCDW (Clay Delay), Pulse Train Duty Cycle

Gary,
I made the measurements on the transmitter as we discussed. I followed the ANSI procedure and have printouts (see attached files 1-3).

In summary:

The pulse width (period from start of first packet to start of next) is 64.4mSec (see figure 1)
That packet contains 41 pulses or bits.
Of those 12 are narrow, having a 360uSec width (see figure 2)
The remaining 29 are wide, having a 760uSec width (see figure 3)

Over a 100msec period the worst case duty cycle included one complete pulse train (64.4mSec) plus 35.6mSec of the second pulse train. This equates to the following:
18 pulses X 360uSec = 6.48mSec
52 pulses X 760uSec = 39.52mSec

Total "on" time of the transmitter over 100msec is 46.0mSec.

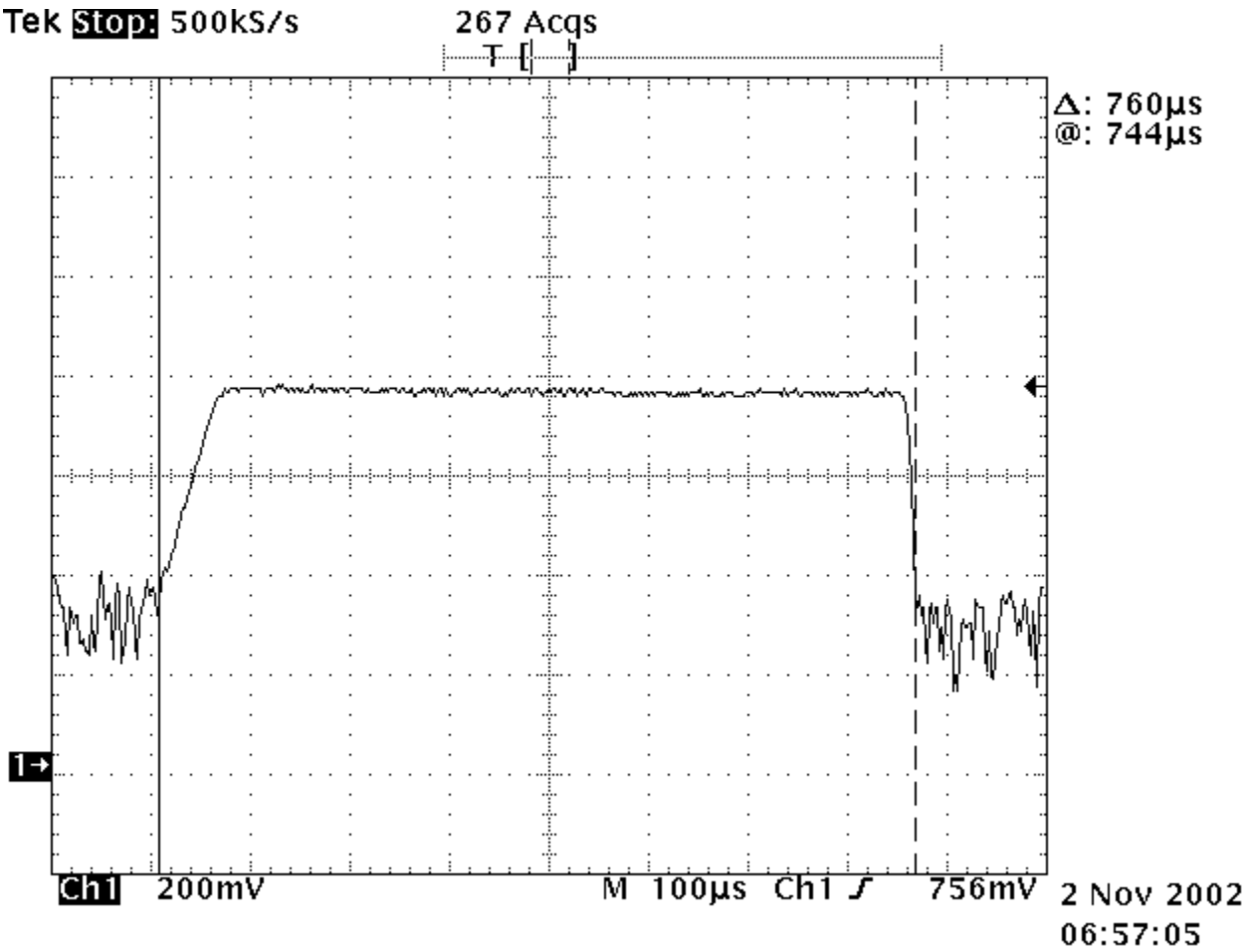
46.0/100 = 46% (duty cycle correction factor)

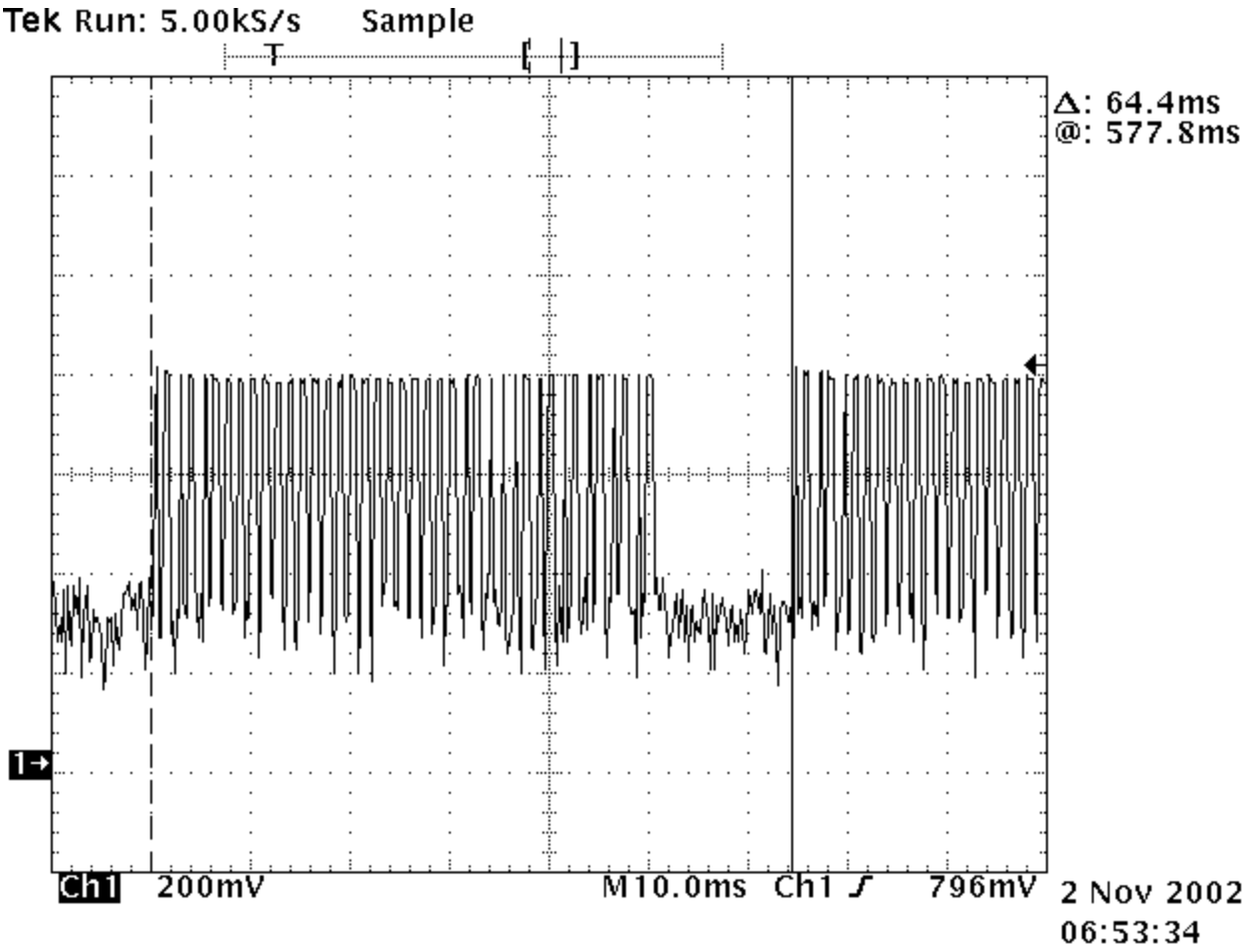
20 X log(0.46) = -6.74 (relaxation factor)

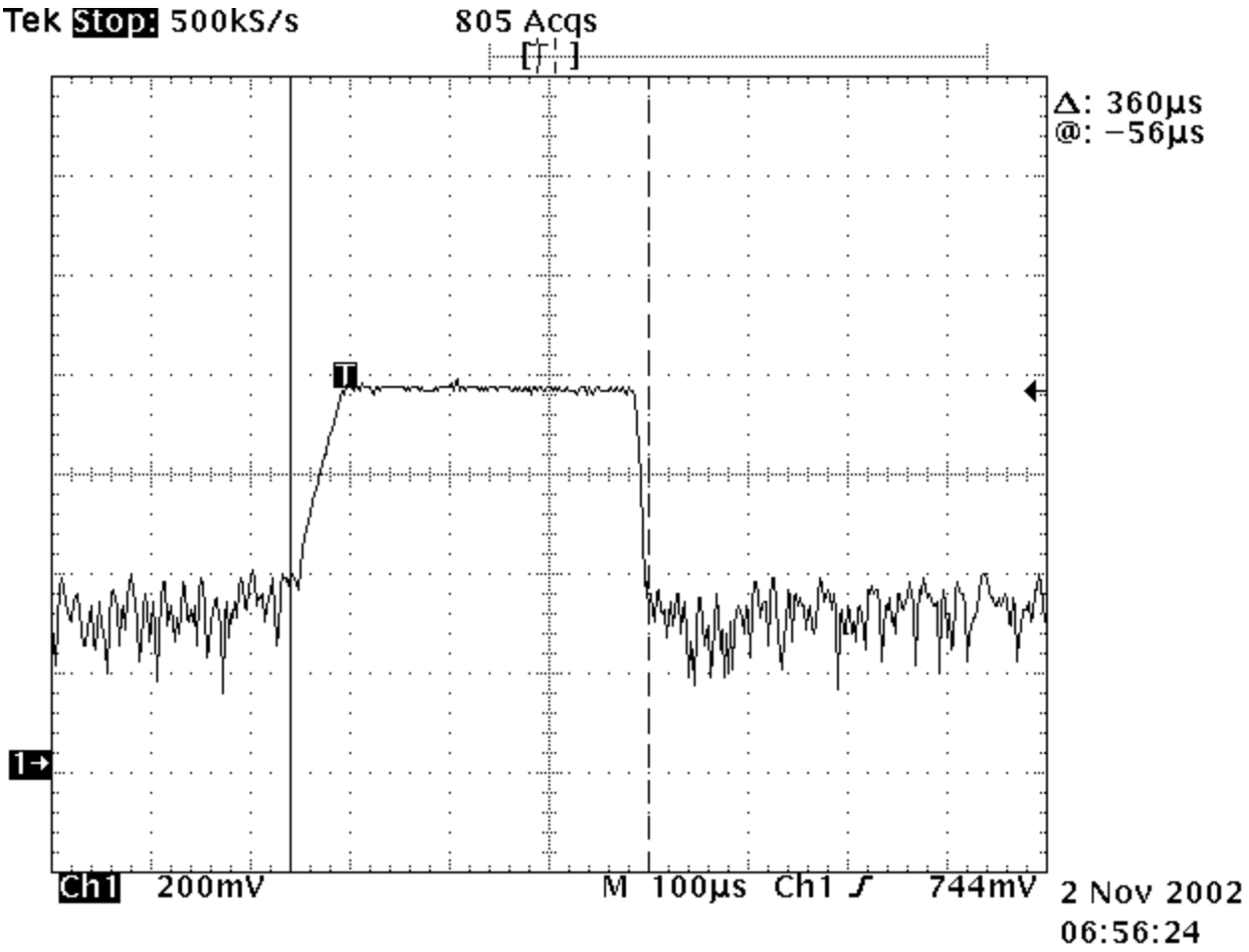
Therefore, with a measured peak reading of 86.0dBuV/m the corrected average reading becomes 79.26dBuV/m against a 80.3dBuV/m limit.

DS

<<Figure3.bmp>> <<Figure1.bmp>> <<Figure2.bmp>>




Tek Run: 5.00kS/s Sample
Δ: 64.4ms
@: 577.8ms
Ch1 200mV
M10.0ms Ch1 ƒ 796mV
2 Nov 2002
06:53:34


Tek Stop: 500kS/s
805 Acqs
Δ: 360µs
@: −56µs
Ch1 200mV
M 100µs Ch1 ƒ 744mV
2 Nov 2002
06:56:24