SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (RF UNIT)

Received signals from the antenna connector are passed through the low-pass filter (L5, L6, C8–C12). The filtered signals are applied to the λ/4 type antenna switching circuit (D101, D102, L4, L206, C209, C210). The passed signals are then applied to the RF amplifier circuit.

The antenna switching circuit functions as a low-pass filter while receiving. However, its impedance becomes very high while D101 and D102 are turned ON (while transmitting). Thus transmit signals are blocked from entering the receiver circuits. The passed signals are then applied to the RF amplifier circuit.

4-1-2 RF CIRCUIT (RF UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit are amplified at the RF amplifier (Q3) and passed through the bandpass filter (FI1) to suppress out-of-band signals. The filtered signals are applied to the 1st mixer circuit.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS (RF UNIT)

The 1st mixer circuit converts the received signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only desired signals will pass through a crystal filter at the next stage of the 1st mixer.

The signals from the bandpass filter (FI1) are mixed at the 1st mixer circuit (Q2) with a 1st LO signal coming from the VCO circuit to produce a 21.7 MHz 1st IF signal.

The 1st IF signal is applied to a crystal filter (FI2) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q1), then applied to the 2nd mixer circuit.

4-1-4 2ND MIXER AND DEMODULATOR CIRCUITS (RF UNIT)

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier (Q1) is applied to the 2nd mixer section in the FM IF IC (IC2, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC contains a 2nd mixer, quadrature detector, noise amplifier and a limiter amplifier, etc. The PLL reference oscillator (X1) is used for the 2nd LO signal via the PLL IC (IC1, pins 16, 17), and is applied to pin 1 of the FM IF IC (IC2).

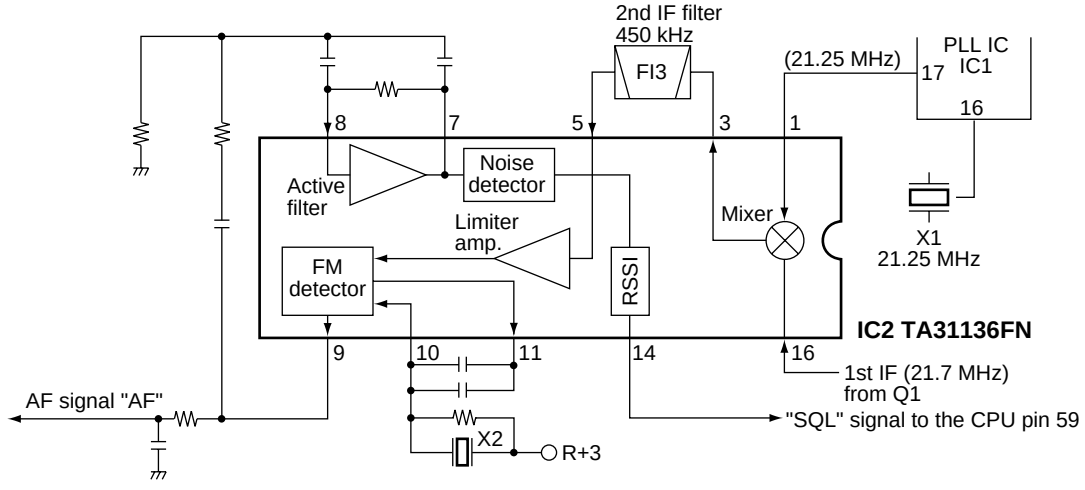
The mixed 2nd IF signal is output from pin 3 (IC2) and passed through the ceramic bandpass filter (FI3) to remove unwanted heterodyne frequencies. It is then amplified at the limiter amplifier section (IC2, pin 5) and applied to the quadrature detector section (IC2, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

4-1-5 AF CIRCUIT (RF AND MAIN UNITS)

AF signals from the FM IF IC (RF unit; IC2, pin 9) are passed through the high-pass filter (RF unit; Q15, Q16) to remove CTCSS signals then applied to the MAIN unit via J2 (pin 10) as the “VOL” signal.

The “VOL” signal (AF signals) from the RF unit is applied to the [VOL] control (MAIN unit; R58) to control the audio level via the volume mute switch (Q23). The level controlled AF signals are applied to the AF power amplifier (IC9, pin 2) to drive an internal speaker (SP1) via the [SP] jack (J1).

• 2nd IF and demodulator circuits



4-1-6 SQUELCH CIRCUIT (RF AND MAIN UNITS)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) are applied to the active filter section (RF unit; IC2, pin 8). The active filter section amplifies and filters noise components. The filtered signals are applied to the noise detector section and output from pin 14 as the "SQL" signal.

The "SQL" signal from IC2 (pin14) is applied to the CPU (MAIN unit; IC1, pin 59). The CPU analyzes the noise condition and outputs the "RMUT" and "AFON" signals to toggle the volume mute (MAIN unit; Q23) and AF mute (MAIN unit; Q5, Q10, Q11) switches.

• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) passes through the tone low-pass filter (MAIN unit; Q7, Q12) to remove AF (voice) signals and is applied to the CTCSS decoder inside the CPU (MAIN unit; IC1, pin 58) via the "CTCIN" line to control the volume mute and AF mute switches.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies audio signals with pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

AF signals from the internal/external microphone are applied to the microphone amplifier circuit (IC2b) via the microphone mute switch (Q6) and pre-emphasis circuit (R7, C24). The amplified signals are passed through the splatter filter (IC2a) and applied to the modulation circuit in the RF unit via J4 (pin 6) as the MOD signal.

4-2-2 MODULATION CIRCUIT (RF UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone AF signals.

The filtered audio signals from the MAIN unit are passed through the deviation adjustment pot (R50), and are then applied to the modulation circuit (D4, D5) to modulate transmit signals at the VCO circuit (Q6).

The modulated signal is applied to the drive amplifier circuit.

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS (RF UNIT)

The amplifier circuit amplifies the VCO oscillating signal to the output power level.

The signal from the buffer amplifiers (Q7, Q203) is passed through the Tx/Rx switching circuit (D2), and are amplified at the pre-drive (Q8) and drive (Q201) amplifiers. The amplified signal is power-amplified at the power amplifier (Q202) to obtain 500 mW of RF power

The amplified transmit signal is passed through the antenna switching circuit (D7) and low-pass filter, and is then applied to the antenna.

4-3 PLL CIRCUITS (RF UNIT)

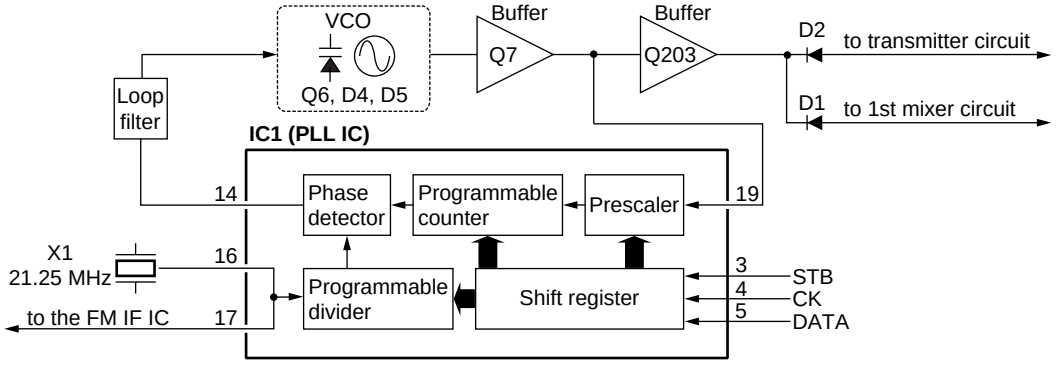
A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit consists of the VCO circuit (Q6). An oscillated signal from the VCO passes through the buffer amplifier (Q7), and is then applied to the PLL IC (IC1, pin19) and prescaled in the PLL IC based on the divided ratio (N-data).

The reference signal is generated at the reference oscillator (X1) and is applied to the PLL IC. The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 13 (IC1). The output signal is passed through the loop filter (R45, C68) and is then applied to the VCO circuit as the lock voltage.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

• PLL circuit



4-4 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
BATT	The voltage from the connected battery cells.
3V	Common 3 V converted from the BATT line at the 3V regulator circuit (IC6). The circuit outputs the voltage regardless of the power ON/OFF condition.
+3V	Common 3 V converted from the BATT line at the +3V regulator circuit (Q25, D4).
R+3	Receive 3 V cotrolled by the R+3 regulator circuit (Q18) using the "RXV" signal from CPU (IC1).
T+3	Transmit 3 V converted from the BATT line at the T+3 regulator circuit (Q27, Q28, Q101, D5) using the "TXV" signal coming from CPU (IC1).

4-5 PORT ALLOCATIONS

4-5-1 CPU (MAIN unit; IC1)

Pin number	Port name	Description
4	SHIFT	Outputs VCO oscillation frequency control signal for Tx/Rx. Low : While transmitting
31	PTT2	Input port for the PTT switch from the external mic jack (MAIN unit; J1). Low : External PTT switch is ON.
34	PTT1	Input port for the internal PTT switch. Low : While PTT switch is pushed.
35	DOWN	Input port for the [DOWN] switch.
36	UP	Input port for the [UP] switch.
37	MODE	Input port for the [MODE] switch.
38	POWSW	Input port for the POWER switch. Low : While POWER switch is pushed.
46	BEEP	Outputs beep audio signal.
48	RMUTE	Outputs volume mute switch (Q23) control signal. High : While squelched
49	AFON	Outputs control signal for the AF amplifier regulator circuit (Q5, Q10, Q11). High: When squelch is open.
50	PLLCK	Outputs clock signal to the PLL IC (RF unit; IC1).
51	PLLDA	Outputs data signals to the PLL IC (RF unit; IC1).
52	PLLST	Outputs strobe signals for the PLL IC (RF unit; IC1).
53	POWER	Outputs control signal for the +3V regulator circuit (MAIN unit; Q25, D4).
54–56	CTCO0–CTCO2	Output port for the CTCSS signals.
57	TXMOD	Outputs control signal for the microphone amplifier (IC2). Low : While microphone amplifier is ON.
58	CTCIN	Input port for the CTCSS decode signals.
59	SQLIN	Input port for squelch level signal.
60	REMIN	Input ports for the control signal from the external remote microphone.
61	BATIN	Input port from the connected battery pack for low battery indication.
62	SENIN	Input port for the RSSI signal from the FM IF IC (RF unit; IC2) to detect receiving signal strength level.
73	EEPCK	Outputs clock signal to the EEPROM (IC3).
74	EEPDA	Outputs data signals to the EEPROM (IC3).
75	PSC	Output port for power save function, applied to VCO regurator circuit (RF unit; Q13, Q14, D8, D9).
76	RXV	Outputs the R+3 regulator control signal (Q25, D4).
77	TXV	Outputs the T+3 regulator control signal (Q27, Q28, Q101, D5).
78	LAMPC	Outputs control signal for LCD backlight. Low : While LCD backlight is ON.
79	MICSW	Outputs internal microphone control signal. High : While internal PTT switch is pushed.
80	MMUTE	Outputs MIC mute signal for RING function. High : While RING signals are output, etc.