Tuning Up Procedure & Operational Manual

Model: ZTE MY39

Version 1.0

8, Feb. 2006

ZTE CORPORATION

1.0 Objective

This document is intended for FCC testing; it mainly includes Tuning Up Procedure and Operational Manual.
It describes the key principles of ZTE MY39; its tuning up, its operation among the interfaces and its antenna features.

2.0 Abbreviation and glossary

CDMA Code Division Multiple Access
EVDO Evolution Data Optimized

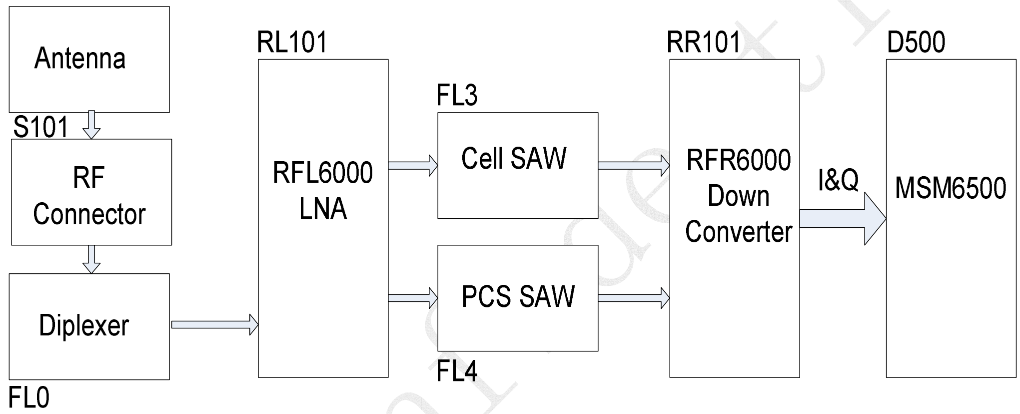
GPS Global positioning system
ARM Advanced RISC Machines
ADC Analog-to-digital converter
AEC Acoustic Echo Cancellation
AGC Automatic Gain Control
ASIC Application Specific Integrated Circuit
CODEC Coder-Decoder
DSP Digital Signal Processor
EBI External Bus Interface
GPIO General-purpose Input/Output
USB Universal Serial Bus
UART Universal Asynchronous Receiver/Transmitter
JTAG Joint Test Action Group (ANSI/ICEEE Std. 1149.1–1990)
PA Power Amplifier
RF Radio Frequency
Tx Transimit
Rx Receive
TCXO Temperature Compensated Crystal Oscillator
LPSDRAM Low Power Synchronous Dynamic Random Access Memory
ZIF Zero Intermediate Frequency

3.1 Principle of Rx Circuit

3.1.1 ZTE MY39 supports quad bands: CDMA 1X CELLULAR 800/PCS 1900, CDMA EVDO CELLULAR 850/PCS 1900.

CELLULAR:	PCS:
Channel Range ： 1-799/991-1023	Channel Range ： 0-1199
Downlink：869MHZ-894MHZ	Downlink：1930MHZ-1990MHZ
Uplink: 824MHZ-849MHZ	Uplink：1850MHZ-1910MHZ
Duplexer：45 MHZ	Duplexer：60 MHZ
Bandwidth：1.25MHZ	Bandwidth：1.25MHZ
Power Range：<=23~30dBm	Power Range：<=23~30dBm

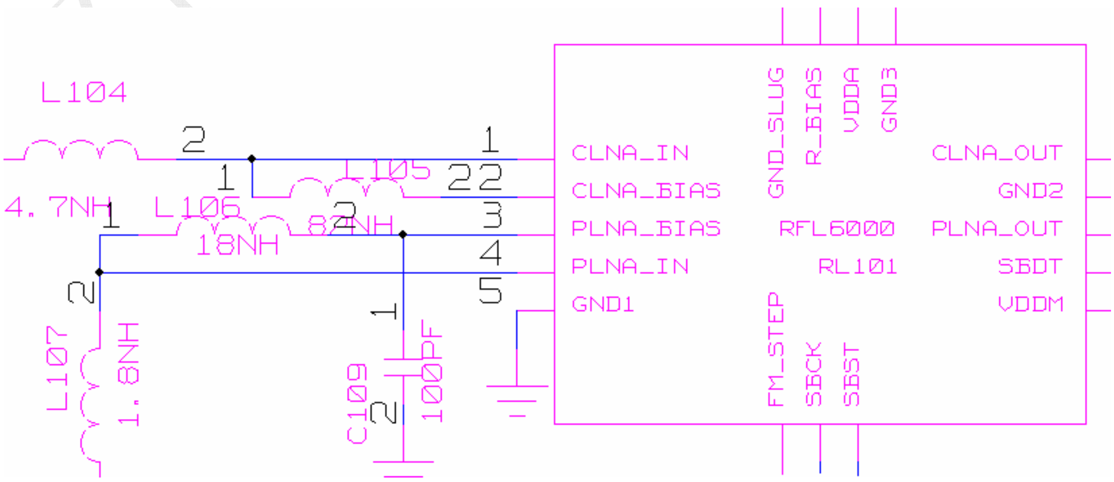
3.1.2 MY39 Block Diagram for Primary Receive Path：



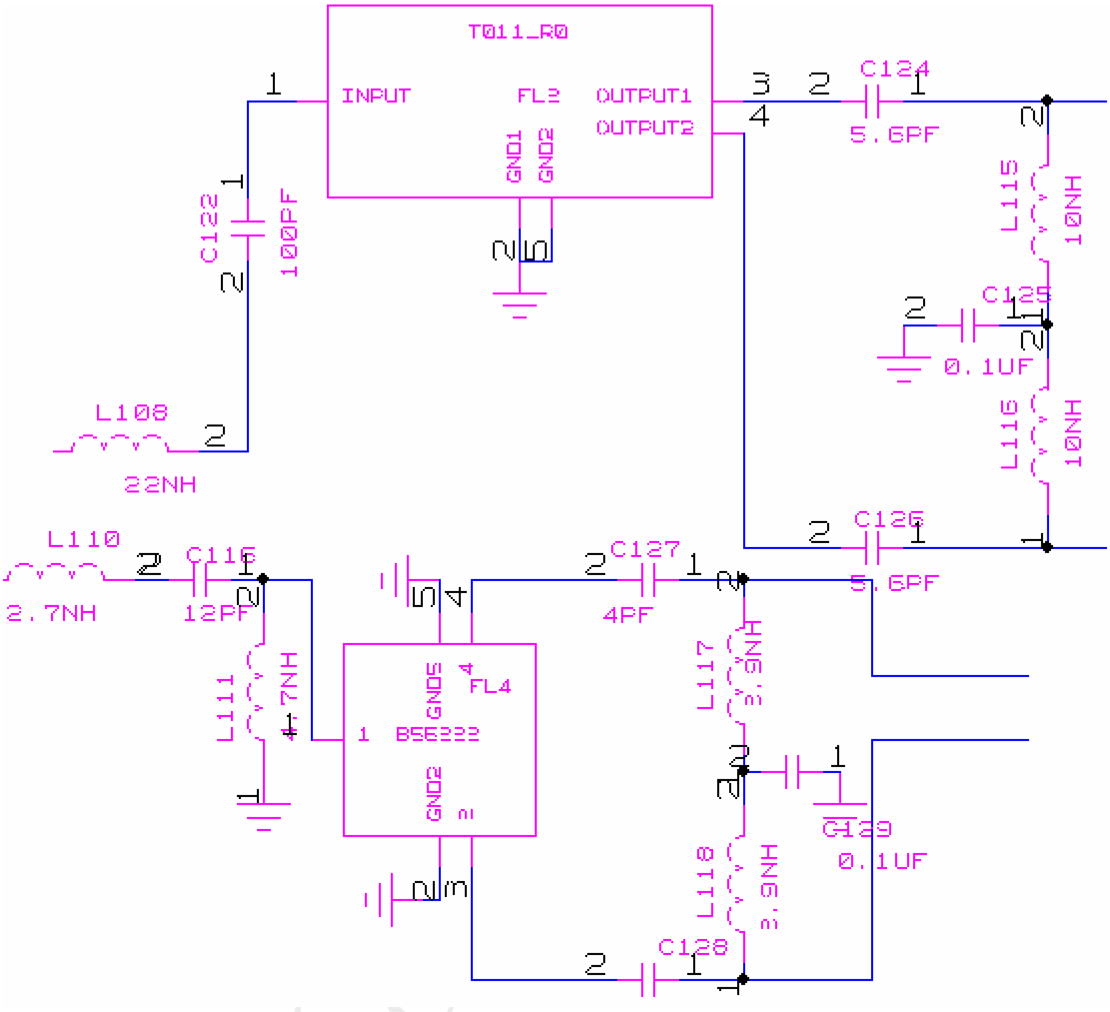
The Block Diagram of RX

3.1.3 Signal is coming from the RF Connector. RF Connector is designed for testing; with the RF cable and equipment our test engineers can analyze the Rx/Tx signal through the RF Connector. The Signal goes into Diplexer from the RF Connector to control the working status.

After the signal comes out from Diplexer, it goes into the related Duplexer. Then the signals coming from two Duplexer go into LNA(RFL6000).



After coming out from LNA, they go into the related RF SAW, and they turn into two signals, espectively.

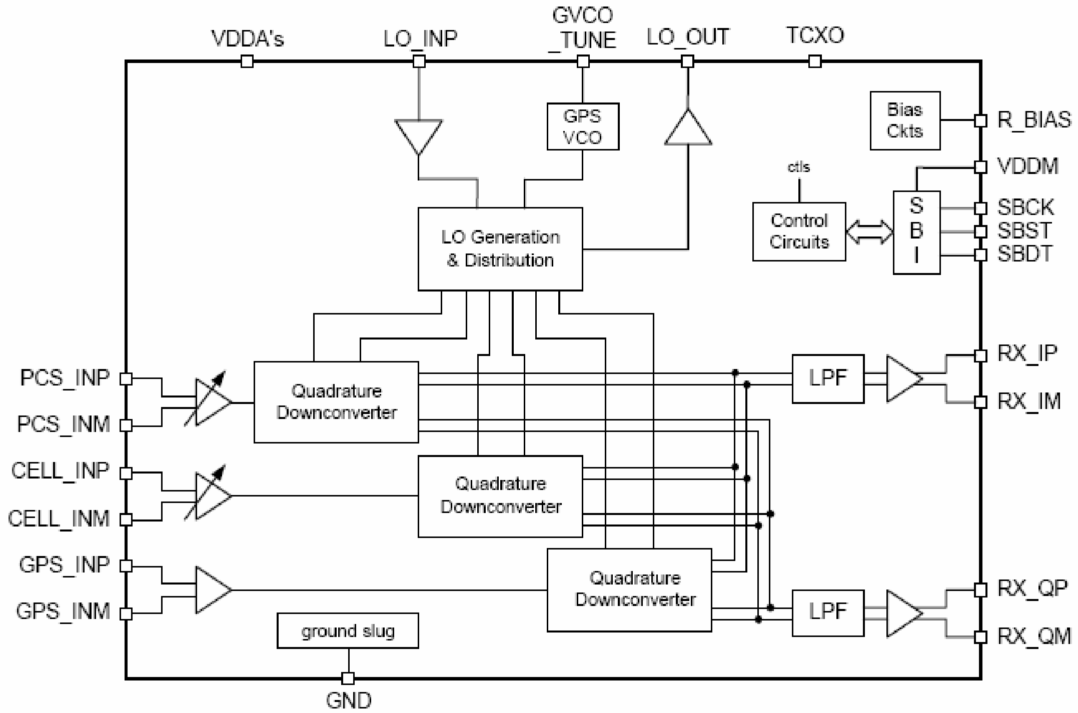


RL101 and RR101 are very important two chip sets. For the receive part, they mainly completes: LNAs（Low Noise Amplifiers）, Down-Converting Mixers, Low Pass Filters and so on.

For example: signal from PCS

path comes out PLNA. After LNA and PCS SAW，A Quadrature Downconvertor mixes down the received signal to baseband. The output baseband signals (IP, IM, QP, QM) after filter and amplifier come out of Pin30、Pin31、Pin33、Pin34 and input to the W21, V21, Y26, Y25 of MSM6500.

The Mixers gains and the LNA gains are set via a standard 3-wire serial bus.



The baseband signals inside the Baseband Processor(MSM6500) will be proceeded with analog to digital conversion、decoding、digital processor、digital to analog conversion, DSP and so on.

3.1.4 The primary receive path circuit tuning up

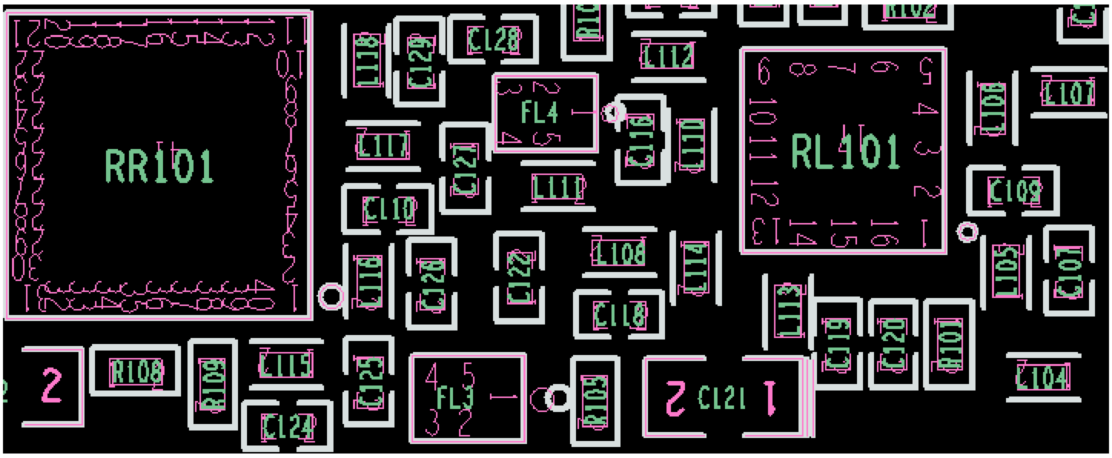
Receiver key parameters include: RX Sensitivity、RX Dynamic range、Single tone desensitization, Intermodulation Spurious Response Attenuation, etc. Here are the equipment we need to analyzer the problems（Such as. CDMA 1X and EVDO）：

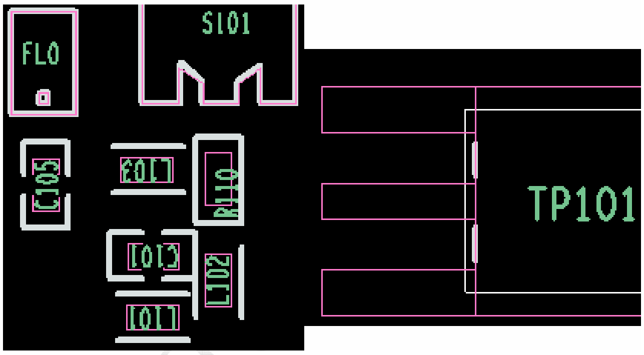
a. Set Agilent8960 to the specific channel and set the basestation output -55dBm.

b. Power on the netcard，the mobile is connected with Agilent8960 by the RF cable，and let the netcard be in the receive & testing mode.

c. Power meter and oscilloscope.

Step 1：According to the signal block diagram test step by step，first get rid of FL0(Diplexer), in this way we can avoid the interference from the backwards and test the input signal to the FL0. If the signal is kind of small, we should check the input to FL0, it might be the problem with L102, R110, C105; otherwise it might be the problem with S101.





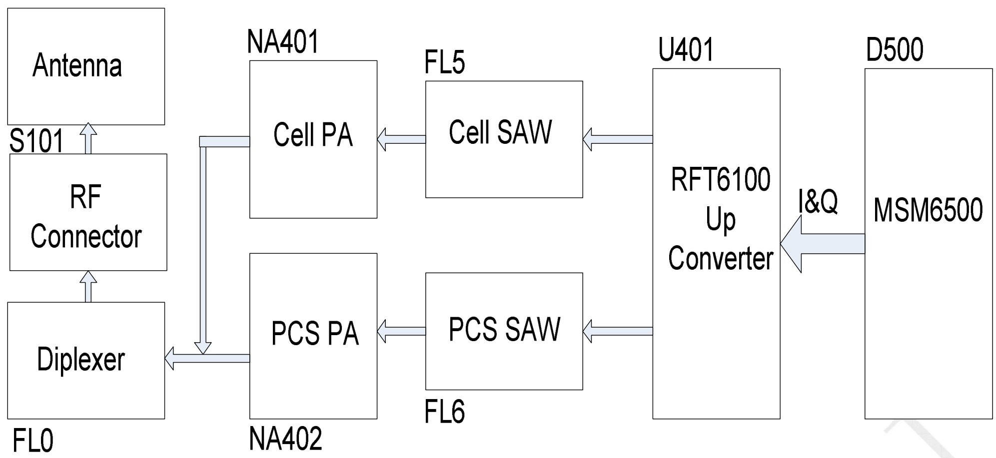
Step 2：Solder the FL0 on，test if its output signal attenuation is big，if it is big, it might have something to do with L102, R110, C105, S101.
Step 3：Test if LNA output signals are normal or not, by testing pin13 or pin11，usually it might be the problem with L104, L105 or L106, L107 if RL101 solder well.
Step 4: Test if RR101 input signals are normal or not, by testing pin40, pin2 or pin6, pin8, usually it might be the problem with FL3, FL4, they solder badly.
Step 5：solder all devices on, If and we cannot find the problem，it should be the problem with PCB.

3.1.5 MY39 Block Diagram for Secondary Receive Path：

The block diagram of secondary receive path is similar to the block diagram of primary receive path, except the two duplexers are substituted by the two filters. In addition to, The output baseband signals (IP, IM, QP, QM) after filter and amplifier come out of Pin30、Pin31、Pin33、Pin34 and input to the W26, V25, U23, U21 of MSM6500.

3.2 Principle of TX Circuit

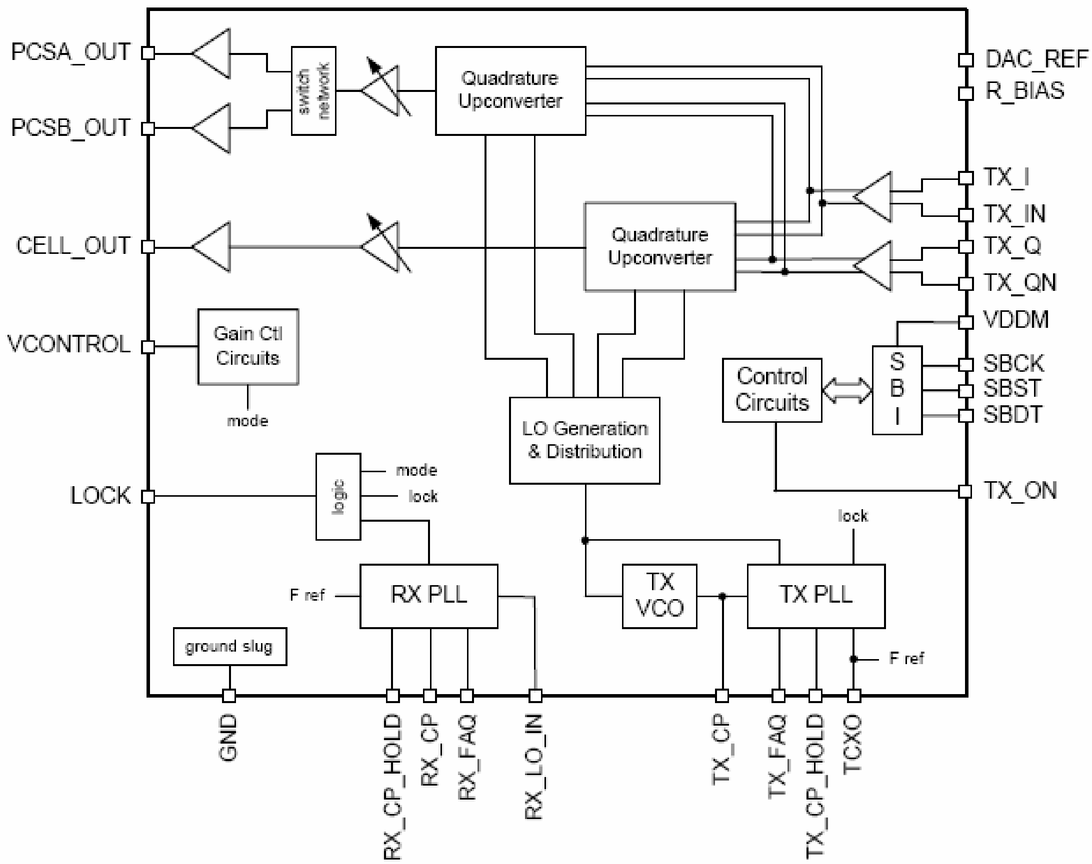
3.2.1 Transmit path circuit block diagram



The Block Diagram of TX

3.2.2 Digital signal by DSP, encoding, D\A conversion into RFT6100(U401), output from B14, A14, B13, A13 of MSM6500 and input into Pin35, Pin36, Pin33, Pin34 of U401.

The transmit section of U401 consists of a quadrature upconvertor, amplifier, a Tx VCO, RX PLL, TX PLL, Gain control circuits and so on. RX VCO is outside it. These components implement a translation loop modulator for directly modulating baseband signals. An integrated power control loop is used to control the power amplifier's output level. RF signal comes out of RF-PA(NA401or NA402) and transmits from the antenna by the RF-Connector.



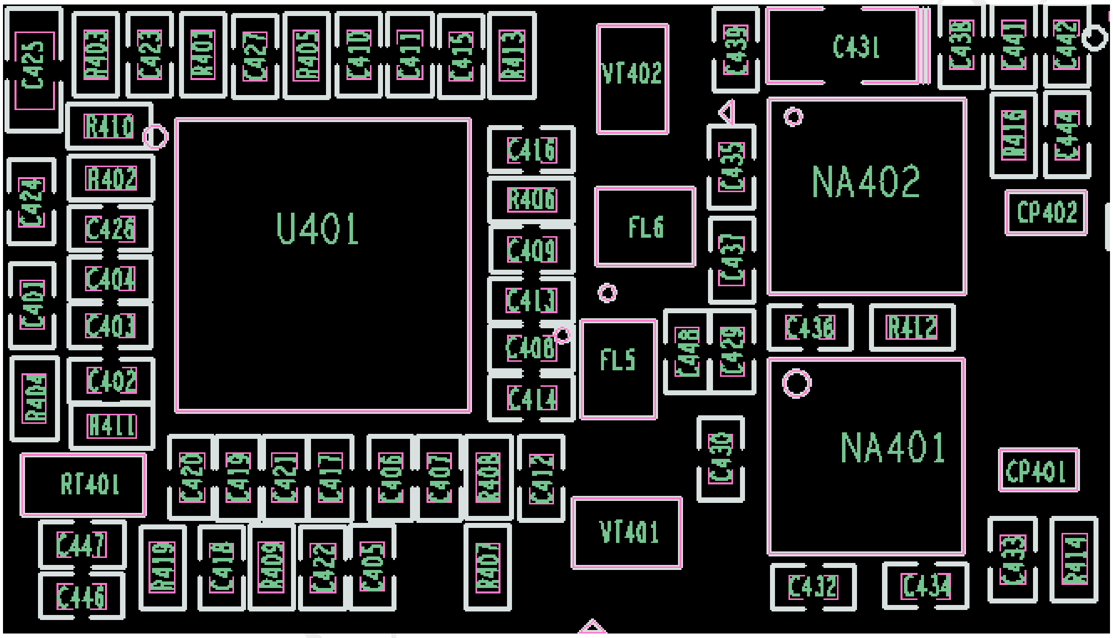
3.2.3 Transmit circuit tuning up

Key parameter of Tx circuit is Frequency Accuracy, Waveform Quality, Range of Closed Loop Power Control, Code Domain Power, MAX. Output Power, Time Response of Open Loop Power Control, etc. Here are the steps to check with the transmit circuit, Following is normal analysis of the circuit, according to failed item to do more analysis. First prepare the equipment we need to analyze the mobiles with problems（Such as. CDMA 1X and EVDO）：

a. Power on the mobile， set the netcard be in the transmit/testing mode using software-QPST(FTM), for example: CDMA 1X 800/1900MHz.

b. Set the spectrum analyzer to the correct center frequency , bandwidth 5MHz、and suitable scan time;

c. Power meter and oscilloscope.



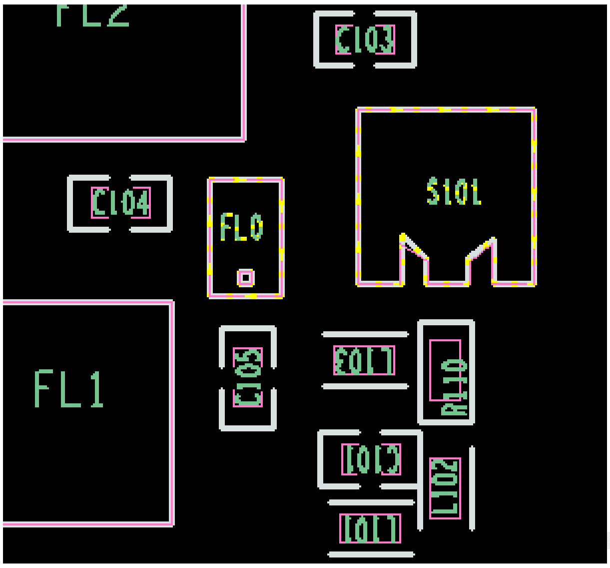
Step1: Measure the I/Q signal from Baseband Processor(D500) to modulation IC (U401). If the I/Q signal is not good, check D500.

Step2: if I/Q signal is good, Measure the output signal of U401, If the signal is not right, check U1000, and parts around U401

Step3: If the signal output from U401 is right, continue to check input signal of PA(NA401 or NA402). If the signal is not right, it might be problem with FL5 or FL6, and parts around it. Measure the Cellular signal at pin4 of CELL PA(NA401); Measure PCS signal at pin2 of PCS PA. If the input signal of PA is right, check output signal of PA. If the output signal is not good check PA or parts around PA. Check the operating voltage “VBAT” and control signal.

Step4: Test Diplexer FL0 input/ output signals. Test C104 when the input signal is PCS; test C105 when the input signal is CELL. For the output signal we could test C103.

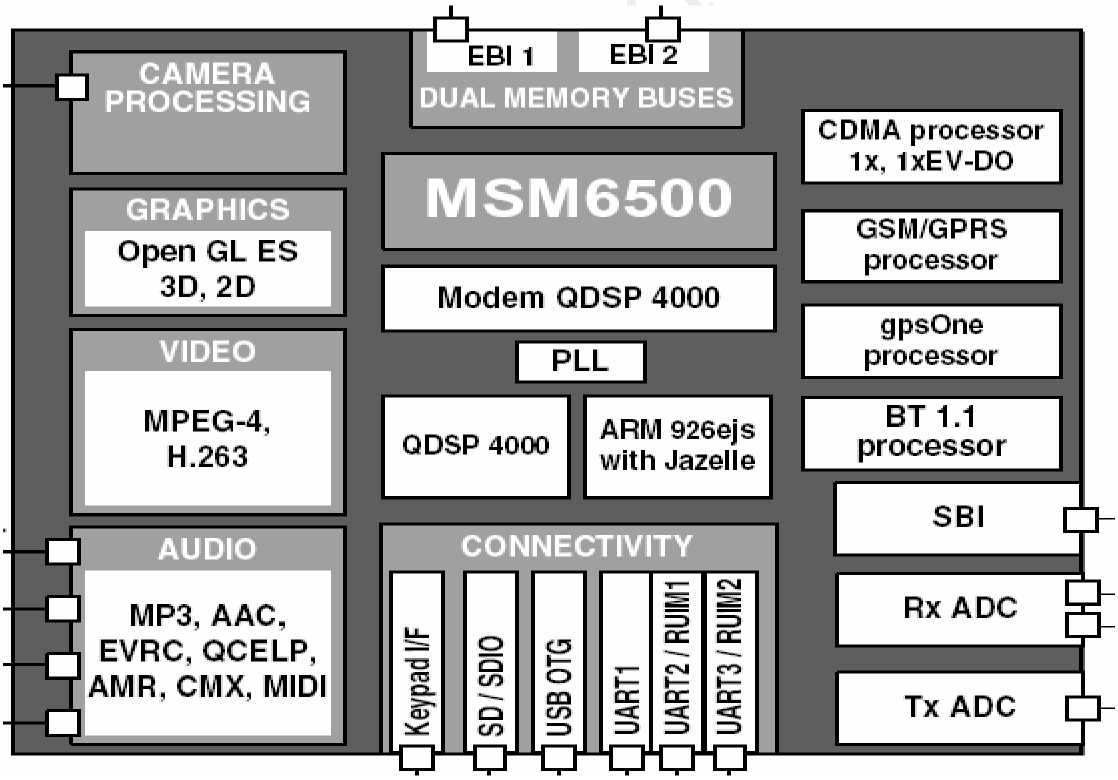
At last, we could test the antenna，if the signal is not good from the antenna check S101，R110，L102.



3.3 Principle of Logic Circuit and tuning up

3.3.1 Principle of the logic circuit:

MSM6500 Functional Block Diagram:



Baseband processor uses MSM6500, which consists of two QDSPs, ARM926EJ-S an d digital, analog and RF interface. It presents address and data bus line to connect to memory chips. It uses RF interface to control and communicate with RF unit, to provide USB controller to communicate with USB transceiver of PM6650. MSM6500 also provide JTAG signal and GPIOs.

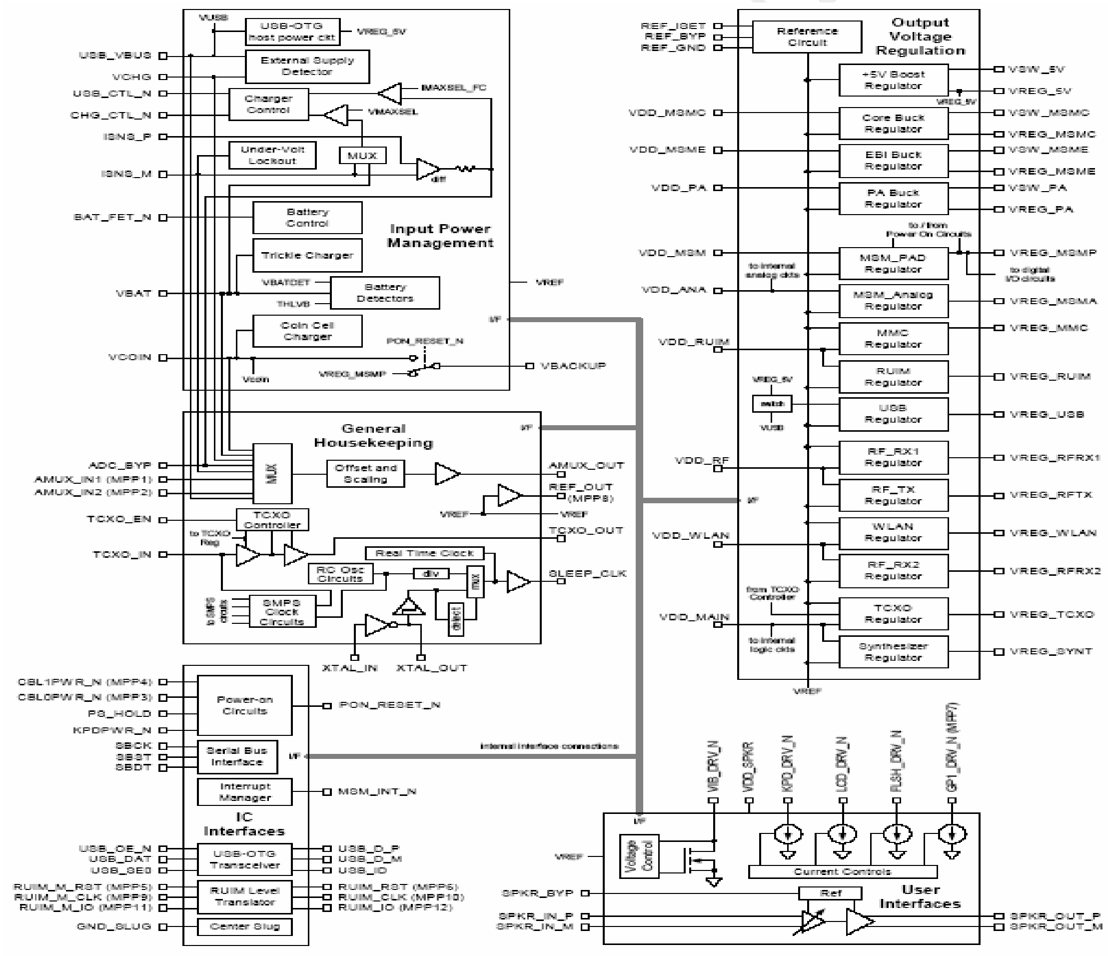
ARM926EJ-S: The main processor of MSM6500 is ARM926EJ-S with 150MHz running rate. It is in charge of the QDSP operation, Voice codec, USB control and other interface operation and it also controls the PM6650 operation and the interfaces to the RF chips.

CDMA Processor: The CDMA Processor in the MSM6500 supports IS-2000 1X and IS-856 1xEV-DO network and it can support CDMA cellular and CDMA PCS operation both.

Memory Interface: MSM6500 has enhanced memory support interface with dual memory buses separating the high-speed memory subsystem (EBI1) from low-speed peripherals (EBI2) such as NAND FLASH memory interface. It has low-power SDRAM (LP-SDRAM) interface and support 16-bit bus and 32-bit bus SDRAM.

USB Controller: MSM6500 integrates a USB On-The-Go controller that supports both unidirectional and bidirectional transceiver interfaces. The USB OTG controller acts as a USB Slave or with limited USB Host functionality. The interface of USB controller connects to the USB transceiver of PM6650.

PM6650 Functional Block Diagram:



Power Management chip uses PM6650 IC, which consists of all voltage supply unit which supplies LDOs and , main clock and slow clock management unit, power on/off management, USB transceiver and so on.

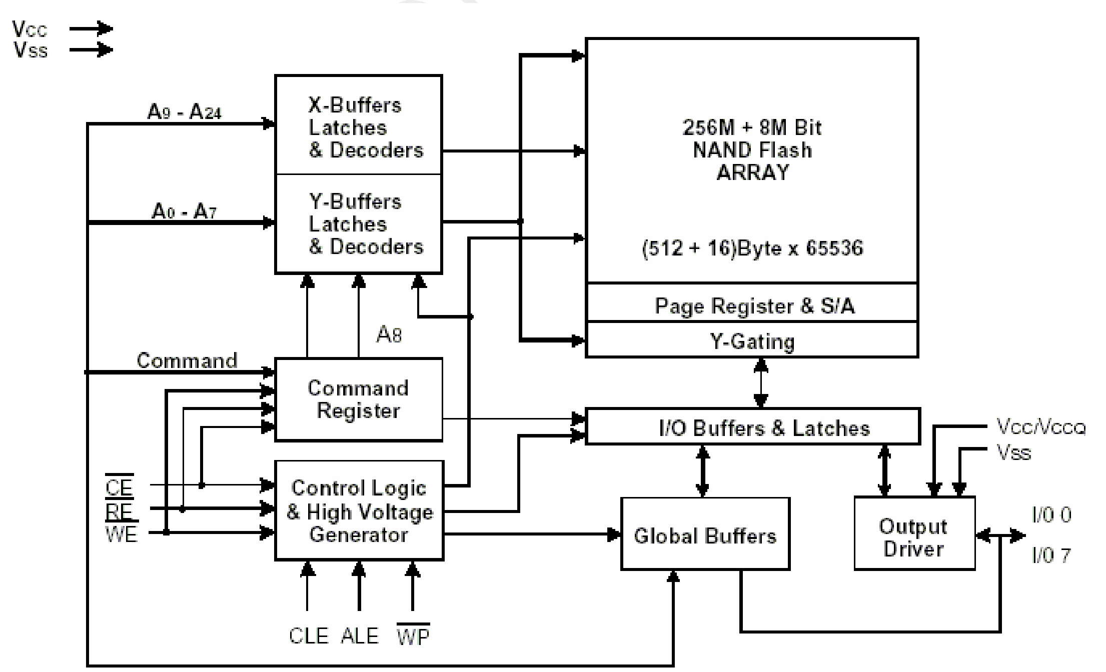
The PM6550 IC includes all the regulated voltages needed for most wireless handset applications(and many other applications). Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, support power management sequencing, and to meet different voltage level requirements. Fifteen voltage regulators are provided—all programmable, all derived from a common bandgap reference circuit.

Two major types of voltage regulator circuits are on-chip: switched-mode power supplies (SMPS) and linear regulators. There are two types of switch-mode power supplies: the boost circuit stepsup its output voltage relative to the input voltage and is rated for 400 mA, and the buck circuits step-down their output voltages and are rated for 500 mA. Three different linear regulators are implemented, categorized by their output current ratings: 300 mA, 150 mA, and 50 mA. Each regulator and SMPS can provide more than its rated output current, though some performance characteristics might be degraded.

The PM6650 IC optimizes TCXO operation during the slotted mode using a dedicated controller that enables and disables appropriate circuits in the proper sequence. The controller is enabled by the TCXO_EN signal (pin 55) from the MSM device, its polarity set by software.

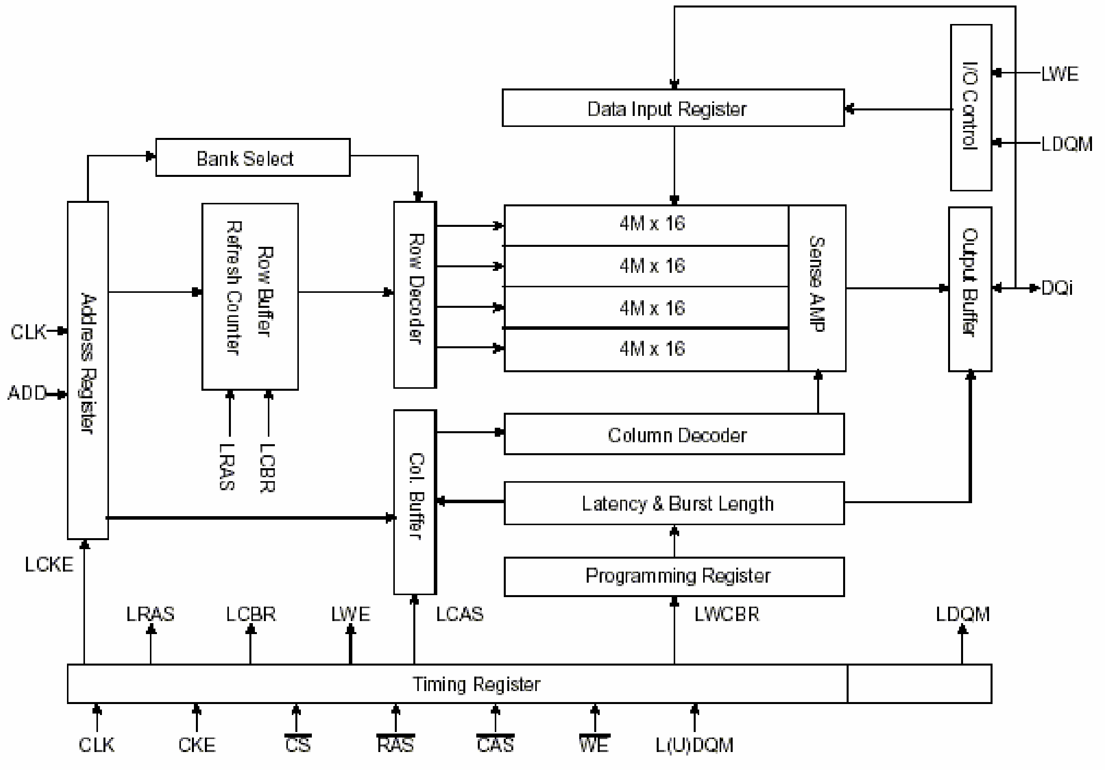
The PM6650 IC includes an integrated universal serial bus/on-the-go (USB-OTG) transceiver onchip. It supports the USB low-speed (1.5 Mb/s) and full-speed (12 Mb/s) modes. The USB-OTG transceiver is used to interface the network's MSM6500 device to uPD720101F1-EA8.

NAND Flash K9F5608Q0C Functional Block Diagram:



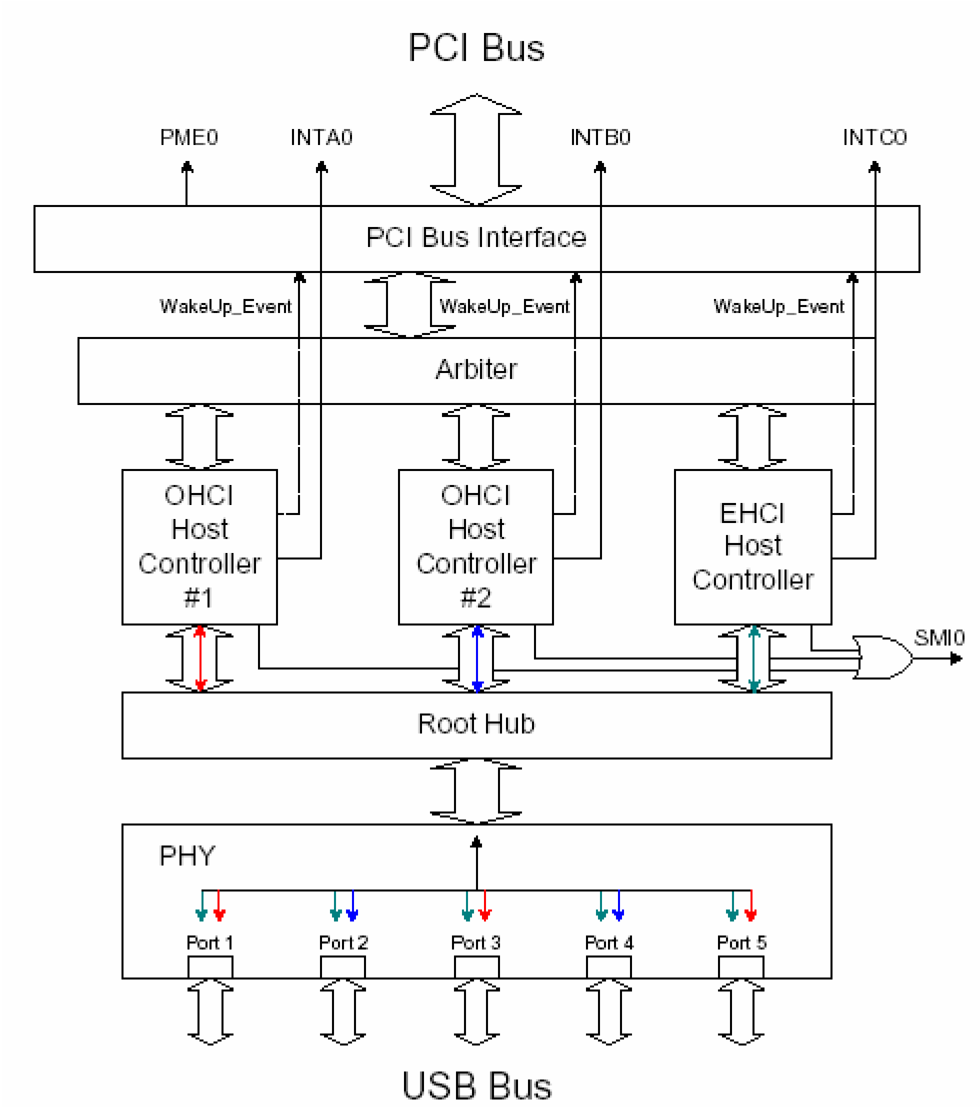
Offered in 32Mx8bit, the K9F5608Q0C is 256M bits with spare 8M bits capacity. The device is offered in 1.8V. Its NAND cell provides the most cost-effective solutIon for the solid state mass storage market. A program operation can be performed in typical 200ms on a 528-byte(X8 device) page and an erase operation can be performed in typical 2ms on a 16K-byte(X8 device) block. Data in the page can be read out at 50ns cycle time per word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F5608Q0C extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

LP-SDRAM K4M28163PF Functional Block Diagram:



The K4M56163PE is 256Mbits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design make a device controlled precisely with the use of system clock and I/O transactions are possible on every clock cycle. The range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

PCI to USB Bridge uPD720101F1 Functional Block Diagram:



PCI to USB bridge chip uses uPD720101F1, which changes the PCI signals to USB signal and which is the communicate bridge between the notebook PC and the CDMA wireless modem.

The uPD720101F1 complies with the Universal Serial Bus Specification Revision 2.0 and Open Host Controller Interface Specification for full-/low-speed signaling and Intel's Enhanced Host Controller Interface Specification for high-speed signaling and works up to 480 Mbps. The uPD720101F1-EA8 is integrated 3 host controller cores with PCI interface and USB2.0 transceivers into a single chip.

uPD720101F1 has 32-bit 33 MHz host interface compliant to PCI Specification release 2.2 and Supports PCI Mobile Design Guide Revision 1.1and PCI-Bus Power Management Interface Specification release 1.1. Its System clock is generated by 48 MHz clock input and the supply of it is 3.3 V power supply, PCI signal pins have 5 V tolerant circuit.

Pins Description of MSM6500:

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
V2	OE1_N	O	SDRAM1_CLK_EN2		P1	O	-	5.4-10.8	Output enable signal (effectively read enable signal). The SDRAM1_CLK_EN2 function allows two SDRAM chips to be put into power down mode independently. See 80-V8946-1. This function is only available on CP90-V9050-x parts. It is not available on CP90-V3195-x parts. This function is selected with EBI1_CFG[27].
V1	A1[24]	O	GPIO[79] SDRAM1_A[0]	B O	P1	BS-PP	-	5.4-10.8	Peripheral address bus.
U4	A1[23]	O	GPIO[78] SDRAM1_DQM[2]	B O	P1	BS-PP	-	5.4-10.8	
T8	A1[22]	O	SDRAM1_D[31]	B	P1	B-K	-	5.4-10.8	
T6	A1[21]	O	SDRAM1_D[30]	B	P1	B-K	-	5.4-10.8	
T4	A1[20]	O	SDRAM1_D[29]	B	P1	B-K	-	5.4-10.8	
R8	A1[19]	O	SDRAM1_D[28]	B	P1	B-K	-	5.4-10.8	
T2	A1[18]	O	SDRAM1_D[27]	B	P1	B-K	-	5.4-10.8	
T1	A1[17]	O	SDRAM1_D[26]	B	P1	B-K	-	5.4-10.8	
R6	A1[16]	O	SDRAM1_D[25]	B	P1	B-K	-	5.4-10.8	
R4	A1[15]	O	SDRAM1_D[24]	B	P1	B-K	-	5.4-10.8	
P11	A1[14]	O			P1	O	-	5.4-10.8	Peripheral address bus, also functions as SDRAM address bus.
P8	A1[13]	O			P1	O	-	5.4-10.8	
P6	A1[12]	O			P1	O	-	5.4-10.8	
P2	A1[11]	O			P1	O	-	5.4-10.8	
P1	A1[10]	O			P1	O	-	5.4-10.8	
N1	A1[9]	O			P1	O	-	5.4-10.8	
N2	A1[8]	O			P1	O	-	5.4-10.8	
N6	A1[7]	O			P1	O	-	5.4-10.8	
N8	A1[6]	O			P1	O	-	5.4-10.8	
N11	A1[5]	O			P1	O	-	5.4-10.8	
M4	A1[4]	O			P1	O	-	5.4-10.8	
M8	A1[3]	O			P1	O	-	5.4-10.8	
L4	A1[2]	O			P1	O	-	5.4-10.8	
L1	A1[1]	O			P1	O	-	5.4-10.8	
L6	D1[15]	B			P1	B-K	-	5.4-10.8	Peripheral data bus, also functions as SDRAM data bus.
L8	D1[14]	B			P1	B-K	-	5.4-10.8	
K4	D1[13]	B			P1	B-K	-	5.4-10.8	
J1	D1[12]	B			P1	B-K	-	5.4-10.8	
K6	D1[11]	B			P1	B-K	-	5.4-10.8	
J2	D1[10]	B			P1	B-K	-	5.4-10.8	
J4	D1[9]	B			P1	B-K	-	5.4-10.8	
H1	D1[8]	B			P1	B-K	-	5.4-10.8	
H4	D1[7]	B			P1	B-K	-	5.4-10.8	
G2	D1[6]	B			P1	B-K	-	5.4-10.8	
J6	D1[5]	B			P1	B-K	-	5.4-10.8	
J8	D1[4]	B			P1	B-K	-	5.4-10.8	
H6	D1[3]	B			P1	B-K	-	5.4-10.8	

Pin #	Native Mode Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol	Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
G4	D1[2]	B			P1	B-K	-	5.4-10.8	
E1	D1[1]	B			P1	B-K	-	5.4-10.8	
F4	D1[0]	B			P1	B-K	-	5.4-10.8	
Y6	XMEM1_CS_N[3]	O	SDRAM1_CS_N[1]	0	P1	BS-PP	-	5.4-10.8	XMEM chip select
Y4	XMEM1_CS_N[2]	O	SDRAM1_CS_N[0]	O	P1	O	-	5.4-10.8	XMEM chip select
AB1	XMEM1_CS_N[1]	O	GPIO[76]	B	P1	BS-PP	-	5.4-10.8	XMEM chip select
W6	XMEM1_CS_N[0]	O			P1	O	-	5.4-10.8	XMEM chip select
AC1	ROM1_CLK	O	SDRAM1_CLK	O	P1	O	-	5.4-10.8	Burst mode flash clock.
G1	ROM1_ADV_N	O	SDRAM1_RAS_N	O	P1	O	-	5.4-10.8	Burst mode flash's address valid signal.
K8	ROM1_WAIT_N	I	SDRAM1_CAS_N	O	P1	BS-PU	-	5.4-10.8	Burst flash ready signal.
H2	PSRAM_CRE	O	SDRAM1_CLK_EN	O	P1	O	-	5.4-10.8	Clock enable signal needed by some PSRAMs. Controlled through the EBI1_PSRAM_CRE register.
SDRAM Interface									
V8	SDRAM1_DQM[3]	O	GPIO[75]	B	P1	BS-PP	-	5.4-10.8	SDRAM byte 3 enable
U4	SDRAM1_DQM[2]	O	GPIO[78] A1[23]	B O	P1	BS-PP	-	5.4-10.8	SDRAM byte 2 enable
M6	SDRAM1_DQM[1]	O	UB1_N	O	P1	O	-	5.4-10.8	SDRAM byte 1 enable
L2	SDRAM1_DQM[0]	O	LB1_N	O	P1	O	-	5.4-10.8	SDRAM byte 0 enable
AC1	SDRAM1_CLK	O	ROM1_CLK	O	P1	O	-	5.4-10.8	SDRAM clock.
H2	SDRAM1_CLK_EN	O	PSRAM_CRE	O	P1	O	-	5.4-10.8	SDRAM clock Enable
V2	SDRAM1_CLK_EN2	O	OE1_N	O	P1	O	-	5.4-10.8	The SDRAM1_CLK_EN2 function allows two SDRAM chips to be put into power down modeindependently. See 80-V8946-1. This function is only available on CP90-V9050-x parts. It is not available on CP90-V3195-x parts. This function is selected with EBI1_CFG[27].
G1	SDRAM1_RAS_N	O	ROM1_ADV_N	O	P1	O	-	5.4-10.8	SDRAM row address strobe.
K8	SDRAM1_CAS_N	O	ROM1_WAIT_N	I	P1	BS-PU	-	5.4-10.8	SDRAM column address strobe.
U8	SDRAM1_WE_N	O	WE1_N	O	P1	O	-	5.4-10.8	SDRAM write enable signal
Y4	SDRAM1_CS_N[0]	O	XMEM1_CS_N[2]	O	P1	O	-	5.4-10.8	SDRAM chip select
Y6	SDRAM1_CS_N[1]	O	XMEM_CS_N[3] GPIO[77]	O B	P1	BS-PP	-	5.4-10.8	SDRAM chip select
V1	SDRAM1_A[0]	O	GPIO[79] A1[24]	B O	P1	BS-PP	-	5.4-10.8	SDRAM address 0
T8	SDRAM1_D[31]	B	A1[22]	O	P1	B-K	-	5.4-10.8	SDRAM chip select GPIO[77] B
T6	SDRAM1_D[30]	B	A1[21]	O	P1	B-K	-	5.4-10.8	
T4	SDRAM1_D[29]	B	A1[20]	O	P1	B-K	-	5.4-10.8	
R8	SDRAM1_D[28]	B	A1[19]	O	P1	B-K	-	5.4-10.8	
T2	SDRAM1_D[27]	B	A1[18]	O	P1	B-K	-	5.4-10.8	
T1	SDRAM1_D[26]	B	A1[17]	O	P1	B-K	-	5.4-10.8	
R6	SDRAM1_D[25]	B	A1[16]	O	P1	B-K	-	5.4-10.8	
R4	SDRAM1_D[24]	B	A1[15]	O	P1	B-K	-	5.4-10.8	
W4	SDRAM1_D[23]	B	GPIO[74]	B	P1	B-K	-	5.4-10.8	
V6	SDRAM1_D[22]	B	GPIO[73]	B	P1	B-K	-	5.4-10.8	
Y2	SDRAM1_D[21]	B	GPIO[72]	B	P1	B-K	-	5.4-10.8	
Y1	SDRAM1_D[20]	B	GPIO[71]	B	P1	B-K	-	5.4-10.8	
W2	SDRAM1_D[19]	B	GPIO[70]	B	P1	B-K	-	5.4-10.8	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol					
W1	SDRAM1_D[18]	B	GPIO[69]	B	P1	B-K	-	5.4-10.8	
V4	SDRAM1_D[17]	B	GPIO[68]	B	P1	B-K	-	5.4-10.8	
U6	SDRAM1_D[16]	B	GPIO[67]	B	P1	B-K	-	5.4-10.8	
External Bus Interface 2 (EBI2)									
AC5	LB2_N	O	A2[0] NAND2_ALE	O O	P2	O	5-9	3-5.4	Low byte enable signal for byte access of 16-bit memory.
AE4	UB2_N	O	NAND2_CLE	O	P2	O	5-9	3-5.4	Upper byte enable signal for byte access of 16-bit memory.
AF4	WE2_N	O			P2	O	5-9	3-5.4	Write enable signal
AF7	OE2_N	O	NAND2_RE_N	O	P2	O	5-9	3-5.4	Output enable signal (effectively read enable signal)
AA15	A2[20]	O	GPIO[34]	B	P2	BS-PP	5-9	3-5.4	Second peripheral address bus
AC13	A2[19]	O			P2	B	5-9	3-5.4	
AF13	A2[18]	O			P2	B	5-9	3-5.4	
AE13	A2[17]	O			P2	O	5-9	3-5.4	
AA13	A2[16]	O			P2	B	5-9	3-5.4	
W13	A2[15]	O			P2	B	5-9	3-5.4	
T13	A2[14]	O			P2	B	5-9	3-5.4	
AC12	A2[13]	O			P2	B	5-9	3-5.4	
AA12	A2[12]	O			P2	B	5-9	3-5.4	
AF11	A2[11]	O			P2	B	5-9	3-5.4	
AE11	A2[10]	O			P2	B	5-9	3-5.4	
W12	A2[9]	O			P2	B	5-9	3-5.4	
AC11	A2[8]	O			P2	B	5-9	3-5.4	
AA11	A2[7]	O			P2	B	5-9	3-5.4	
W11	A2[6]	O			P2	B	5-9	3-5.4	
AC10	A2[5]	O			P2	B	5-9	3-5.4	
AF9	A2[4]	O			P2	B	5-9	3-5.4	
AA10	A2[3]	O			P2	B	5-9	3-5.4	
AE9	A2[2]	O			P2	B	5-9	3-5.4	
W10	A2[1]	O			P2	B	5-9	3-5.4	
AC5	A2[0]	O	LB2_N NAND2_ALE	O O	P2	O	5-9	3-5.4	
AC9	D2[15]	B			P2	B-K	5-9	3-5.4	Second peripheral data bus
AF8	D2[14]	B			P2	B-K	5-9	3-5.4	
AE8	D2[13]	B			P2	B-K	5-9	3-5.4	
AC8	D2[12]	B			P2	B-K	5-9	3-5.4	
AE7	D2[11]	B			P2	B-K	5-9	3-5.4	
AA9	D2[10]	B			P2	B-K	5-9	3-5.4	
W9	D2[9]	B			P2	B-K	5-9	3-5.4	
AA8	D2[8]	B			P2	B-K	5-9	3-5.4	
AC7	D2[7]	B			P2	B-K	5-9	3-5.4	
AF5	D2[6]	B			P2	B-K	5-9	3-5.4	
AC6	D2[5]	B			P2	B-K	5-9	3-5.4	
AE5	D2[4]	B			P2	B-K	5-9	3-5.4	
AA7	D2[3]	B			P2	B-K	5-9	3-5.4	
AF3	D2[2]	B			P2	B-K	5-9	3-5.4	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol					
AD1	D2[1]	B			P2	B-K	5-9	3-5.4	
AB4	D2[0]	B			P2	B-K	5-9	3-5.4	
AF14	LCD2_CS_N	O	GPIO[38]	B	P2	BS-PP	5-9	3-5.4	Peripheral LCD chip select
T14	LCD2_EN	O	GPIO[37]	B	P2	BS-PP	5-9	3-5.4	LCD enable signal
AF16	XMEM2_CS_N[3]	O	GPIO[36]	B	P2	BS-PP	5-9	3-5.4	Peripheral chip select
AC15	XMEM2_CS_N[2]	O	GPIO[35]	B	P2	BS-PP	5-9	3-5.4	Peripheral chip select
AA14	XMEM2_CS_N[1]	O			P2	O	5-9	3-5.4	Peripheral chip select
W14	XMEM2_CS_N[0]	O			P2	O	5-9	3-5.4	Peripheral chip select
NAND Interface									
AE16	NAND2_FLASH_READY	I	GPIO[33]	B	P2	BS-PP	3-5	1.8-3	NAND flash ready input
AC5	NAND2_ALE	O	LB2_N A2[0]	O O	P2	O	5-9	3-5.4	NAND flash address latch enable
AE4	NAND2_CLE	O	UB2_N	O	P2	O	5-9	3-5.4	NAND flash command latch enable
AF7	NAND2_RE_N	O	OE2_N	O	P2	O	5-9	3-5.4	NAND flash read enable
L26	NAND_BOOT_ERR	O	GPIO[95] UART1_DP_TX_DATA	B O	P3	BS-PP	5-9	-	Indicates NAND flash boot error. Powers up as NAND_BOOT_ERR when booting from NAND flash (BOOT_MODE = 1).
User Interface									
R21	KEYSENSE4_N	I	GPIO[48] ETM_TRACE_PKT2	B O	P3	BS-PP	3-6	-	Can be used to sense key contact closure when connected to an external keypad. These pins require an active-low, level-sensitive input signal and may cause an interrupt to the microprocessor. A possible application is detecting KEYSENSE interrupt and sending out drive signals via GPIOs to determine which key was pressed.
R23	KEYSENSE3_N	I	GPIO[47] ETM_TRACE_PKT1	B O	P3	BS-PP	3-6	-	
P16	KEYSENSE2_N	I	GPIO[46] ETM_TRACE_PKT0	B O	P3	BS-PP	3-6	-	
P19	KEYSENSE1_N	I	GPIO[63] ETM_PIPESTAT1	B O	P3	BS-PP	3-6	-	
P21	KEYSENSE0_N	I	GPIO[62] ETM_PIPESTAT0	B O	P3	BS-PP	3-6	-	
L19	RINGER	O	GPIO[18]	B	P3	BS-PP	3-5	-	DTMF tone generator circuit output which selects the pitch and cadence of the subscriber's ring. This output drives the second transducer. Ringer needs a PD on power-up.
UART/UIM Interface									
M21	UART1_RFR_N	O	GPIO[98]	B	P3	BS-PP	3-5	-	UART1 ready-for-receive signal
N16	UART1_CTS_N	I	GPIO[97]	B	P3	BS-PP	3-5	-	UART1 clear-to-send signal
M23	UART1_DP_RX_DATA	I	GPIO[96]	B	P3	BS-PP	3-5	-	UART1 receive serial data input
N21	UART1_DP_RX_DATA	I	USB_DAT_VP I2C_SDA	B B	P3	B-K	4-5	-	UART1 receive serial data input
L26	UART1_DP_TX_DATA	O	GPIO[95] NAND_BOOT_ERR	B O	P3	BS-PP	3-5	-	UART1 transmit serial data output. Boots up as NAND_BOOT_ERR when booting from NAND flash (BOOT_MODE = 1).
N19	UART1_DP_TX_DATA	O	USB_SE0_VM I2C_SCL	B B	P3	B-K	4-5	-	UART1 transmit serial data output
E4	UART2_RFR_N	O	GPIO[91] UIM_CLK	B O	P3	BS-PP	3-5	-	UART2 ready-for-receive signal

Pin #	Native Mode: Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol	Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
G6	UART2_CTS_N	I	GPIO[90] UIM_RESET	B O	P3	BS-HPP	3-5	-	UART2 clear-to-send signal
C1	UART2_DP_RX_DATA	I	GPIO[89] UIM_PWR_EN	B O	P3	BS-PP	3-5	-	UART2 receive serial data input. Must be pulled down.
D1	UART2_DP_TX_DATA	O	GPIO[88] UIM_DATA	B B	P3	BS-HPP	3-5	-	UART2 transmit serial data output.
L25	UART3_RFR_N	O	GPIO[87] UIM2_CLK	B O	P3	BS-PP	3-5	-	UART3 ready-for-receive signal
L23	UART3_CTS_N	I	GPIO[86] UIM2_RESET	B O	P3	BS-HPP	3-5	-	UART3 clear-to-send signal
L21	UART3_DP_RX_DATA	I	GPIO[85] UIM2_PWR_EN	B O	P3	BS-PP	3-5	-	UART3 receive serial data input. Must be pulled down.
M19	UART3_DP_TX_DATA	O	GPIO[84] UIM2_DATA	B B	P3	BS-HPP	3-5	-	UART3 transmit serial data output.
E4	UIM_CLK	O	GPIO[91] UART2_RFR_N	B O	P3	BS-PP	3-5	-	UIM clock. Note that UIM function is driven to/from GPIO registers, not by an MSM core.
G6	UIM_RESET	O	GPIO[90] UART2_CTS_N	B I	P3	BS-HPP	3-5	-	UIM reset. UIM_RESET is high voltage tolerant (3V), and open collector.
C1	UIM_PWR_EN	O	GPIO[89] UART2_DP_RX_DATA	B I	P3	BS-PP	3-5	-	UIM power enable
D1	UIM_DATA	B	GPIO[88] UART2_DP_TX_DATA	B O	P3	BS-HPP	3-5	-	UIM data. UIM_DATA is high voltage tolerant (3V), and open collector.
L25	UIM2_CLK	O	GPIO[87] UART3_RFR_N	B O	P3	BS-PP	3-5	-	UIM2 clock
L23	UIM2_RESET	O	GPIO[86] UART3_CTS_N	B I	P3	BS-HPP	3-5	-	UIM2 reset. UIM2_RESET is high voltage tolerant (3V).
L21	UIM2_PWR_EN	O	GPIO[85] UART3_DP_RX_DATA	B I	P3	BS-PP	3-5	-	UIM2 power enable
M19	UIM2_DATA	B	GPIO[84] UART3_DP_TX_DATA	B O	P3	BS-HPP	3-5	-	UIM2 data. UIM2_DATA is high voltage tolerant (3V).
USB Transceiver Interface									
N21	USB_DAT_VP	B	I2C_SDA UART1_DP_RX_DATA	B I	P3	B-K	4-5	-	Single-ended data. Differential plus (+)
N19	USB_SE0_VM	B	I2C_SCL UART1_DP_TX_DATA	B O	P3	B-K	4-5	-	Single-ended data. Differential minus (-)
N25	USB_OE_TP_N	B			P3	B-K	2-5	-	An active low output used to enable or disable the D+ and D- pins of the transceiver.
N23	USB_RX_DATA	I	GPIO[29]	B	P3	B-PP	3-5	-	Single-ended input from USB transceiver
N26	USB_SUSPEND	O	GPIO[17]	B	P3	B-PP	3-5	-	Suspended state indicator
MMC Interface									
H13	MMC_DATA	B	GPIO[32]	B	P3	BS-HPP	3-5	-	MMC data. High voltage tolerant (3V).
D12	MMC_CLK	O	GPIO[31]	B	P3	BS-PP	3-5	-	MMC clock.
L13	MMC_CMD	B	GPIO[30]	B	P3	BS-HPP	3-5	-	MMC command. High voltage tolerant (3V).
SBI for RTR6300, RFR6000, RFL6000 (first receive chain)									
H26	SBST	O			P3	O	2-5	-	I3Q serial bus start/stop
J23	SBDT	B			P3	B-K	2-5	-	I3Q serial bus data
K21	SBCK	B			P3	B-PP	2-5	-	I3Q serial bus clock
SBI for RFR6000, RFL6000 (second receive chain)									
H18	SBST1	O	GPIO[93]	B	P3	BS-PP	2-5	-	I3Q serial bus start/stop
G26	SBDT1	B	GPIO[1]	B	P3	B-KPU	2-5	-	I3Q serial bus data

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
H25	SBCK1	O	GPIO[0] WDOG_STB	B O	P3	B-PP	2-5	-	I3Q serial bus clock
AUX_SBI for RFT6100									
D11	AUX_SBST	O	GPIO[8] GRFC[5]	B O	P3	B-PP	2-5	-	I3Q serial bus start/stop
A8	AUX_SBDT	B	GPIO[4] GRFC[1]	B	P3	B-PP	2-5	-	I3Q serial bus data
H10	AUX_SBCK	O	GPIO[7] GRFC[4]	B O	P3	B-PP	2-5	-	I3Q serial bus clock
I2C Interface									
J21	I2C_SDA	B	GPIO[26]	B	P3	BS-PP	3-5	-	I2C serial bus data
N21	I2C_SDA	B	USB_DAT_VP UART1_DP_RX_DATA	B I	P3	B-K	4-5	-	I2C serial bus data
J19	I2C_SCL	B	GPIO[27]	B	P3	BS-PP	3-5	-	I2C serial bus clock
N19	I2C_SCL	B	USB_SE0_VM UART1_DP_TX_DATA	B O	P3	B-K	4-5	-	I2C serial bus clock
Bluetooth									
G23	BT_CLK	I	GPIO[25]	B	P3	BS-PP	3-5	-	12 MHz Bluetooth clock
F23	BT_SBST	O	GPIO[24]	B	P3	BS-PP	3-5	-	BT SBI strobe signal
E26	BT_SBCK	O	GPIO[23]	B	P3	BS-PP	3-5	-	BT SBI clock
E25	BT_SBDT	B	GPIO[22]	B	P3	BS-PP	3-5	-	BT SBI input/output data
G21	BT_TX_RX_N	O	GPIO[21]	B	P3	BS-PP	3-5	-	BT Tx/Rx strobe
D26	BT_DATA	B	GPIO[20]	B	P3	BS-PP	3-5	-	BT Tx/Rx data

Camera Interface (ITU656)									
D20	CAMIF_DATA7	I	GPIO[61] ETM_TRACE_PKT15	B O	P3	B-K	3-6	-	Data from the camera module
A22	CAMIF_DATA6	I	GPIO[60] ETM_TRACE_PKT14	B O	P3	B-K	3-6	-	
D21	CAMIF_DATA5	I	GPIO[59] ETM_TRACE_PKT13	B O	P3	B-K	3-6	-	
B22	CAMIF_DATA4	I	GPIO[58] ETM_TRACE_PKT12	B O	P3	B-K	3-6	-	
F20	CAMIF_DATA3	I	GPIO[57] ETM_TRACE_PKT11	B O	P3	B-K	3-6	-	
A23	CAMIF_DATA2	I	GPIO[56] ETM_TRACE_PKT10	B O	P3	B-K	3-6	-	
B23	CAMIF_DATA1	I	GPIO[55] ETM_TRACE_PKT9	B O	P3	B-K	3-6	-	
D22	CAMIF_DATA0	I	GPIO[54] ETM_TRACE_PKT8	B O	P3	B-K	3-6	-	
A24	CAMIF_VSYNC	B	GPIO[16]	B	P3	BS-PP	3-5	-	Input vertical reference signal
E23	CAMIF_HSYNC	B	GPIO[15]	B	P3	BS-PP	3-5	-	Input horizontal reference signal
D25	CAMIF_PCLK	I	GPIO[14]	B	P3	BS-PP	3-5	-	Input pixel clock
H21	CAMIF_PROBE	O	GPIO[13] GP_MN	B O	P3	BS-PP	3-5	-	For debug only
AUX CODEC/PCM/Stereo DAC Interface									
K19	AUX_PCM_CLK	B	GPIO[80] SDAC_CLK	B O	P3	BS-PP	2-5	-	PCM clock for auxiliary CODEC port
J25	AUX_PCM_DOUT	O	GPIO[83] SDAC_DOUT	B O	P3	BS-PP	2-5	-	PCM data output for auxiliary CODEC port

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol					
K23	AUX_PCM_DIN	I	GPIO[82] SDAC_MCLK	B O	P3	BS-PP	2-5	-	PCM data input for auxiliary CODEC port
J26	AUX_PCM_SYNC	O	GPIO[81] SDAC_L_R_N	B O	P3	BS-PP	2-5	-	PCM data strobe for auxiliary CODEC port
K19	SDAC_CLK	O	GPIO[80] AUX_PCM_CLK	B I	P3	BS-PP	2-5	-	PCM clock for stereo DAC port
J25	SDAC_DOUT	O	GPIO[83] AUX_PCM_DOUT	B O	P3	BS-PP	2-5	-	PCM data out for stereo DAC port
K23	SDAC_MCLK	O	GPIO[82] AUX_PCM_DIN	B I	P3	BS-PP	2-5	-	PCM data strobe for stereo DAC port
J26	SDAC_L_R_N	O	GPIO[81] AUX_PCM_SYNC	B O	P3	BS-PP	2-5	-	PCM left/right strobe for stereo DAC port
PA control DAC signals									
P26	PA_POWER_CTL	O			PA_CTL_DAC	AO	-	-	Output from the PA Power Control DAC. Analog pin to control GSM PA. Single ended signal.
General Purpose Pulse Density Modulated Outputs									
A20	GP_PDM2	Z	PA_RANGE1	O	P3	Z-PP	2-5	-	General purpose 8-bit PDM. Clocked at TCXO/4 rate.
H17	GP_PDM1	Z	PA_RANGE0	O	P3	Z-PP	2-5	-	General purpose 8-bit PDM. Clocked at TCXO/4 rate.
F19	GP_PDM0	Z	GPIO[92]	BO	P3	BS-PP	2-5	-	General purpose 16-bit PDM. Clocked at TCXO/4 rate.
General Purpose M/N Counter Clock Outputs									
H21	GP_MN	O	GPIO[13] CAMIF_PROBE		P3	BS-PP	3-5	-	General purpose processor-controlled M/N counter. Clocked at TCXO/4 rate.
C26	GP_CLK	O	GPIO[19] SYNTH_LOCK	B I	P3	B-PP	3-5	-	General purpose PLL-based clock output. Same clock as GP_CLK <D8>
D8	GP_CLK	O	GPIO[44] ETM_PIPESTATOB	B O	P3	BS-PP	3-6	-	General purpose PLL-based clock output. Same clock as GP_CLK <C26>
JTAG Interface									
H15	TRST_N	I			P3	BS-PD	3-5	-	JTAG reset
D16	TCK	I			P3	BS-PU	3-5	-	JTAG clock input
F15	TMS	I			P3	BS-PU	3-5	-	JTAG mode select pin
D15	TDI	I			P3	BS-PU	3-5	-	JTAG data input
F16	TDO	Z			P3	Z	5-9	-	JTAG data output
H16	RTCK	O			P3	O	5-9	-	Driven only by ARM9 JTAG
GSM Interface									
H12	GRFC[10]	O	TX_ON	O	P3	O	3-5	-	TX_ON
D5	GRFC[9]	O	GPIO[12]	B	P3	B-PP	2-5	-	GPS_SEL
B4	GRFC[8]	O	GPIO[11]	B	P3	B-PP	2-5	-	GSM_ANT_SEL2_N
T23	GRFC[7]	O	GPIO[10]	B	P3	B-PP	2-5	-	GSM_ANT_SEL1_N
R19	GRFC[6]	O	GPIO[9]	B	P3	B-PP	2-5	-	GSM_ANT_SEL0_N
D11	GRFC[5]	O	GPIO[8] AUX_SBST	B O	P3	B-PP	2-5	-	TX_VCO_0_EN_N
H10	GRFC[4]	O	GPIO[7] AUX_SBCK	B O	P3	B-PP	2-5	-	TX_VCO_1_EN_N
F10	GRFC[3]	O	GPIO[6]	B	P3	B-PP	2-5	-	UHF_BAND_SEL
D9	GRFC[2]	O	GPIO[5]	B	P3	B-PP	2-5	-	GSM_PA_BAND

Pin #	Native Mode: Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol	Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
A8	GRFC[1]	O	GPIO[4] AUX_SBDT	B B	P3	B-PP	2-5	-	GSM_PA_EN
B8	GRFC[0]	O	GPIO[3]	B	P3	B-PP	2-5	-	UHF_VCO_0_EN
RF Rx Interface									
H9	RX_VCO_SEL	O	GPIO[43] ETM_PIPESTAT1B	B O	P3	BS-PP	3-6	-	Selects which VCO used for RFR6000
A5	UHF_VCO_1_SEL	O	GPIO[28]	B	P3	B-PP	3-5	-	Enables second UHF VCO
TXDAC Interface									
B14	I_OUT	O			DAC	AO	-	-	Non-inverted current mode output from the I transmit DAC.
A14	I_OUT_N	O			DAC	AO	-	-	Inverted current mode output from the I transmit DAC.
B13	Q_OUT	O			DAC	AO	-	-	Non-inverted current mode output from the Q transmit DAC.
A13	Q_OUT_N	O			DAC	AO	-	-	Inverted current mode output from the Q transmit DAC.
F13	DAC_REF	I			DAC	AI	-	-	Reference to set the gain of the I&Q transmit DACs.
RF Tx Interface									
A19	PA_ON1	O	GPIO[2]	B	P3	B-PP	2-5	-	Signal that controls the power amplifier. PA_ON is high only when the RF power amplifier is needed for transmission. Supports up to two power amplifiers. Both PAs are powered off on hardware reset.
B19	PA_ON0	O			P3	O	3-5	-	
H12	TX_ON	O	GRFC[10]	O	P3	O	3-5	-	By using TX_ON, the TX IF can be powered off separately from PA_ON. Since PA requires longer warm-up time, this can save power. This output goes low on hardware reset.
A20	PA_RANGE1	O	GP_PDM2	O	P3	Z-PP	2-5	-	Digital outputs from the transmit AGC circuit which can be used to alter the transmit power amplifier characteristics. These pins default to PA_RANGE functionality.
H17	PA_RANGE0	O	GP_PDM1	O	P3	Z-PP	2-5	-	
F18	TCXO_EN	O	GPIO[94]	B	P3	BS-PP	2-5	-	Enables TCXO and related circuitry.
H14	TRK_LO_ADJ	O			P3	Z-PP	2-5	-	PDM output from the frequency tracking circuit which sets the subscriber VHF and UHF frequencies.
L14	TX_AGC_ADJ	O			P3	Z-PP	2-5	-	PDM output from the transmit AGC circuit to control the transmit output power.
C26	SYNTH_LOCK	I	GPIO[19] GP_CLK	B O	P3	B-PP	3-5	-	Synthesizer lock signal
General Purpose I/O and Interrupt Pins									
M21	GPIO[98]	B	UART1_RFR_N	O	P3	BS-PP	3-5	-	
N16	GPIO[97]	B	UART1_CTS_N	I	P3	BS-PP	3-5	-	
M23	GPIO[96]	B	UART1_DP_RX_DATA	I	P3	BS-PP	3-5	-	
L26	GPIO[95]	B	UART1_DP_TX_DATA NAND_BOOT_ERR	O O	P3	BS-PP	3-5	-	
F18	GPIO[94]	B	TCXO_EN	O	P3	BS-PP	2-5	-	
H18	GPIO[93]	B	SBST1	O	P3	BS-PP	2-5	-	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
F19	GPIO[92]	B	GP_PDM0	Z	P3	BS-PP	2-5	-	
E4	GPIO[91]	B	UART2_RFR_N UIM_CLK	O O	P3	BS-PP	3-5	-	
G6	GPIO[90]	B	UART2_CTS_N UIM_RESET	I O	P3	BS-HPP	3-5	-	
C1	GPIO[89]	B	UART2_DP_RX_DATA UIM_PWR_EN	I O	P3	BS-PP	3-5	-	
D1	GPIO[88]	B	UART2_DP_TX_DATA UIM_DATA	O B	P3	BS-HPP	3-5	-	
L25	GPIO[87]	B	UART3_RFR_N UIM2_CLK	O O	P3	BS-PP	3-5	-	
L23	GPIO[86]	B	UART3_CTS_N UIM2_RESET	I O	P3	BS-HPP	3-5	-	
L21	GPIO[85]	B	UART3_DP_RX_DATA UIM2_PWR_EN	I O	P3	BS-PP	3-5	-	
M19	GPIO[84]	B	UART3_DP_TX_DATA UIM2_DATA	O B	P3	BS-HPP	3-5	-	
J25	GPIO[83]	B	AUX_PCM_DOUT SDAC_DOUT	O B	P3	BS-PP	2-5	-	
K23	GPIO[82]	B	AUX_PCM_DIN SDAC_MCLK	I B	P3	BS-PP	2-5	-	
J26	GPIO[81]	B	AUX_PCM_SYNC SDAC_L_R_N	O B	P3	BS-PP	2-5	-	
K19	GPIO[80]	B	AUX_PCM_CLK SDAC_CLK	B B	P3	BS-PP	2-5	-	
V1	GPIO[79]	B	A1[24] SDRAM1_A[0]	O O	P1	BS-PP	-	5.4-10.8	
U4	GPIO[78]	B	A1[23] SDRAM1_DQM[2]	O O	P1	BS-PP	-	5.4-10.8	
Y6	GPIO[77]	B	XMEM1_CS_N[3] SDRAM1_CS_N[1]	O O	P1	BS-PP	-	5.4-10.8	
AB1	GPIO[76]	B	XMEM1_CS_N[1]	O	P1	BS-PP	-	5.4-10.8	
V8	GPIO[75]	B	SDRAM1_DQM[3]	O	P1	BS-PP	-	5.4-10.8	
W4	GPIO[74]	B	SDRAM1_D[23]	B	P1	B-K	-	5.4-10.8	
V6	GPIO[73]	B	SDRAM1_D[22]	B	P1	B-K	-	5.4-10.8	
Y2	GPIO[72]	B	SDRAM1_D[21]	B	P1	B-K	-	5.4-10.8	
Y1	GPIO[71]	B	SDRAM1_D[20]	B	P1	B-K	-	5.4-10.8	
W2	GPIO[70]	B	SDRAM1_D[19]	B	P1	B-K	-	5.4-10.8	
W1	GPIO[69]	B	SDRAM1_D[18]	B	P1	B-K	-	5.4-10.8	
V4	GPIO[68]	B	SDRAM1_D[17]	B	P1	B-K	-	5.4-10.8	
U6	GPIO[67]	B	SDRAM1_D[16]	B	P1	B-K	-	5.4-10.8	
F8	GPIO[66]	B	ETM_TRACECLK	O	P3	BS-PP	3-6	-	
D18	GPIO[65]	B	ETM_TRACESYNC	O	P3	BS-PP	3-6	-	
F11	GPIO[64]	B	ETM_PIPESTAT2	O	P3	BS-PP	3-6	-	
P19	GPIO[63]	B	KEYSENSE1_N ETM_PIPESTAT1	I O	P3	BS-PP	3-6	-	
P21	GPIO[62]	B	KEYSENSE0_N ETM_PIPESTAT0	I O	P3	BS-PP	3-6	-	
D20	GPIO[61]	B	CAMIF_DATA7 ETM_TRACE_PKT15	I O	P3	B-K	3-6	-	
A22	GPIO[60]	B	CAMIF_DATA6 ETM_TRACE_PKT14	I O	P3	B-K	3-6	-	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
D21	GPIO[59]	B	CAMIF_DATA5 ETM_TRACE_PKT13	I O	P3	B-K	3-6	-	
B22	GPIO[58]	B	CAMIF_DATA4 ETM_TRACE_PKT12	I O	P3	B-K	3-6	-	
F20	GPIO[57]	B	CAMIF_DATA3 ETM_TRACE_PKT11	I O	P3	B-K	3-6	-	
A23	GPIO[56]	B	CAMIF_DATA2 ETM_TRACE_PKT10	I O	P3	B-K	3-6	-	
B23	GPIO[55]	B	CAMIF_DATA1 ETM_TRACE_PKT9	I O	P3	B-K	3-6	-	
D22	GPIO[54]	B	CAMIF_DATA0 ETM_TRACE_PKT8	I O	P3	B-K	3-6	-	
H11	GPIO[53]	B	ETM_TRACE_PKT7	O	P3	BS-PP	3-6	-	
D10	GPIO[52]	B	ETM_TRACE_PKT6	O	P3	BS-PP	3-6	-	
A7	GPIO[51]	B	ETM_TRACE_PKT5	O	P3	BS-PP	3-6	-	
B7	GPIO[50]	B	ETM_TRACE_PKT4	O	P3	BS-PP	3-6	-	
F9	GPIO[49]	B	ETM_TRACE_PKT3	O	P3	BS-PP	3-6	-	
R21	GPIO[48]	B	KEYSENSE4_N ETM_TRACE_PKT2	I O	P3	BS-PP	3-6	-	
R23	GPIO[47]	B	KEYSENSE3_N ETM_TRACE_PKT1	I O	P3	BS-PP	3-6	-	
P16	GPIO[46]	B	KEYSENSE2_N ETM_TRACE_PKT0	I O	P3	BS-PP	3-6	-	
A4	GPIO[45]	B	ETM_TRACESYNC_B	O	P3	BS-PP	3-6	-	
D8	GPIO[44]	B	ETM_PIPESTAT0B GP_CLK	O O	P3	BS-PP	3-6	-	
H9	GPIO[43]	B	RX_VCO_SEL ETM_PIPESTAT1B	O O	P3	BS-PP	3-6	-	
D7	GPIO[42]	B	ETM_PIPESTAT2B	O	P3	BS-PP	3-6	-	
H23	GPIO[41]	B	ETM_GPIO_IRQ_SRC	I	P3	BS-PP	3-5	-	
D6	GPIO[40]	B	ETM_GPIO_CS_N	O	P3	BS-PP	3-5	-	
F7	GPIO[39]	B	ETM_KEYSENSE_IRQ_ SRC	I	P3	BS-PP	3-5	-	
AF14	GPIO[38]	B	LCD2_CS_N	O	P2	BS-PP	5-9	3-5.4	
T14	GPIO[37]	B	LCD2_EN	O	P2	BS-PP	5-9	3-5.4	
AF16	GPIO[36]	B	XMEM2_CS_N[3]	O	P2	BS-PP	5-9	3-5.4	
AC15	GPIO[35]	B	XMEM2_CSN_N[2]	O	P2	BS-PP	5-9	3-5.4	
AA15	GPIO[34]	B	A2[20]	O	P2	BS-PP	5-9	3-5.4	
AE16	GPIO[33]	B	NAND2_FLASH_READY	I	P2	BS-PP	3-5	1.8-3	
H13	GPIO[32]	B	MMC_DATA	B	P3	BS-HPP	3-5	-	
D12	GPIO[31]	B	MMC_CLK	O	P3	BS-PP	3-5	-	
L13	GPIO[30]	B	MMC_CMD	B	P3	BS-HPP	3-5	-	
N23	GPIO[29]	B	USB_RX_DATA	I	P3	B-PP	3-5	-	
A5	GPIO[28]	B	UHF_VCO_1_EN	O	P3	B-PP	3-5	-	
J19	GPIO[27]	B	I2C_SCL	B	P3	BS-PP	3-5	-	
J21	GPIO[26]	B	I2C_SDA	B	P3	BS-PP	3-5	-	
G23	GPIO[25]	B	BT_CLK	I	P3	BS-PP	3-5	-	
F23	GPIO[24]	B	BT_SBST	O	P3	BS-PP	3-5	-	
E26	GPIO[23]	B	BT_SBCK	O	P3	BS-PP	3-5	-	
E25	GPIO[22]	B	BT_SBDT	B	P3	BS-PP	3-5	-	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
G21	GPIO[21]	B	BT_TX_RX_N	O	P3	BS-PP	3-5	-	
D26	GPIO[20]	B	BT_DATA	B	P3	BS-PP	3-5	-	
C26	GPIO[19]	B	SYNTH_LOCK GP_CLK	I O	P3	B-PP	3-5	-	
L19	GPIO[18]	B	RINGER	O	P3	BS-PP	3-5	-	
N26	GPIO[17]	B	USB_SUSPEND	O	P3	B-PP	3-5	-	
A24	GPIO[16]	B	CAMIF_VSYNC	B	P3	BS-PP	3-5	-	
E23	GPIO[15]	B	CAMIF_HSYNC	B	P3	BS-PP	3-5	-	
D25	GPIO[14]	B	CAMIF_PCLK	I	P3	BS-PP	3-5	-	
H21	GPIO[13]	B	GP_MN CAMIF_PROBE	O O	P3	BS-PP	3-5	-	
D5	GPIO[12]	B	GRFC[9]	O	P3	B-PP	2-5	-	
B4	GPIO[11]	B	GRFC[8]	O	P3	B-PP	2-5	-	
T23	GPIO[10]	B	GRFC[7]	O	P3	B-PP	2-5	-	
R19	GPIO[9]	B	GRFC[6]	O	P3	B-PP	2-5	-	
D11	GPIO[8]	B	GRFC[5] AUX_SBST	O O	P3	B-PP	2-5	-	
H10	GPIO[7]	B	GRFC[4] AUX_SBCK	O O	P3	B-PP	2-5	-	
F10	GPIO[6]	B	GRFC[3]	O	P3	B-PP	2-5	-	
D9	GPIO[5]	B	GRFC[2]	O	P3	B-PP	2-5	-	
A8	GPIO[4]	B	GRFC[1] AUX_SBDT	O B	P3	B-PP	2-5	-	
B8	GPIO[3]	B	GRFC[0]	O	P3	B-PP	2-5	-	
A19	GPIO[2]	B	PA_ON1	O	P3	B-PP	2-5	-	
G26	GPIO[1]	B	SBDT1	B	P3	B-KPU	2-5	-	
H25	GPIO[0]	B	SBCK1 WDOG_STB	O O	P3	B-PP	2-5	-	
Analog RF Rx Interface									
W21	I_IP_CH0	I			BBR	AI			Channel 0 differential analog I signal (+)
V21	I_IM_CH0	I			BBR	AI			Channel 0 differential analog I signal (-)
Y26	Q_IP_CH0	I			BBR	AI			Channel 0 differential analog Q signal (+)
Y25	Q_IM_CH0	I			BBR	AI			Channel 0 differential analog Q signal (-)
W26	I_IP_CH1	I			BBR	AI			Channel 1 differential analog I signal (+)
V25	I_IM_CH1	I			BBR	AI			Channel 1 differential analog I signal (-)
U23	Q_IP_CH1	I			BBR	AI			Channel 1 differential analog Q signal (+)
U21	Q_IM_CH1	I			BBR	AI			Channel 1 differential analog Q signal (-)
Internal CODEC Signals									
AE20	MIC1P	I			CDC	AI			Mic 1 input (+)
AF20	MIC1N	I			CDC	AI			Mic 1 input (-)
AC19	MIC2P	I			CDC	AI			Mic 2 input (+)
AA18	MIC2N	I			CDC	AI			Mic 2 input (-)
AE19	AUXIP	I			CDC	AI			Auxiliary input (+)

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
AF19	AUXIN	I			CDC	AI			Auxiliary input (-)
AA19	MICOUTP	O			CDC	AO			Mic output to external Tx high pass filter (+)
W18	MICOUTN	O			CDC	AO			Mic output to external Tx high pass filter (-)
AF22	MICINP	I			CDC	AI			Mic input from external Tx high pass filter (+)
AE22	MICINN	I			CDC	AI			Mic input from external Tx high pass filter (-)
AC20	MICFBP	I			CDC	AI			Mic amp feedback from external Tx high pass filter (+)
AC21	MICFBN	I			CDC	AI			Mic amp feedback from external Tx high pass filter (-)
AF18	EAR1OP	O			EAR	AO			Earphone 1 amplifier output (+)
AC17	EAR1ON	O			EAR	AO			Earphone 1 amplifier output (-)
AA17	AUXOP	O			HPH	AO			Auxiliary output (+)
AC18	AUXON	O			HPH	AO			Auxiliary output (-)
AE23	MICBIAS	O			CDC	AO			Mic bias supply output, no decoupling capacitors
AF24	CCOMP	I			CDC	AI			External decoupling capacitor input for CODEC voltage reference
W15	HPH_R	O			HPH	AO			Stereo headphone right output
W17	HPH_L	O	EAR2O		HPH	AO			Stereo headphone left output
W17	EAR2O	O	HPH_L		HPH	AO			Earphone 2 amplifier output
General-purpose ADC									
AD26	PA_DAC_EXT_REF	I			BBR	AI			External PA DAC reference voltage
AB23	HKAIN[5]	I			BBR	AI			Analog mux input channels to the on-chip house-keeping ADC
AC25	HKAIN[4]	I			BBR	AI			
AC26	HKAIN[3]	I			BBR	AI			
Y21	HKAIN[2]	I			BBR	AI			
AB25	HKAIN[1]	I			BBR	AI			
AA23	HKAIN[0]	I			BBR	AI			
ETM Interface									
F8	ETM_TRACECLK	O	GPIO[66]	B	P3	BS-PP	3-6	-	ETM Debugging Interface. ETM pin functionality selected by the MODE[20] pins.
D18	ETM_TRACESYNC	O	GPIO[65]	B	P3	BS-PP	3-6	-	
F11	ETM_PIPESTAT2	O	GPIO[64]	B	P3	BS-PP	3-6	-	
P19	ETM_PIPESTAT1	O	GPIO[63] KEYSENSE1_N	B I	P3	BS-PP	3-6	-	
P21	ETM_PIPESTAT0	O	GPIO[62] KEYSENSE0_N	B I	P3	BS-PP	3-6	-	
D20	ETM_TRACE_PKT15	O	GPIO[61] CAMIF_DATA7	B I	P3	B-K	3-6	-	
A22	ETM_TRACE_PKT14	O	GPIO[60] CAMIF_DATA6	B I	P3	B-K	3-6	-	
D21	ETM_TRACE_PKT13	O	GPIO[59] CAMIF_DATA5	B I	P3	B-K	3-6	-	
B22	ETM_TRACE_PKT12	O	GPIO[58] CAMIF_DATA4	B I	P3	B-K	3-6	-	

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol					
F20	ETM_TRACE_PKT11	O	GPIO[57] CAMIF_DATA3	B I	P3	B-K	3-6	-	
A23	ETM_TRACE_PKT10	O	GPIO[56] CAMIF_DATA2	B I	P3	B-K	3-6	-	
B23	ETM_TRACE_PKT9	O	GPIO[55] CAMIF_DATA1	B I	P3	B-K	3-6	-	
D22	ETM_TRACE_PKT8	O	GPIO[54] CAMIF_DATA0	B I	P3	B-K	3-6	-	
H11	ETM_TRACE_PKT7	O	GPIO[53]	B	P3	BS-PP	3-6	-	
D10	ETM_TRACE_PKT6	O	GPIO[52]	B	P3	BS-PP	3-6	-	
A7	ETM_TRACE_PKT5	O	GPIO[51]	B	P3	BS-PP	3-6	-	
B7	ETM_TRACE_PKT4	O	GPIO[50]	B	P3	BS-PP	3-6	-	
F9	ETM_TRACE_PKT3	O	GPIO[49]	B	P3	BS-PP	3-6	-	
R21	ETM_TRACE_PKT2	O	GPIO[48] KEYSENSE4_N	B I	P3	BS-PP	3-6	-	
R23	ETM_TRACE_PKT1	O	GPIO[47] KEYSENSE3_N	B I	P3	BS-PP	3-6	-	
P16	ETM_TRACE_PKT0	O	GPIO[46] KEYSENSE2_N	B I	P3	BS-PP	3-6	-	
A4	ETM_TRACESYNC_B	O	GPIO[45]	B	P3	BS-PP	3-6	-	
D8	ETM_PIPESTAT0B	O	GPIO[44]	B	P3	BS-PP	3-6	-	
H9	ETM_PIPESTAT1B	O	GPIO[43] RX_VCO_SEL	B O	P3	BS-PP	3-6	-	
D7	ETM_PIPESTAT2B	O	GPIO[42]	B	P3	BS-PP	3-6	-	
H23	ETM_GPIO_IRQ_SRC	I	GPIO[41]	B	P3	BS-PP	3-5	-	In ETM mode, this pin is an unmaskable interrupt source and should be pulled low.
D6	ETM_GPIO_CS_N	O	GPIO[40]	B	P3	BS-PP	3-5	-	
F7	ETM_KEYSENSE_IRQ_SRC	I	GPIO[39]	B	P3	BS-PP	3-5	-	In ETM mode, this pin is an unmaskable interrupt source and should be pulled low.
Power/Ground									
D2 N4 AB2 AC14 T26 F25 F26 D19 B9 B5	VDD_C								Digital VDD for core logic
E2 P4 AC2 AE14 T25 G25 B20 A9 A6 B6	GND								

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function	Dir-Pol					
F1 F2 M1 M2 U1 U2	VDD_P1								Digital VDD for pad group 1
K1 K2 R1 R2 AA1 AA2	GND								
AE6 AF6 AE12 AF12	VDD_P2								Digital VDD for pad group 2
AE10 AF10 AE15 AF15	GND								
R25 R26 K25 K26 A17 B17 A12 B12 A3	VDD_P3								Digital VDD for pad group 3
M25 M26 A21 B21 A15 B15 A10 B10	GND								
AA20	VDD_A CDC								Analog VDD for the Codec
AC22	GND_RET								Ground return for the Codec. Decoupling capacitor is connected between CCOMP and GND_RET.
D13	VDD_A DAC								Analog VDD for the TX DAC
W16	VDD_A EAR								Analog VDD for earphone amplifier
AC16	VDD_A HPH								Analog VDD for stereo DAC
P25	VDD_A PA_CTL_DAC								Analog VDD for PA control DAC
D17	VDD_A PLL								Analog VDD for the digital clock PLLs
U19 T19 W25 T21	VDD_A BBR								Analog VDD for the baseband sigma-delta modulator and HKADC

Pin #	Native Mode				Volt	Pad Type	2.6V Drive (mA)	1.8V Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Function (SURF Function)	Dir-Pol					
AF23 D14 AE18 AB26 AA16 P23 B18 F17 V19 V23 W23 V26	GND								
A1 A2 A25 A26 B1 B2 B3 B24 B25 B26	dnc								Many dnc pins are shorted together internally. Can be left unconnected or connected to ground for improved thermal flow and reduced RFI.
C2 C25 D4 D23 F6 F21 H8 H19 K101	dnc								Many dnc pins are shorted together internally. Can be connected to ground for improved thermal flow and reduced RFI.
L11 L12 L15 L16 M11 M12 M13 M14 M15 M16	dnc								Many dnc pins are shorted together internally. These centrally located dnc pins should be connected to ground for improved thermal flow and reduced RFI.
N12 N13 N14 N15 P12 P13 P14 P15 R11 R12	dnc								Many dnc pins are shorted together internally. These centrally located dnc pins should be connected to ground for improved thermal flow and reduced RFI.
R13 R14 R15 R16 T11 T12 T15 T16	dnc								Many dnc pins are shorted together internally. These centrally located dnc pins should be connected to ground for improved thermal flow and reduced RFI.
W8 W19 AA6 AA21 AC4 AC23 AD2 AD25 AE1 AE2	dnc								Many dnc pins are shorted together internally. Can be left unconnected or connected to ground for improved thermal flow and reduced RFI.
AE3 AE24 AE25 AE26 AF1 AF2 AF25 AF26	dnc								Many dnc pins are shorted together internally. Can be left unconnected or connected to ground for improved thermal flow and reduced RFI.

Pins Description of PM6650:

Pin	Pin name	Type	Pin description
General housekeeping (GH)			
1	ADC_BYP	AI	An internal series resistor and an external shunt capacitor at this pin create a lowpass filter for the sensed current signal into the analog multiplexer. Connect a 0.1 µF capacitor to ground.
44	XTAL_IN	AI	Connect the 32.768 kHz crystal across these pins with capacitors from each pin to ground. Capacitor values depend upon the crystal. An external 32.768 kHz oscillator module may be used.
46	XTAL_OUT	AO	
45	SLEEP_CLK	DO	Buffered 32.768 kHz sleep clock signal; connect to MSM device sleep clock input.
58	TCXO_IN	AI	Input from the handset VCTCXO - analog (sinusoidal) or CMOS logic levels. External AC-coupling required (100 pF).
55	TCXO_EN	DIS	Control signal that enables TCXO controller tasks.
53	TCXO_OUT	AO	Buffered and validated VCTCXO output clock signal - CMOS logic levels compatible with MSM devices.
70	AMUX_IN1 (MPP1)	AI	This is a multi-purpose pin whose intended function is the first external input to the analog multiplexer (battery ID). This pin is paired with MPP2 (pin 72). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
72	AMUX_IN2 (MPP2)	AI	This is a multi-purpose pin. The intended function is the second external input to the analog multiplexer (temperature sensor). This pin is paired with MPP1 (pin 70). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
82	AMUX_OUT	AO	Output of the analog multiplexer. Connect directly to one of the MSM HKADC input pins.
80	REF_OUT (MPP8)	AO	This is a multi-purpose pin. The intended function is a buffered version of the internal voltage reference. Typically, it is used for GSM PA reference voltage. This pin is paired with MPP7 (pin 21). Further descriptions of multipurpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.

IC interfaces (ICIs)			
13	USB_OE_N	DI	USB output enable signal (active LOW); driven by an MSM GPIO pin programmed for the USB_TX_OE_N function.
17	USB_DAT	DI, DO	Plus (+) line of the digital-differential, bi-directional USB signal to/from the MSM device. This line complements pin 19 (USB_SE0). Signal levels are translated between MSM and USB domains within the PM6650 IC.
19	USB_SE0	DI, DO	Minus (-) line of the digital-differential, bi-directional USB signal to/from the MSM device. This line complements pin 17 (USB_DAT). Signal levels are translated between MSM and USB domains within the PM6650 IC.
11	USB_ID	AI	Analog input used to sense whether a peripheral device is connected, and if connected, to determine the peripheral type.

Pin	Pin name	Type	Pin description
18	USB_D_P	DIS, DO, AO	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device. This line complements pin 20 (USB_D_M). Inputs are Schmitt-triggered levels; outputs can be configured as digital logic levels or analog (audio) signals.
20	USB_D_M	DIS, DO, AO	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device. This line complements pin 19 (USB_D_P). Inputs are Schmitt-triggered levels; outputs can be configured as digital logic levels or analog (audio) signals.
24	KPDPWR_N	DIS	Connect this pin to the keypad power button; it is pulled-up internally. Pulling this pin low triggers a power-on sequence.
57	PS_HOLD	DI	Connect this pin to the MSM PS_HOLD output pin. During a PM6650 power-on sequence the MSM device must drive this signal high before an internal counter expires or the PM6650 IC will return the handset to the off state. Once the PM6650 IC is powered on, the MSM device keeps the PM6650 IC on by continuing to drive this signal high. The MSM device requests the PM6650 IC to power-down the handset by driving this signal low.
66	CBL1PWR_N (MPP4)	DIS	These two pins are multi-purpose pins. Their intended function is to recognize a serial cable insertion and initiate the power-on sequence. Both pins are pulled-up internally; both must be pulled to logic low to initiate the power-on sequence. An interrupt is generated for any logic level transition on either pin. These two MPP pins are paired together. Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
68	CBL0PWR_N (MPP3)	DIS	
9	PON_RESET_N	DO	Connect this signal to the MSM RES_IN input pin. During a PM6650 power-on sequence this signal is driven low to initiate an MSM power-on reset. This signal is driven high when an internal counter times out, releasing the MSM power-on reset command.
30	RUIM_M_IO (MPP11)	DI, DO	This is a multi-purpose pin. The intended function is the bi-directional RUIM data on the MSM-side of the RUIM level translator. Pulled-up internally to either VREG_MSME or VREG_MSMP (configurable). This pin is paired with MPP12 (pin 26). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
26	RUIM_IO (MPP12)	DI, DO	This is a multi-purpose pin. The intended function is the bi-directional RUIM data on the RUIM-side of the RUIM level translator. Pulled-up internally to VREG_RUIM. This pin is paired with MPP11 (pin 30). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
34	RUIM_M_CLK (MPP9)	DI	This is a multi-purpose pin. The intended function is the RUIM clock input on the MSM-side of the RUIM level translator. Logic levels are set by either VREG_MSME or VREG_MSMP (configurable). This pin is paired with MPP10 (pin 38). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.

Pin	Pin name	Type	Pin description
38	RUIM_CLK (MPP10)	DO	This is a multi-purpose pin. The intended function is the RUIM clock output on the RUIM-side of the RUIM level translator. Logic levels are set by VREG_RUIM. This pin is paired with MPP9 (pin 34). Further descriptions of multipurpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
40	RUIM_M_RST (MPP5)	DI	This is a multi-purpose pin. The intended function is the RUIM reset input on the MSM-side of the RUIM level translator. Logic levels are set by either VREG_MSME or VREG_MSMP (configurable). This pin is paired with MPP6 (pin 43). Further descriptions of multipurpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
43	RUIM_RST (MPP6)	DO	This is a multi-purpose pin. The intended function is the RUIM reset output on the RUIM-side of the RUIM level translator. Logic levels are set by VREG_RUIM. This pin is paired with MPP5 (pin 40). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
47	SBDT	DIS, DO	Bi-directional SBI data signal; connect to the MSM SBDT pin. This bus is shared with RFICs.
49	SBCK	DIS	SBI clock signal; connect to the MSM SBCK pin. This bus is shared with RFICs.
51	SBST	DIS	SBI strobe signal; connect to the MSM SBST pin. This bus is shared with RFICs.
59	MSM_INT_N	DO	PM6650 interrupt statuses are reported to the MSM device using this signal. Logic low signals that an interrupt event has occurred. The signal stays low until all interrupts are cleared or masked by the MSM device.
slug	GND_SLUG	P	Primary IC ground; solder directly to PCB surface ground then connect directly to PCB internal ground plane using many vias.

Input power management (IPM)			
2	VCHG	AI	A valid analog voltage at this pin is recognized by the PM6650 IC to be an external supply, and factors into the IC's power management operating mode. Connect an immediate 1.0 F capacitor to ground and a 10k resistor to ground.
16	USB_VBUS	AI, AO	This pin is configured as an analog input or an analog output depending upon the type of peripheral device connected. Connect an immediate 4.7 F capacitor to ground and a 47k- resistor to ground.
3	ISNS_P	AI	The positive current sensor input—connect to the pass transistor side of the sense resistor.
5	ISNS_M	AI	The negative current sensor input—connect to the V_{DD} side of the sense resistor. Also used to monitor and/or regulate the V_{DD} voltage.
4	CHG_CTL_N	AO	Control signal for the external pass transistor—a low voltage turns on the pass transistor. This signal is pulled-up internally to V_{CHG} or V_{DD} depending upon the selected PM6650 operating mode.
15	USB_CTL_N	AO	Control signal for the external USB pass transistor—a low voltage turns on the pass transistor. This signal is pulled-up internally to the higher of two voltages, USB_VBUS or V_{DD}.
6	VBAT	AI	Monitors the battery voltage; connect directly to the battery plus (+) terminal.

Pin	Pin name	Type	Pin description
60	VCOIN	AI	Connection to the optional coin cell. If present, provides backup power to the crystal oscillator and real time clock circuits to maintain time and alarm functions if a valid external supply or main battery is not connected.
7	BAT_FET_N	AO	Control signal to the external battery MOSFET; connect directly to its gate. The resulting operation depends upon whether an external supply is present—the battery can charge or provide phone power through the MOSFET.
48	VBACKUP	AO	Connect this pin to the SRAM supply pin(s). An internal switch determines the SRAM power source as follows: ▪ VREG_MSMP powers SRAM when the PM6650 IC is on (when PON_RESET_N is high). ▪ The coin cell (VCOIN) powers SRAM when the PM6650 IC is in one of its off states.

Output voltage regulation (OVR)			
29	VDD_PA	P	Input supply voltage for the PA buck converter circuits. See note 1. In addition, bypass this pin with a 4.7 F capacitor.
33	VDD_MSMC	P	Input supply voltage for the MSMC buck converter circuits. See note 1. In addition, bypass this pin with a 4.7 F capacitor.
35	VDD_MSME	P	Input supply voltage for the MSME buck converter circuits. See note 1. In addition, bypass this pin with a 4.7 F capacitor.
41	VDD_RUIM	P	Input supply voltage for the RUIM and MMC linear regulator circuits. See note 1.
52	VDD_MSM	P	Input supply voltage for the MSMP linear regulator circuits. See note 1.
54	VDD_ANA	P	Input supply voltage for the MSMA linear regulator circuits. See note 1.
65	VDD_WLAN	P	Input supply voltage for the WLAN and RFRX2 linear regulator circuits. See note 1.
71	VDD_RF	P	Input supply voltage for the RFRX1 and RFTX linear regulator circuits. See note 1.
83	VDD_MAIN	P	Input supply voltage for the SYNT and TCXO linear regulator circuits and PM6650 logic circuits. See note 1. In addition, bypass this pin with a 0.1 F capacitor.
14	VSW_5V	AO	The switching output of the +5V boost (step-up) switched-mode power supply (SMPS).
12	VREG_5V	AI	Senses the regulated output of the +5V boost (step-up) SMPS. Bypass this pin with a 4.7 F ceramic capacitor.
27	VSW_PA	AO	The switching output of the PA buck (step-down) SMPS.
28	VREG_PA	AI	Senses the regulated output of the PA buck (step-down) SMPS. Bypass this pin with a 4.7 F ceramic capacitor.
31	VSW_MSMC	AO	The switching output of the MSMC buck (step-down) SMPS.
32	VREG_MSMC	AI	Senses the regulated output of the MSMC buck (step-down) SMPS. Bypass this pin with a 4.7 F ceramic capacitor.
37	VSW_MSME	AO	The switching output of the MSME buck (step-down) SMPS.
36	VREG_MSME	AI	Senses the regulated output of the MSME buck (step-down) SMPS. Bypass this pin with a 4.7 F ceramic capacitor.

Pin	Pin name	Type	Pin description
10	VREG_USB	AO	Linear regulator output intended to power the internal USB transceiver; not recommended as a general purpose regulated power source. Bypass this pin with a 1.0 F ceramic capacitor. Power to the USB regulator circuits is either VREG_5V or USB_VBUS (software selectable).
39	VREG_MMC	AO	Linear regulator output intended to power MMC circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_RUIM voltage powers the MMC regulator circuits.
42	VREG_RUIM	AO	Linear regulator output intended to power RUIM circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_RUIM voltage powers the RUIM regulator circuits.
50	VREG_MSMP	AO	Linear regulator output intended to power the MSM peripheral functions; not recommended as a general-purpose regulated power source. Bypass this pin with a 4.7 F ceramic capacitor and connect directly to MSM V_{DDP} pins. The VDD_MSM voltage powers the MSMP regulator circuits.
56	VREG_MSMA	AO	Linear regulator output intended to power the MSM device analog functions; not recommended as a general-purpose regulated power source. Bypass this pin with a 4.7 F ceramic capacitor and connect directly to MSM V_{DDA} pins. The VDD_ANA voltage powers the MSMA regulator circuits.
64	VREG_WLAN	AO	Linear regulator output intended to power WLAN or Bluetooth circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_WLAN voltage powers the WLAN regulator circuits.
67	VREG_RFRX2	AO	Linear regulator output intended to power diversity receiver circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_WLAN voltage powers the RFRX2 regulator circuits.
69	VREG_RFRX1	AO	Linear regulator output intended to power primary receiver circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_RF voltage powers the RFRX1 regulator circuits.
73	VREG_RFTX	AO	Linear regulator output intended to power transmitter circuits or others. Bypass this pin with a 2.2 F ceramic capacitor. The VDD_RF voltage powers the RFTX regulator circuits.
81	VREG_SYNT	AO	Linear regulator output intended to power frequency synthesizer circuits or others. Bypass this pin with a 1.0 F ceramic capacitor. The VDD_MAIN voltage powers the SYNT regulator circuits.
84	VREG_TCXO	AO	Linear regulator output intended to power VCTCXO circuits or others. Bypass this pin with a 1.0 F ceramic capacitor. The TCXO regulator circuits are powered by the VDD_MAIN voltage and are enabled by the TCXO controller.
61	REF_ISET	AI	Connect this pin to a 121k, 1% resistor to ground for internal reference generation.
63	REF_BYP	AI	Connect this pin to a 0.1 µF ceramic capacitor to ground—as directly to pin 62 (REF_GND) as possible. This capacitor is part of a lowpass filter for the internal reference. Do not load this pin.
62	REF_GND	AI	Ground for the internal reference—connect as directly as possible to the handset's reference ground.

Pin	Pin name	Type	Pin description
User interfaces (UIs)			
8	FLSH_DRV_N	AO	Programmable current sink intended to support a camera flash strobe or other functions. This driver has a programmable timer, generates high-current pulses to drive several white LEDs in parallel (each powered off +5V), and is suitable for a digital camera flash strobe.
21	GP1_DRV_N (MPP7)	AO	This is a multi-purpose pin whose intended function is the programmable current sink intended to support general purpose LED or backlight devices. This pin is paired with MMP2 (pin 80). Further descriptions of multi-purpose pins are given in the *PM6650 Power Management IC User Guide* (80-V5773-7) and at the end of this table.
22	LCD_DRV_N	AO	Programmable current sink intended to support LCD backlights or other functions.
23	KPD_DRV_N	AO	Programmable current sink intended to support keypad backlights or other functions.
25	VIB_DRV_N	AO	Vibration motor driver output—connect to the vibration motor negative terminal. The positive terminal of the motor connects to V_{DD}.
76	SPKR_IN_P	AI	Plus input to the speaker driver circuit. This pin is biased internally and requires AC-coupling (0.1 F capacitor is recommended or 4.7 F for USB audio). Intended for differential inputs (complemented by pin 78, SPKR_IN_M), but can be driven single-ended.
78	SPKR_IN_M	AI	Minus input to the speaker driver circuit. This pin is biased internally and requires AC-coupling (0.1 F capacitor is recommended or 4.7 F for USB audio). Intended for differential inputs (complemented by pin 76, SPKR_IN_P), but can be driven single-ended.
75	SPKR_OUT_P	AO	Plus speaker driver output; connect directly to the plus speaker terminal.
79	SPKR_OUT_M	AO	Minus speaker driver output; connect directly to the minus speaker terminal.
74	SPKR_BYP	AI	Connected to the speaker driver circuit's internal mid-rail bias voltage. Connect a 0.1 or 1.0 F capacitor immediately to ground (value depends upon the SBI-programmable speaker delay value).
77	VDD_SPKR	P	Power supply for the speaker. Bypass with a 0.1 F capacitor to ground.

Multi-purpose pins (MPPs)			
21	GP1_DRV_N (MPP7)	—	These multi-purpose pins are software configurable with the following options: ▪ Digital input ▪ Digital output ▪ Digital level translator—uses 1 MPP pair (note 4) ▪ Analog input ▪ Analog output ▪ Current sink Each pin has an intended function as defined elsewhere in this table, but can be reconfigured via SBI programming. See the *PM6650 Power Management IC User Guide* (80-V5773-7) for more details.
26	RUIM_IO (MPP12)	—	
30	RUIM_M_IO (MPP11)	—	
34	RUIM_M_CLK (MPP9)	—	
38	RUIM_CLK (MPP10)	—	
40	RUIM_M_RST (MPP5)	—	
43	RUIM_RST (MPP6)	—	
66	CBL1PWR_N (MPP4)	—	
68	CBL0PWR_N (MPP3)	—	
70	AMUX_IN1 (MPP1)	—	
72	AMUX_IN2 (MPP2)	—	
80	REF_OUT (MPP8)	—	

Notes:

1. All PM6650 VDD pins are driven by the handset supply voltage (V_{DD}) that includes a 22 F (or higher) ceramic bypass capacitor.
2. Pin type definitions:
   AI = analog input
   AO = analog output
   DI = digital input from MSM device
   DO = digital output to MSM device
   P = power or ground
   — = do not connect

Pins Description of K9F5608Q0C:

Pin NAME	Pin Function
I/O_0 ~ I/O_7 (K9F5608X0C) I/O_0 ~ I/O_{15} (K9F5616X0C)	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. I/O8 ~ I/O15 are used only in X16 organization device. Since command input and address input are x8 operation, I/O8 ~ I/O15 are not used to input command & address. I/O8 ~ I/O15 are used only for data input and output.
CLE	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	CHIP ENABLE The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation.
$\overline{RE}$	READ ENABLE The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	WRITE ENABLE The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	WRITE PROTECT The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low. When LOCKPRE is a logic high and $\overline{WP}$ is a logic low, the all blocks go to lock state.
R/$\overline{B}$	READY/BUSY OUTPUT The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{ccQ}	OUTPUT BUFFER POWER V_{ccQ} is the power supply for Output Buffer. V_{ccQ} is internally connected to Vcc, thus should be biased to Vcc.
Vcc	POWER Vcc is the power supply for device.
Vss	GROUND
N.C	NO CONNECTION Lead is not internally connected.
DNU	DO NOT USE Leave it disconnected
LOCKPRE	LOCK MECHANISM & POWER-ON AUTO-READ ENABLE To Enable and disable the Lock mechanism and Power On Auto Read. When LOCKPRE is a logic high, Block Lock mode and Power-On Auto-Read mode are enabled, and when LOCKPRE is a logic low, Block Lock mode and Power-On Auto-Read mode are disabled. Power-On Auto-Read mode is available only on 3.3V device(K9F56XXU0C). Not using LOCK MECHANISM & POWER-ON AUTO-READ, connect it Vss or leave it N.C

Pins Description of K4M28163PF:

Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A_0 ~ A_{12}	*Address*
BA_0 ~ BA_1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
L(U)DQM	*Data Input/Output Mask*
DQ_0 ~ 15	*Data Input/Output*
V_{DD}/V_{SS}	*Power Supply/Ground*
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*

Pins Description of uPD720101F1:

Power supply

Pin	Pin No.	Direction	Function
V_{DD}	13, 14, 23, 37, 38, 47, 52, 66, 73, 75, 76, 78, 80, 116, 131, 143	Power	+3.3 V power supply
V_{DD_PCI}	98, 103, 124	Power	+5 V for 5 V PCI or +3.3 V for 3.3 V PCI
AV_{DD}	68, 70	Power	+3.3 V power supply for analog circuit
V_{SS}	1, 12, 21, 25, 30, 36, 48, 49, 60, 71, 82, 110, 112, 115, 119, 130, 137, 140, 142	Power	Ground
AV_{SS}	24, 69, 111	Power	Ground for analog circuit
N.C.	17, 105	-	These N.C. pins must be pulled high on the board.

Analog signaling

Pin	Pin No.	Direction	Function
RREF	22	Analog	RREF must be connected a 1% precision reference resistor of 9.1 kΩ. The other side of resistor must be connected to local ground.

PCI interface

Pin	Pin No.	Direction	Function
AD (31 : 0)	44, 89, 127, 45, 128, 90, 46, 91, 2, 50, 51, 3, 94, 4, 95, 53, 8, 56, 100, 9, 101, 57, 10, 58, 11, 61, 102, 62, 15, 63, 16, 104	I/O	PCI "AD [31 : 0]" signal
CBE (3 : 0)0	93, 5, 99, 59	I/O	PCI "C/BE [3 : 0]" signal
PAR	132	I/O	PCI "PAR" signal
FRAME0	96	I/O	PCI "FRAME#" signal
IRDY0	129	I/O	PCI "IRDY#" signal
TRDY0	6	I/O	PCI "TRDY#" signal
STOP0	97	I/O	PCI "STOP#" signal
IDSEL	92	I	PCI "IDSEL" signal
DEVSEL0	54	I/O	PCI "DEVSEL#" signal
REQ0	126	O	PCI "REQ#" signal
GNT0	144	I	PCI "GNT#" signal
PERR0	55	I/O	PCI "PERR#" signal
SERR0	7	O	PCI "SERR#" signal
INTA0	125	O	PCI "INTA#" signal
INTB0	88	O	PCI "INTB#" signal
INTC0	43	O	PCI "INTC#" signal
PCLK	42	I	PCI "CLK" signal
VBBRST0	87	I	Hardware reset for Chip
CRUN0	64	I/O	PCI "CLKRUN#" signal
PME0	141	O	PCI "PME#" signal

System clock & reset for power management

Pin	Pin No.	Direction	Caution
XT1/SCLK	136	I	System clock input or Oscillator input Apply 48-MHz clock input or connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
XT2	19	O	If 48-MHz clock input is applied to SCLK, this signal must be opened. Otherwise, connect to 30-MHz X'tal. Clock frequency is selected by "Clock_sel reg." in EXT2.
VCCRST0	123	I	Reset for power management.

USB interface

Pin	Pin No.	Direction	Function
DP (5 : 1)	81, 118, 77, 29, 27	I/O	USB D+ high-speed signal Shared with DMx pins having the same numbers.
RSDP (5 : 1)	35, 33, 31, 114, 74	O	USB D+ full-speed signal Connected to DPx through 36 Ω 1% precision Rs resistor.
DM (5 : 1)	34, 32, 139, 113, 72	I/O	USB D– high-speed signal Shared with DPx pins having the same numbers.
RSDM (5 : 1)	79, 117, 138, 28, 26	O	USB D– full-speed signal Connected to DMx through 36 Ω 1% precision Rs resistor.
OCI (5 : 1)	86, 40, 85, 84, 83	I	Pin for inputting the overcurrent status of the USB Root Hub Port 1: No power supply problem 0: Overcurrent has occurred
PPON (5 : 1)	41, 122, 121, 39, 120	O	Power supply control output for USB Root Hub Port 0: Power supply OFF 1: Power supply ON

Legacy support interface

Pin	Pin No.	Direction	Function
LEGC	134	I	Legacy support switch 0: Legacy OFF 1: Legacy ON
SMI0	133	O	System management interrupt output 0: Interrupt occurs 1: Interrupt does not occur

Serial ROM interface

Pin	Pin No.	Direction	Caution
SRCLK	108	O	Serial ROM Clock Out
SRDTA	67	I/O	Serial ROM Data
SRMOD	20	I	Serial ROM Input Enable 0 (default): Serial ROM Inactive 1: Serial ROM Active

Test signals

Pin	Pin No.	Direction	Caution
SMC	106	I	Should be left open on circuit board.
AMC	18	I	Should be left open on circuit board.
NANDTEST	109	I	NAND-Tree test enable. 0 (default): NAND-Tree test disable 1: NAND-Tree test enable This can be left open on circuit board.
TEB	65	I	Should be left open on circuit board.
TEST	135	I	Should be left open on circuit board.
NTEST1	107	I	Should be left open on circuit board.

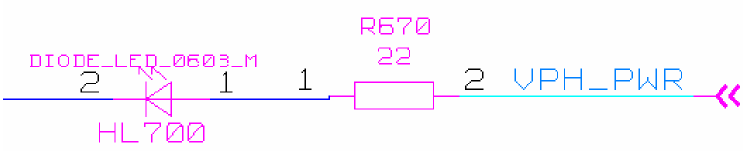
3.3.2 Logic circuit tuning up:

Cannot turn on : the program does not run and the LED is off

a. Turn on power supply, check if the voltage level(VPH_PWR) at pin2 of R 670 was correct. If VPH_PWR is abnormal, then check the circuits related with power supply, especially the chip-pm6650.
b. If the VPH_PWR is normal, then check if the outputs of the sleep clock a nd main clock were correct. If not, please check the circuits related with cl ock outputting.
c. If the clock output is normal, then download codes into the Nand flash. If the procedure of downloading is not successful, please check the circuits re lated with the nand flash and the sdram.
d. If the procedure of downloading is OK, check the circuits related with the main chip “msm6500” and the flash and the sdram. If all the connection is normal, you should replace the corresponding chip.

LED does not work , but the card is detected by computer:

1. Check if R670 is in open trace state. If so, re-solder it or replace it.
2. Check if LED HL700 is in open trace state. If so, re-solder it or replace it with new one.



Cannot insert into the card socket of computer

1. Check the 68-pins card connector is well placed and well soldered
2. Re-solder the card connector. And if it does not work, replace it with new one.

The card caused the computer restart or breakdown

1. Check the 68-pins card connector is well placed and well soldered, especial ly check if the pins are soldered short.

2. Re-solder the card connector. And if it does not work, replace it with new one.

4. Antenna Feature of ZTE MY39

Return Loss

Frequency	880MHz	1880MHz

Return Loss	-4.11	-12.18

Gain

Frequency(MHZ)	**ZTE MY39 Antenna**		
	E1	**E2**	**H**
824MHz	-2.56	-1.37	-1.33
880MHz	-0.74	0.14	0.13
1880MHz	1.86	-1.54	0.98
1990MHz	1.39	-1.38	0.39

XY plane is the **E1** plane, that means the Theta=90 degree.
XZ plane is the **E2** plane, that means the Phi = 0 degree.
YZ plane is the **H** plane, that means the Phi = 90 degree.

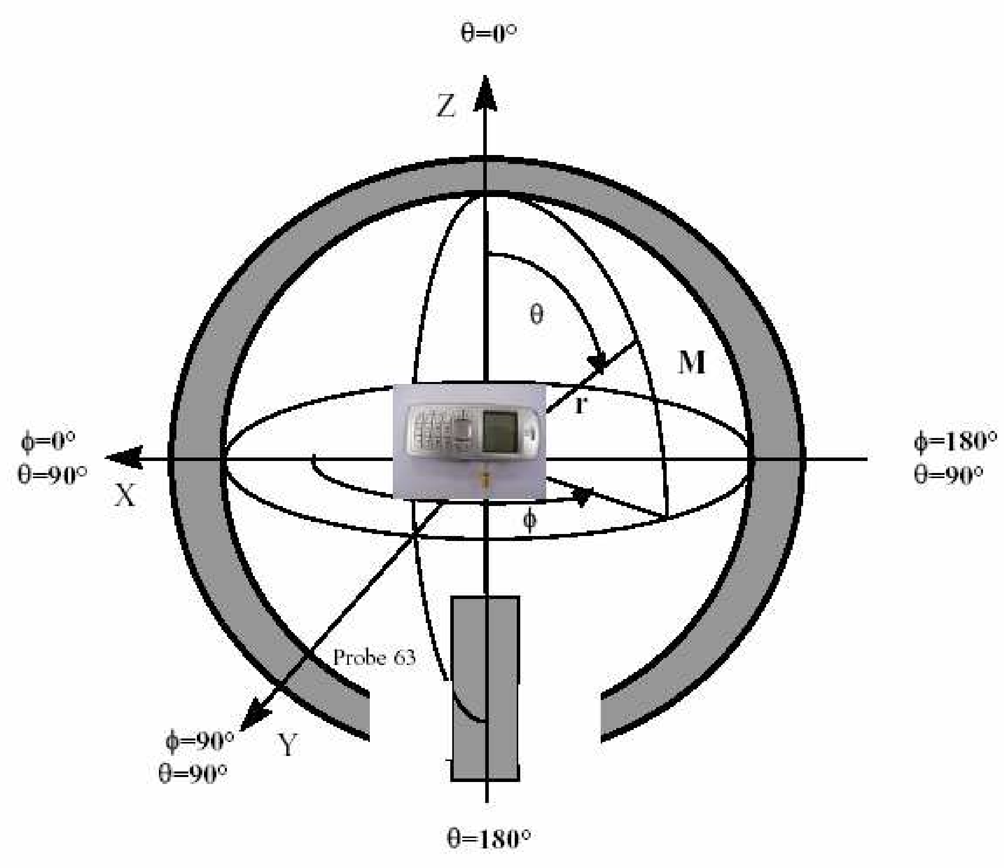


Figure 3: Coordinate System

Efficiency

Frequency (MHz)	**824**	**880**	**1880**	**1990**
Efficiency	34%	51%	61%	57%