a module solution provider

WG7550-00 WLAN/BT/FM/GPS Module

TI WL1283 IEEE 802.11a/b/g/n

BT4.0+FM+GPS solution

Datasheet

Revision 0.4

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1. OVERVIEW

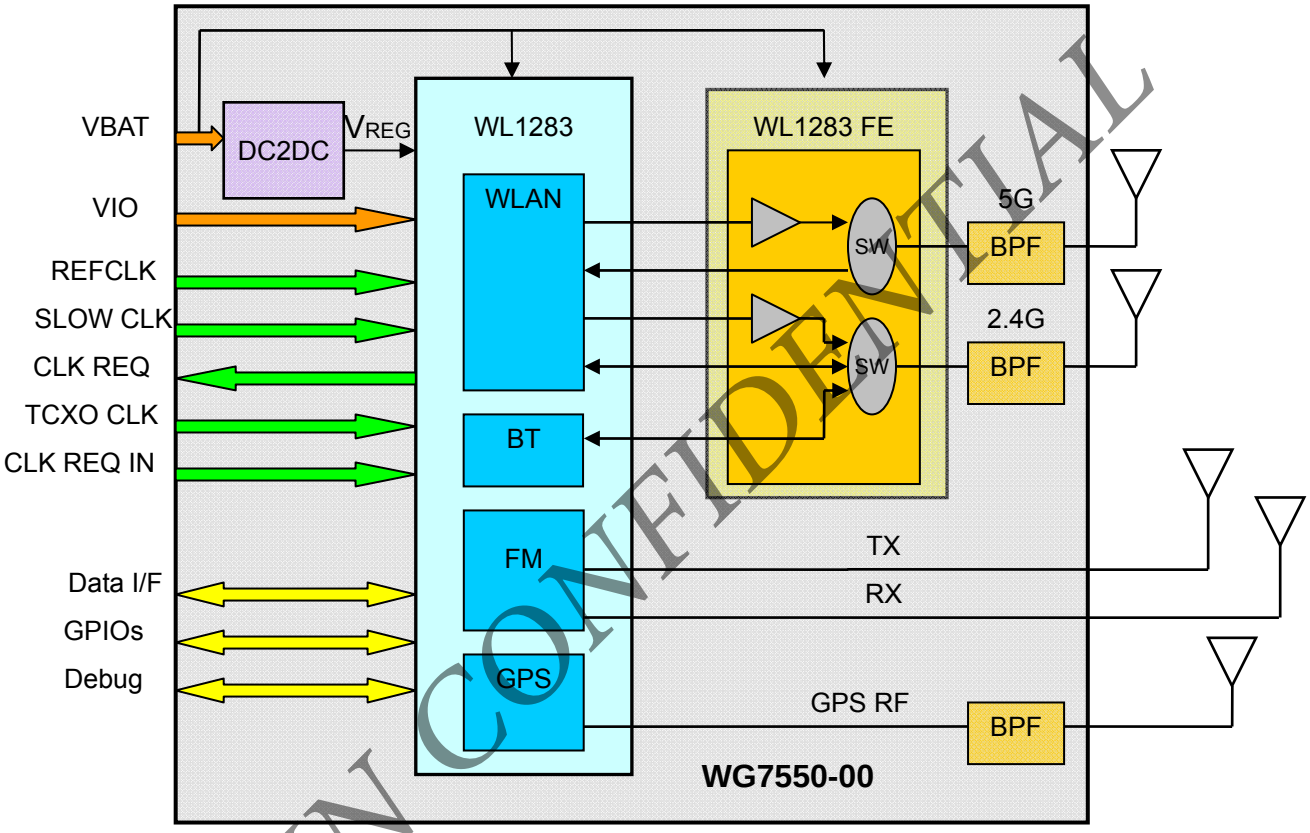
WG7550-00, a WiFi , Bluetooth , FM and GPS SiP (system in package) module, is the most demanded design for all handset and portable devices with TI WL1283 IEEE 802.11a/b/g/n and BT 4.0 EDR solutions to provide the best WiFi and BT coexistence interoperability and power saving technologies from TI.

1.1. General Features

- WLAN, Bluetooth, GPS, FM radio on a SiP module
- LGA106 pin package
- Dimension 12.3mm(L) x 10.2mm(W) x 1.4mm(H)
- Based on TI WL1283 65-nm CMOS technology packaged in WSP for module
- Support for BLE (BT Low Energy) dual mode
- Bluetooth IP includes Audio and Voice Processor (AVPR) targeted for off-loading the host CPU from coding voice/audio samples when running A2DP and WBS profiles
- Seamless integration with TI OMAP application processor and GSM-GPRS-UMTS chipset
- Internal support for WLAN and Bluetooth Co-existence (bandwidth sharing, antenna sharing)
- Direct connection to battery using external switching mode power supply supporting 5.5V to 2.3V operation
- Support for BLE (BT Low Energy) dual mode
- VIO in the 1.8V domain
- Fast Clock using external TCXO crystal
- RoHS Compliance

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram



2.2. Block Functional Feature

2.2.1. WLAN Features

- Support 802.11 2.4GHz b/g/n mode
- Support 802.11 5GHz a/n mode
- Optimized for ultra low current consumption in all operating modes including extremely low power modes
- IEEE Std 802.11d, e, h, I, k, r, s PICS compliant

- Supports Cisco Client eXtensions (CCX) standard
- Support Secure Digital Input/Output (SDIO)
- Medium-Access Controller (MAC)
  - Embedded ARM Central Processing Unit (CPU)
  - 292kByte (Used for Program code, data and packet data) Embedded Random-Access Memory (RAM)
  - Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys
  - Supports Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
  - Designed to Work with IEEE Std 802.1x for Virtual Private Network (VPN) Solutions
- Baseband Processor
  - All IEEE Std 802.11a/b/g and 802.11n Data Rates up to 72.2Mbps
- 2.4/5 GHz Radio
  - Digital Radio Processor (DRP) implementation
  - Internal LNA
  - Supports: IEEE Std 802.11b, 802.11g, 802.11a and 802.11n

2.2.2. Bluetooth Features

- Support Bluetooth 4.0 (BLE) + EDR specification compliant.
- BT Enhanced Data Rate (2 and 3 Mbps)
- Support for Bluetooth 2005 core release
- Enhanced host Interfaces (UART)
- Fully compliant with BT4.0 BLE dual mode standard:
  - TI BLE solution optimized for the proximity / sports use-case
  - Supports large number of multiple connections (up to 10)
  - Multiple sniff instances are tightly coupled to achieve minimum power consumption
  - Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance
- On-chip Embedded radio

  - Integrated 2.4 GHz RF transceiver
  - Support for Class-1.5 (higher output power) applications
- Embedded ARM Microprocessor System
- High rate H4 UART HCI
- Temperature detection and compensation mechanism ensure minimal variation in the RF performance over the entire temperature range
- TI-proprietary low-power scan achieves paging and inquiry scans with fast RSSI algorithm, at 1/3 normal power.
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - Assisted A2DP (A3DP) support –SBC Encoding implemented internally
  - Assisted WB-Speech (AWBS) support – modified SBC codec implemented internally
  - FM over Bluetooth A3DP – FM Radio to Bluetooth Stereo Headset

2.2.3. BLE Features

Fully compliant with BT4.0 Low Energy (BLE) dual mode standard:

- TI BLE solution optimized for the proximity/sports use-case
- Supports large number of multiple connections (up to 10)
- Multiple sniff instance are tightly coupled to achieve minimum power consumption
- Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN

Notes: Advanced audio and voice processing (AVPR) capabilities, and ANT are not available when BLE is enabled.

2.2.4. ANT Features

Fully compliant with all ANT Protocols:

- ANT solution optimized for the fitness, health and consumers use-case
- Supports large number of multiple connections (up to 8)
- Simple to complex network topologies
- Support high-resolution proximity pairing
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN
- ANT provides immediate access to the millions of ANT+ sensors already in the market and an ongoing option for cost and power optimized sensors

The ANT protocol has been designed to very power-efficient, yet is flexible enough to support various network topologies (point-to-point, star, 1-to-N, N-to-1) and data transfer modes (broadcast, broadcast with acknowledge, mass data transfer). Each logical ANT channel can be independently configured for 1-way or 2-way operation.

Notes: Advanced audio and voice processing (AVPR) capabilities, and BLE are not available when ANT is enabled.

2.2.5. FM Radio (RX/TX) Features

- Support both Europe/US (87.5 to 108MHz) and Japan FM bands (76 to 90 MHz) with 50kHz step size
- Half-duplex receive-transmit capability with RDS/RDBS support
- Support for both analog and digital audio interfaces (I2S/PCM)
- I2S interface can be in master/slave mode supporting a wide range of frame-sync and bit clock frequencies and supports I2S and PCM protocols
- Operation through Bluetooth host interface (UART) or Slimbus, for control, RDS and audio transfer
- On-Chip FM Receive
- On-Chip 0dBm output FM Transmitter
- Up to 48k Samples/sec audio sampling for stereo headsets
- Full digital implementation
- Digital MPX signal, thus eliminating need for noise blanking

circuits
- Soft Mute
- Stereo/Mono blend based on signal condition for RX
- Selectable 50/75-us de-emphasis filter
- I^2S format for stereo/mono digital audio data
- Analog stereo audio inputs/outputs
- Software selectable level for soft mute and stereo/mono blend level for RX
- Fast independent up/down tuning function
- Supports a dedicated enable pin for the FM IP

2.2.6. GPS Features

- Significantly improved TTFF (Time to First Fix) at low signal power levels through enhanced receiver core architecture
  - Assisted TTFF <= 1.5 second with all satellites at -130dBm
  - Hot start (from IDLE) TTFF <= 10 seconds with all satellites at -155dBm
  - Asynchronous networks TTFF <= 42 seconds with all satellites at -155dBm with zero ppm clock offset
- Improved TTFF in autonomous cold start conditions,
  - Average autonomous cold start TTFF of < 34 seconds in open-sky conditions
  - Autonomous cold start TTFF of < 42 seconds with all satellites at -142dBm
- Sensitivity improvements
  - -159dBm hot start acquisition with all SVs at equal power
  - -162dBm tracking sensitivity
- Support for SBAS
- Carrier phase measurements for improved performance in multi-path scenarios and handling of user dynamics
- Dedicated Delay Locked Loops for SV tracking to improve multi-path detection and mitigation.
- Hybrid solution with sensors to augment GPS to enhance user experience in urban canyons and during dead-reckoning

- Sleep based Advanced Power Management (APM) tracking for significantly lower power consumption

3. MODULE SPECIFICATION

3.1. Absolute Maximum Ratings

Over operating free-air temperature range

Characteristics		Value	Unit
Supply Voltage Range	VBAT	-0.5 to 5.5	V
	VIO	-0.5 to 2.1	V
Input Voltage to Analog Pins		-0.5 to 2.1	V
Input Voltage to all Other Pins		-0.5 to VIO + 0.5V	V
Operating Ambient Temperature Range		-30 to 75	˚C
Storage Temperature Range		-40 to 125	˚C

3.2. Recommended Operating Conditions

The WG7550 requires three two supplies: VBAT and VIO.

Power Supply	Voltage		
	Min.	Typ.	Max.
VBAT	2.3V	3.6V	4.8V
VIO	1.62V	1.8V	1.92V

3.3. WLAN RF Characteristic

3.3.1. 2.4-GHz Receiver

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Operation frequency range			2412		2484	MHz
Sensitivity	1 Mbps DSSS		-92.5	-96.0	–	dBm
	2 Mbps DSSS		-90.0	-93.5	–	
	5.5 Mbps CCK		-88.0	-91.0	–	
	11 Mbps CCK		-85.0	-87.0	–	
	6 Mbps OFDM		-88.0	-90.0	–	
	9 Mbps OFDM		-87.5	-89.5	–	
	12 Mbps OFDM		-86.0	-88.0	–	
	18 Mbps OFDM		-84.5	-86.5	–	
	24 Mbps OFDM		-82.0	-83.5	–	
	36 Mbps OFDM		-79.0	-80.0	–	
	48 Mbps OFDM		-74.5	-76.0	–	
	54 Mbps OFDM		-70.0	-73.0	–	
	MCS0(1)		-87.5(5)	-90.0	–	
	MCS1(1)		-85.0(5)	-86.0	–	
	MCS2(1)		-83.0(5)	-84.0	–	
	MCS3(1)		-81.0(5)	-82.5	–	
	MCS4(1)		-77.0(5)	-79.0	–	
	MCS5(1)		-73.0(5)	-75.0	–	
	MCS6(1)		-71.0(5)	-73.0	–	
	MCS7(1)		-68.0(5)	-71.0	–	
Max Input Level(2)	OFDM(11g or 11n)		-10		-6	dBm
	CCK		-4		0	
	2DSSS		-4		0	
Adjacent Channel Rejection	54OFDM	ADJCI	30	32		dB
	11CCK		48	54		
LO Leakage					-70	dBm

(1) Greenfield mode : degrade 1 dB for mixed mode

(2) At < 10% packet error rate (PER) limit.

3.3.2. 5-GHz Receiver

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Operation frequency range		FREF	4900		5825	MHz
Sensitivity	54 Mbps OFDM(3)		-68.0(1)	-71.0	–	
	48 Mbps OFDM		-70.5	-73.5	–	
	36 Mbps OFDM		-74.5	-77.5	–	
	24 Mbps OFDM		-77.5(1)	-80.5	–	
	18 Mbps OFDM		-80.5	-83.5	–	
	12 Mbps OFDM(2)		-82.5(1)	-85.5	–	
	9 Mbps OFDM		-84.0	-87.0	–	
	6 Mbps OFDM		-85.0	-88.0	–	
	MCS0(1)		-84.5	-86.5	–	
	MCS1(1)		-85.0(5)	-86.0	–	
	MCS2(1)		-83.0(5)	-84.0	–	
	MCS3(1)		-81.0(5)	-82.5	–	
	MCS4(1)		-77.0(5)	-79.0	–	
	MCS5(1)		-73.0(5)	-75.0	–	
	MCS6(1)		-69.0(5)	-72.0	–	
	MCS7(1)		-65.0(1)	-68.0	–	
Max Input Level	OFDM				-17	dBm
Adjacent Channel Rejection	54M OFDM	ADJCI	17			dB
LO Leakage					-63	dBm

3.3.3. 2.4-GHz Transmitter

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Maximum RMS output power	1 Mbps,2 Mbps		17.0	18.0	–	dBm
	5.5 Mbps,11 Mbps		17.0	18.0	–	

	6 Mbps at EVM: -7 dB, 9 Mbps at EVM: -10 dB		16.5	17.5	–	
	12 Mbps at EVM: -12 dB, 18 Mbps at EVM: -15 dB		16.0	17.0	–	
	24 Mbps at EVM: -18 dB, 36 Mbps at EVM: -21 dB		14.0	15.5	–	
	48 Mbps at EVM: -25 dB, 54 Mbps at EVM: -25 dB		12.5	14.0	–	
	MCS0 at EVM: -7 dB		15.5	16.5		
	MCS1 at EVM: -12 dB		14.0	16.0		
	MCS2 at EVM: -15 dB		14.0	16.0		
	MCS3 at EVM: -18 dB		13.0	15.0		
	MCS4 at EVM: -21 dB		13.0	15.0		
	MCS5 at EVM: -24 dB		12.5	14.0		
	MCS6 at EVM: -25 dB		12.5	14.0		
	MCS7 at EVM: -28 dB		11.5	13.0	–	
In band power variation below 10 dBm / above 10 dBm			±3/ ±1			dB

3.3.4. 5-GHz Transmitter

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Maximum RMS output power	6 Mbps at EVM: -7 dB, 9 Mbps at EVM: -10 dB		16.5	18.0	–	dBm
	12 Mbps at EVM: -12 dB, 18 Mbps at EVM: -15 dB		14.5	16.0	–	
	24 Mbps at EVM: -18 dB, 36 Mbps at EVM: -21 dB		13.5	15.0	–	
	48 Mbps at EVM: -25 dB, 54 Mbps at EVM: -25 dB		12.0	13.5	–	
	MCS0 at EVM: -7 dB		15.0	16.5		
	MCS1 at EVM: -12 dB		13.5	15.0		
	MCS2 at EVM: -15 dB		13.5	15.0		

	MCS3 at EVM: -18 dB		12.5	14.0		
	MCS4 at EVM: -21 dB		12.5	14.0		
	MCS5 at EVM: -24 dB		12.0	13.5		
	MCS6 at EVM: -25 dB		12.0	13.5		
	MCS7 at EVM: -28 dB		11.0	12.5	–	
EVM	24 Mbps and 36 Mbps at +13.5dBm		-23			dB
	48 Mbps and 54 Mbps at +12.0dBm		-25			
	MCS7 at + 11.0dBm		-28			
In band power variation			±3/ ±1			dB

3.4. Bluetooth RF

3.4.1. BT Transmitter, GFSK, Class 2 & Class 1.5

Characteristics		Min	Typ	Max	Unit
RF output power	VDD_LDO_IN_CLASS1P5 = VBAT	7	9	---	dBm
	VDD_LDO_IN_CLASS1P5 = 1.8V	5	7	---	
Power variation over BT band		-1		1	dB
Gain control range			30		dB
Power control step		2	5	8	dB

3.4.2. BT Receiver Characteristics, In-Band Signals

Characteristics		Min	Typ	Max	Unit
Sensitivity	GFSK, BER = 0.1%	-88	-90		dBm
	Pi/4-DQPSK, BER = 0.01%	-86	-90		
	8DPSK, BER = 0.01%	-80	-84		
Max. useable input power	GFSK, BER = 0.1%	-5			dBm
	Pi/4-DQPSK, BER = 0.1%	-10			
	8DPSK, BER = 0.1%	-10			

3.5. BLE RF

BT Transmitter						
Characteristics		**Min**	**Typ**	**Max**	**BLE SPEC**	**Unit**
RF output power	CLASS1P5 = VBAT	7	9	---	<= -10	dBm
Power variation over BLE band		-1		1		dB

BT Receiver Characteristics, In-Band Signals						
Characteristics		**Min**	**Typ**	**Max**	**BLE SPEC**	**Unit**
Sensitivity	PER=30.8%	-89	-92	---	<= -70	dBm
Max. useable input power	GFSK, PER = 30.8%	-5	---	---	>= -10	dBm

3.6. FM Radio Electrical Characteristics

Characteristics	**Condition**		**Min**	**Typ**	**Max**	**Unit**
Audio output impedance	FM function enabled and during auto-search				50	Ω
	FM function disabled and when muted		50			KΩ
Audio input impedance			30			KΩ
Selectable RF Rx input impedance	With external matching circuitry – Default = 50 Ω			50	500	Ω
RF input return loss	With external matching circuitry		-10			dB
Receiver current consumption	FM Rx at sensitivity level, BT in deep sleep			12	15	mA
Transmitter current consumption	FM TX on, BT in deep sleep	Digital audio		13	16	mA
		Analog audio				
FM off current				1	2	uA

3.7. GPS RF Subsystem Specifications

GPS performance specifications :

Baseline Tests		
Category	**Baseline Test Conditions** [1] [2]	**Typical Performance** [3] [4]
Autonomous Cold Start[5]	• At –130 dBm • At –142 dBm • At sensitivity –146 dBm	• Average TTFF < 35 s, CEP95 < 6 m • Average TTFF < 42s , CEP95 < 11 m • Average TTFF < 225 s, CEP95 < 25 m
With network assistance Asynchronous network (Coarse time assisted) baseline performance[6]	• At –130 dBm • At –145 dBm • At –150 dBm • At –155 dBm • At sensitivity –157 dBm	• Average TTFF < 2 s, CEP95 < 12 m • Average TTFF < 2.5 s, CEP95 < 25 m • Average TTFF < 5.5 s, CEP95 < 45 m • Average TTFF < 20 s, CEP95 < 200 m • Average TTFF < 60 s, CEP95 < 350 m
With network assistance Synchronous network (Fine time assisted) baseline performance	• At –130 dBm • At –145 dBm • At –150 dBm • At –155 dBm • At sensitivity –158 dBm	• Average TTFF < 1 s, CEP95 < 15 m • Average TTFF < 2 s, CEP95 < 25 m • Average TTFF < 5 s, CEP95 < 40 m • Average TTFF < 18 s, CEP95 < 125 m • Average TTFF < 80 s, CEP95 < 300 m
Tracking[7]	• At –130 dBm • At –148 dBm • At –150 dBm • At –155 dBm • At –158 dBm • At –161.5 dBm (with data wipeoff)	• CEP95 < 3 m • CEP95 < 6 m • CEP95 < 7 m • CEP95 < 20 m • CEP95 < 75 m • CEP95 < 225 m
Hot start[8]	• At –130 dBm • At –145 dBm • At –150 dBm • At –155 dBm • At sensitivity –158 dBm	• Average TTFF < 1 s, CEP95 < 15 m • Average TTFF < 2 s, CEP95 < 20 m • Average TTFF < 5 s, CEP95 < 40 m • Average TTFF < 17 s, CEP95 < 125 m • Average TTFF < 80 s, CEP95 < 300 m
Standard Compliance Tests	**Standard Compliance Test Conditions**[9]	
3GPP Performance Standard	3GPP Standard 34.171 • Accuracy • Sensitivity • Multi-path • Dynamic range • Moving scenario tests	Fully 3GPP compliant; all tests met with margin • CEP95 < 10 m and TTFF95 < 5 s • CEP95 < 50 m and TTFF95 < 15 s • CEP95 < 30 m and TTFF95 < 11 s • CEP95 < 35 m and TTFF95 < 13 s • 100% yield with CEP95 < 10 m
3GPP Performance Standard Sensitivity Test Margin[10]	• UE Based • UE Assisted (with TOW Resolve[11] at server) • UE Assisted (without TOW Resolve at server)	• 7 dB margin (–149 dBm/–154 dBm) • 7 dB margin (–149 dBm/–154 dBm) • 6.5 dB margin (–148.5 dBm/–153.5 dBm)

(1) *Sensitivity* is defined as the lowest power level at which the yield is > 50%. *Yield* refers to the percentage of successful fixes (within timeout) relative to the number of fix attempts.
(2) Baseline performance test specification uses 9SV scenario with all equal power having PDOP < 3.
(3) Typical test conditions are for a nominal device at room temperature.
(4) All specifications are based on a system configuration that includes a front-end external RF filter with an insertion loss of 1.2 dB and with GPS configured in internal LNA. *CEP95* refers to a 95% circular error probable.
(5) Cold start specification is based on a timeout of 300 s and frequency uncertainty of 2 ppm.
(6) All baseline specifications are based on the following receiver configuration parameters: Position uncertainty: 10 km, frequency uncertainty: ±0.5 ppm, frequency offset: 0 ppm, time uncertainty: 33 µs (synchronous network) and 2 sec (asynchronous network), timeout: 128 sec.
(7) Tracking performance is measured with a reporting interval of once every second.
(8) Hot Start specification is based on a timeout of 128 sec with 5 sec in sleep state between fixes.
(9) 3GPP standard compliance tests are conducted on ULTS-ADS with the following receiver configuration: Frequency uncertainty: ±0.2 ppm, frequency offset: 0 ppm.
(10) Margins are referenced to 3GPP 25.171 (–142 dBm/–147 dBm). Additional +1-dB margin available when referenced to 3GPP 34.171 (–141 dBm/–146 dBm) on ULTS setup.
(11) TOW Resolve is also known as Solve-for-time technique.

3.8. External Slow Clock Input (SLEEP_CLK)

The external slow clock input SLEEP_CLK must be present at all times. The slow clock is used to maintain timers that synchronize the device to the access point (AP) beacons.

Table 1. External Slow Clock Input Requirements

Characteristics (1)	Condition	Min.	Typ.	Max.	Unit
Frequency			32.768		KHz
Frequency Accuracy (Initial + temp + aging)	WLAN, BT, GPS, FM_RX			+/-150	ppm
	FM_TX (2)			+/- 40	
Input Transmit Time	10% ~ 90%			100	ns
Frequency Duty Cycle		30	50	70	%
Fail Safe Maximum Value				2.0	V
Input Voltage Limits (Square Wave)	V_{IH}	0.65xVIO		VIO	Vpeak
	V_{IL}	0		0.35xVIO	
Input Impedance		1			MΩ
Input Capacitance				5	pF
Rise and fall time				100	ns
Phase noise	1kHz, 10kHz			-125	dBc/Hz
Jitter (3)	Integrated over 300Hz ~ 15000Hz			1Hz/0.5nS	

(1) Slow clock is a fail safe input

(2) If the available slow clock source does not meet the +/-40ppm requirement, there are two options;

- Use the fast clock for the FM_TX functionality. This is configured using a vendor-specific command to switch to Fref operation after enabling the FM core with the slow clock source.
- Enable clock error calibration in the FM core to compensate for the clock source error. The calibration can be done using a known vendor-input clock error or intrinsically to the core (self-calibration).

(3) Not required if fast clock is used for FM TX and RX

3.9. External TCXO Clock Input

Table 2. External TCXO Clock Input Requirements

Characteristics	Condition		Min.	Typ.	Max.	Unit
Frequency				26		MHz
Frequency Accuracy(1)	Short term				+/- 2	ppm
	Long term				+/- 6	
Input voltage limits (TCXO_M)	DC coupled	V_{IL}	0		0.2	V
		V_{IH}	1.45		1.95	V
Input voltage limits (TCXO_P)	AC coupled		0.8		1.2	V_{p-p}
Input impedance	Input resistance		20	30	40	KΩ
	Input capacitance		1.5	2.0	3.0	pF
Frequency Duty Cycle			35	50	65	%
Harmonica					-10	dBc
Thermal freq. stability versus temp. change of TCXO_CLK source(2)				5	50	ppb/°C
Frequency drift rate (from time min. dc voltage is provided from VDD_TCXO)	From 0.1 s to 0.5 s				0.1	ppm/s
	From 0.5 s to 1.5 s				0.015	ppm/s
	From 1.5 s onwards				0.005	ppm/s
Power-up time(3)				2	10	ms
Phase noise	At 10-Hz offset				-78.4	dBc/Hz
	At 100-Hz offset				-103.4	dBc/Hz
	At 1-KHz offset				-129.4	dBc/Hz
	At 10-KHz offset				-142.4	dBc/Hz
	At 100-KHz offset				-147.4	dBc/Hz
Integrated phase noise (10Hz to 1MHz)					8.5	psRMS

(1) Short term : voltage and temperature effects
Long term : including aging

(2) Thermal stability has an impact on maximum GPS integration time without loss in sensitivity. The best performance will occur at the level of 5 ppb/°C, but the performance may be limited due to available TCXO. The calculated target

thermal stability values are based on a maximum temperature gradient of 0.3°C/s. Thermal stability may be relaxed at extreme temperatures (high and low) upto 100 ppb/°C based on available TCXO quality. Not required if fast clock is used for FM TX and RX.

(3) Power-up time is calculated from the time VDD_TCXO reaches 95% of steady state value till the time the TCXO_CLK amplitude is within voltage limit specified above and TCXO_CLK frequency is within 0.1 ppm of final steady state frequency.

4. POWER CONSUMPTION

4.1. Device Shutdown Current

The SDIO/CLK_REQ lines should be driven by the host to prevent leakage in sleep/shutdown modes.

Mode Description	Power Supply	Typ.	Max.	Unit
Shutdown mode (BT, WLAN, GPS and FM sections in shutdown mode) Values are over process and at room temperature	1.8V (VIO)	1	2	uA
	Total V_{BAT} at 3.6V	25	35	

4.2. WLAN Power Consumption

4.2.1. Active Mode

- During Listen Mode operation, the radio is in a low power mode optimized to receive only 11b beacons. The DC2DC, FEM and WL1283 devices are active but consume less current.
- In TX and RX modes, all devices are active and consume maximum currents.

Mode Description		Power Supply	11Mbps IEEE802.11b		54/65Mbps IEEE802.11g/n		54/65Mbps IEEE802.11a/n		Unit
			Typ (1)	Max (2)	Typ (1)	Max (2)	Typ (1)	Max (2)	
TX Data	11b/g: Packet size =2048 bytes 11n: Packet size =1024 bytes 11b delay=0.004ms 11g/n delay=0.002ms 11M done at 20.5dBm, 54/65M 11g done at 15.5dBm, 11a done at 15dBm	1.8V (VIO)	0.09	0.1	0.09	0.1	0.17	0.2	mA
		Total V_{BAT} =3.6V	265	280	190	205	235	280	

Receive Data	1.8V (VIO)	0.09	0.1	0.09	0.1	0.09	0.1	mA
	Total V_{BAT} =3.6V	70	80	80	90	80	90	
Listen For 11b in Listen mode, 1Mbps. For 11g in Listen mode, 6Mbps.	1.8V (VIO)	0.09	0.1	n/a	n/a	n/a	n/a	mA
	Total V_{BAT} =3.6V	52	60	n/a	n/a	n/a	n/a	

(1) Nominal process at 25℃

(2) Over process and temperature

4.2.2. Inactive and Dynamic Modes

Mode Description	Power Supply	Typ(1)	Max(2)	Unit
Sleep mode (BT, GPS and FM in reset) (3)	1.8V (VIO)	20	25	uA
	Total V_{BAT} at 3.6V	150	230	

(1) Nominal process at 25℃

(2) Room temp over process

(3) Values indicate current between beacons

Mode Description (1)	Power Supply	Max	Unit
Dynamic mode Beacon (DTIM =1 : TBTT = 100ms) Beacon duration~1.6ms : Rate= 1Mbps Beacon in Listen mode	Total V_{BAT} at 3.6V to TPS62611	0.75	mA

(1) This mode reflects results with software drivers and not the RTTT tool.

4.3. BT Power Consumption

BT supply current was measured using the HDK and HCI Tester tool at F_{ref} 26MHz.

4.3.1. Static State

Characteristics		Typ	Max	Unit
Supply current in deep sleep mode	VIO	23	30	uA
	V_{BAT}	80	200	

4.3.2. Dynamic State

Transmit power at 4dBm, nominal, room temperature. V_{BAT}=3.6V, F_{ref} at 26MHz. Currents are without the current taken for the TCXO.

Use Case	Mode Description	VBAT	Unit
Idle current (ARM off) (1)	Master/Slave	1.85	mA
Deep sleep	Master/Slave	80	uA
SCO link HV3	Master/Slave	9.3	mA
eSCO link EV3 64Kbps, no retransmission	Master/Slave	9.6	
eSCO link 2-EV3 64Kbps, no retransmission	Master/Slave	6.5	
GFSK full throughput: Tx=DH1, RX=DH5	Master/Slave	28.2	
EDR full throughput: Tx=2-DH1, RX=2-DH5	Master/Slave	28.9	
EDR full throughput: Tx=3-DH1, RX=3-DH5	Master/Slave	28.9	
Sniff, 1 attempt, 1.28sec	Master/Slave	130/140	uA
Page or Inquiry Scan 1.28s, 11.25ms	Master/Slave	280	
Page scan 1.28s, 11.25msec and Inquiry Scan 2.56s, 11.25ms	Master/Slave	370	
Low power scan, 1.28 interval	Master/Slave	165	

4.4. FM Power Consumption

Typical values are at room temp at nominal process; maximum receive and transmit values are over process and temperature.

CHARACTERISTICS	CONDITION			VBAT (1) MIN	VBAT (1) TYP (2)	VBAT (1) MAX	UNIT
Receiver supply current	FM Rx on at sensitivity conditions, Bluetooth in deep sleep, WLAN off, GPS off	Digital audio output			8.2		mA
		Analog audio output			9		
Transmitter supply current	FM Tx on at unregulated 123 $dB\mu V_{RMS}$ output, Bluetooth in deep sleep, WLAN off, GPS off , PA operating from dc-2-dc	Digital audio input	Japan band		24	24	mA
			Europe band		21	24	
		Analog audio input	Japan band		26	27	
			Europe band		23	27	
	FM TX on at regulated 120 $dB\mu_{VRMS}$ output. bluetooth in deep sleep, WLAN off, GPS off, PA operating from dc-2-dc	Digital audio input	Japan band		16	16	
			Europe band		14	16	
		Analog audio input	Japan band		19	19	
			Europe band		17	19	
	FM Tx on at regulated 123 $dB\mu V_{RMS}$ output, Bluetooth in deep sleep, WLAN off, GPS off, Pa operating from VBAT	Digital audio input	Japan band		23	23	
			Europe band		20	23	
		Analog audio input	Japan band		26	26	
			Europe band		23	26	

(1) Measured values reflect nominal dc-2-dc efficiency in the listed operating conditions, and may improve as the load on the dc-2-dc increases when the other core functions are active (for example, WLAN, GPS, or Bluetooth).

(2) Typical value is the measured average in the band; Japan: 76 to 90 MHz, Europe: 87.5 to 108 MHz.

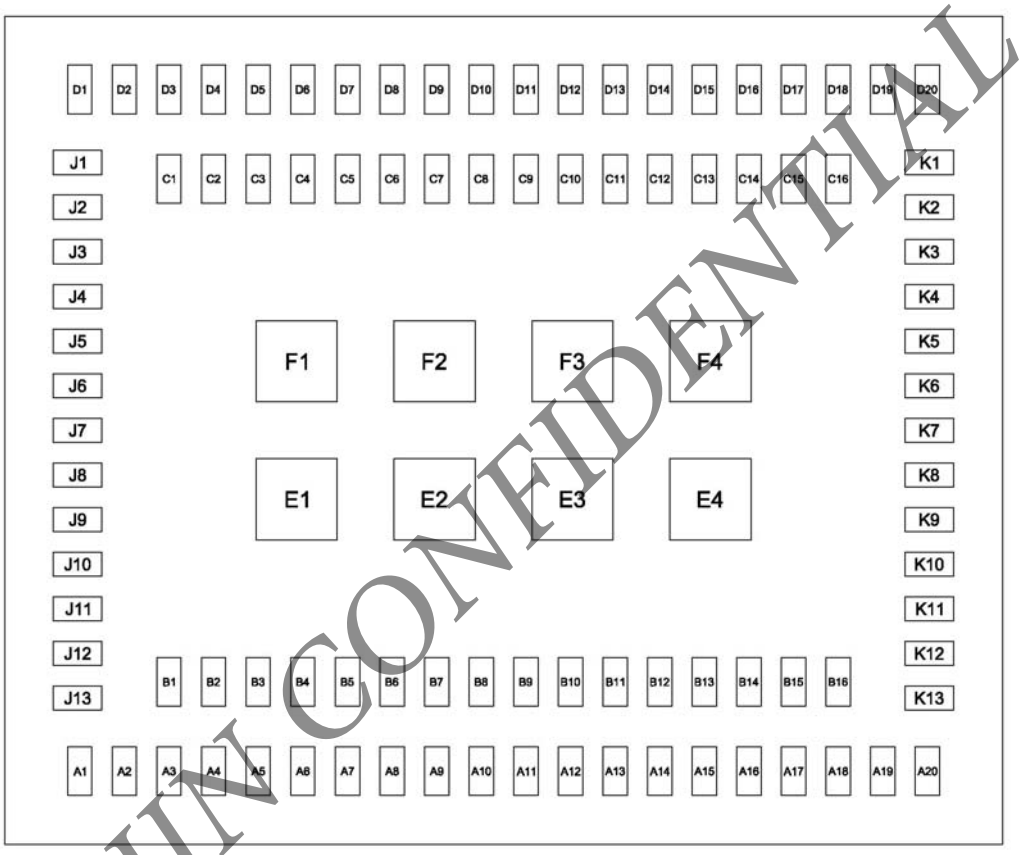
4.5. GPS Power Consumption

CHARACTERISTICS	COMMENTS	VBAT		VIO		UNIT
		TYP (1)	MAX (2)	TYP (1)	MAX (2)	
Sleep	Lowest possible power consumption state in which all GPS related information (decoded satellite data, previous position and time) are retained along with loaded firmware to provide a *hot fix* on wakeup	0.12	1.1	0.5	0.55	mA
Idle	Transition mode between active, sleep modes with RF, and other signal processing blocks turned off.	1.9	5	0.5	0.55	mA
Acquisition	Power state when receiver is active and looking to acquire the satellite signal.	36.5	42	0.5	0.55	mA
Tracking	Power state where receiver is active and HW is optimally used for satellite tracking and making location fixes.	22	27	0.5	0.55	mA
Low-Power Tracking	Adaptive RF mode for reduced current based on GPS signal conditions.	20	24	0.5	0.585	mA

(1) Room temperature, nominal
(2) Over temperature, over process

5. MODULE PIN OUT

5.1. Module Pin Assignment



Module Top View

5.2. Pin Description

No.	Index	Name	Type	Description
1	A1	GND	-	Ground
2	A2	VBAT_FE	I	Power supply input
3	A3	GND	-	Ground
4	A4	WA_RF_ANT	I/O	RF transmitter output and RF receiver input
5	A5	GND	-	Ground
6	A6	GND	-	Ground
7	A7	TXCO_P	-	TCXO ac-coupled clk input. If dc-coupled clk used, tie to GND.
8	A8	TCXO_M	-	TCXO dc-coupled clk input. If ac-coupled clk used, tie to VIO.
9	A9	GND	-	Ground
10	A10	FREE_CLK/XTALP	-	ac-coupled Fref input. If dc-coupled clk used, tie to GND. Also, XO output. GND if not used.
11	A11	XTALMSQ_CLK	-	dc-coupled Fref input. If ac-coupled clk used, tie to VIO. Also, XO input. GND if not used.
12	A12	GND	-	Ground
13	A13	VDD_1V8_IN	P	1.8V rail input
14	A14	VDD_1V8_OUT	P	1.8V rail output
15	A15	PCM_AUD_FSYNC	I/O	Bluetooth PCM frame sync in or out.
16	A16	PCM_AUD_OUT	I/O	Bluetooth PCM Data out
17	A17	PCM_AUD_IN	I/O	Bluetooth PCM Data in
18	A18	PCM_AUD_CLK	I/O	Bluetooth PCM clock in or out
19	A19	TCXO_LDO_OUT	P	TCXO LDO out to external TCXO power rail. Voltage determines according to TCXO_VOL_SEL. Requires external 0.1uF cap to GND. N/C if not used.
20	A20	GND	-	Ground
21	K13	VBAT	P	Power supply input
22	K12	BT_WAKE	I/O	Internal use as BT_WU. N/C if not used.
23	K11	HOST_WAKEUP	I/O	Internal use as HOST_WU. N/C if not used.
24	K10	SDIO_CLK	I	WLAN SDIO clock

25	K9	SDIO_D2	I/O	WLAN SDIO data bit 2
26	K8	SDIO_D0	I/O	WLAN SDIO data bit 0
27	K7	SDIO_D3	I/O	WLAN SDIO data bit 3
28	K6	SDIO_D1	I/O	WLAN SDIO data bit 1
29	K5	SDIO_CMD	I/O	WLAN SDIO command in
30	K4	LDO_IN_FM_TX	P	FM VBAT PA input supply
31	K3	GND	-	Ground
32	K2	FM_OUT_P	O	RF transmitter output
33	K1	FM_OUT_M	O	RF transmitter output
34	D20	GND	-	Ground
35	D19	FM_RX	I	FM receiver input
36	D18	GND	-	Ground
37	D17	FM_AUD_IN_L	I	FM audio in left channel
38	D16	FM_AUD_IN_R	I	FM audio in right channel
39	D15	FM_AUD_OUT_R	O	FM audio out right channel
40	D14	FM_AUD_OUT_L	O	FM audio out left channel
41	D13	GND	-	Ground
42	D12	SLEEPCLK	-	Slow clock in
43	D11	GND	-	Ground
44	D10	GPS_ANT	I	GPS RF receiver input
45	D9	GND	-	Ground
46	D8	NC	--	N/C
47	D7	GND	-	Ground
48	D6	UART_RX	I	BT UART I/F
49	D5	UART_RTS	O	BT UART I/F
50	D4	VIO	P	VIO power supply
51	D3	BT_EN	I	BT reset
52	D2	WL_EN	I	WLAN reset
53	D1	GND	-	Ground
54	J1	WB_RF_ANT	I/O	RF transmitter output and receiver input
55	J2	GND	-	Ground
56	J3	UART_CTS	I	BT UART I/F
57	J4	UART_TX	O	BT UART I/F
58	J5	TCXO_VOL_SEL	I	TCXO LDO output voltage select: 'GND'→1.83V

				‘floating’→2.5V ‘VIO’→ 2.87V
59	J6	TCXO_CLK_REQ	O	TCXO clock request to host: HiZ: not active (configurable to be 0) ‘1’: request external TCXO clock Requires ext pull resister <100KΩ depending on system req.
60	J7	VDD_LDO_IN_CLASS1P5	P	Bluetooth input VBAT supply for Bluetooth PA
61	J8	GPS_PA_EN	I	GPS PA enable. Indication of some kind of coexistence issue transmitting.
62	J9	WL_EXT_LNA_EN	O	WLAN external LNA control. Active High.
63	J10	FREE_CLK_REQ	O	Fref clock request to host: HiZ: not active (configurable to be 0) ‘1’: request external Fref clock Requires ext pull resister <100KΩ depending on system req.
64	J11	WLAN_IRQ	O	WLAN interrupt out. Active low.
65	J12	GPS_UART_RX	I	Internal use. Leave N/C
66	J13	GPS_UART_TX	O	Internal use. Leave N/C
67	B1	DC2DC_MODE	I/O	SMPS mode select: internal SMPS mode(in): '0' PFM Mode. '1' PWM Mode. N/C if not used.
68	B2	GND	-	Ground
69	B3	GPS_SENSE_I2C_SCL	I	Not used. Leave N/C
70	B4	GPS_SENSE_I2C_SDA	I/O	Not used. Leave N/C
71	B5	GND	-	Ground
72	B6	GND	-	Ground
73	B7	WLAN_UART_DBG	O	This pin should be connected to test point on board for software debug.
74	B8	DC2DC_REQ_IN	I	Host request to activate internal SMPS ‘0’: not active ‘1’: activate internal SMPS. While ‘1’ internal SMPS continue working.

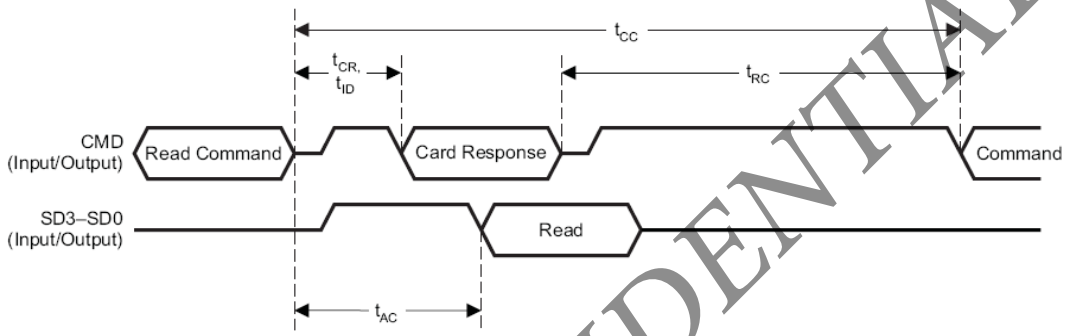
				GND if not used.
75	B9	TCXO_CLK_OUT	O	TCXO clock out(to be fed to external device)
76	B10	EXT_DC_REQ	O	Vbat request to host '0': not active '1' activate Vbat rail. N/C if not used.
77	B11	FM_I2S_DI	I/O	FM I2S data in
78	B12	FM_I2S_FSYNC	I/O	FM I2S frame sync in or out
79	B13	FM_I2S_DO	I/O	FM I2S data out
80	B14	FM_I2S_CLK	I/O	FM I2S clock
81	B15	SB_DATA	I/O	SLIMbus data. GND if not used.
82	B16	SB_CLK	I/O	SLIMbus clock. GND if not used.
83	C16	GND	-	Ground
84	C15	GND	-	Ground
85	C14	BT_SCL	I/O	Not used. Leave N/C
86	C13	BT_SDA	I/O	Not used. Leave N/C
87	C12	WL_RS232_RX	I	This pin should be connected to test point on board for hardware debug.
88	C11	WL_RS232_TX	O	This pin should be connected to test point on board for hardware debug.
89	C10	GND	-	Ground
90	C9	GPS_EXT_LNA_EN	O	GPS external LNA enable output.
91	C8	GPS_PPS_OUT	I/O	Not used. Leave N/C
92	C7	GPS_IRQ	O	Not used. Leave N/C
93	C6	GPS_TIMESTAMP	I	Not used. Leave N/C
94	C5	GND	-	Ground
95	C4	BT_UART_DBG	I/O	This pin should be connected to test point on board for software debug.
96	C3	WiMAX_SYNC	I/O	Not used. Leave N/C
97	C2	TCXO_CLK_REQ_IN	I	Host request to activate TCXO LDO: '0': not active '1': activate TCXO LDO and enable output TCXO clock via TCXO_CLK_OUT. GND if not used.
98	C1	GND	-	Ground

99	E1	GND	-	Ground
100	E2	GND	-	Ground
101	E3	GND	-	Ground
102	E4	GND	-	Ground
103	F4	GND	-	Ground
104	F3	GND	-	Ground
105	F2	GND	-	Ground
106	F1	GND	-	Ground

6. INTERFACE CHARACTERISTICS

6.1. WLAN SDIO Characteristic

6.1.1. SDIO Read Timing

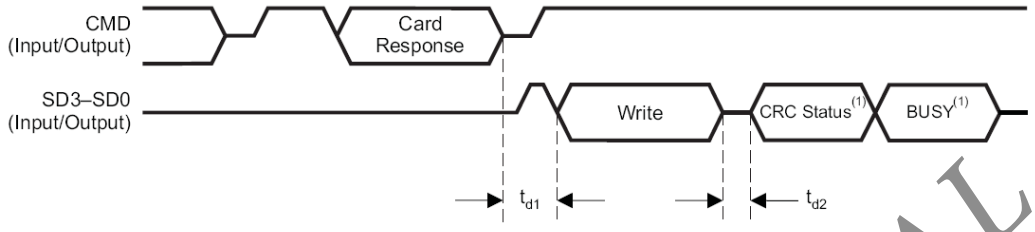


SDIO Single Block Read

Table 3. SDIO Read Switching characteristics

Parameter		Min.	Max.	Unit
t_{CR}	Delay time, assign relative address/data transfer mode, CMD command invalid to CMD response valid	2	64	Clock Cycles
t_{ID}	Delay time, identification, CMD command invalid to CMD response valid	5	5	
t_{CC}	Delay time, CMD command invalid to CMD response valid	58	---	Clock Cycles
t_{RC}	Delay time, CMD response invalid to CMD command valid	8	---	Clock Cycles
t_{AC}	Access time, CMD command invalid to SD3-SD3 read data valid	2	---	Clock Cycles

6.1.2. SDIO Interface Write Timing



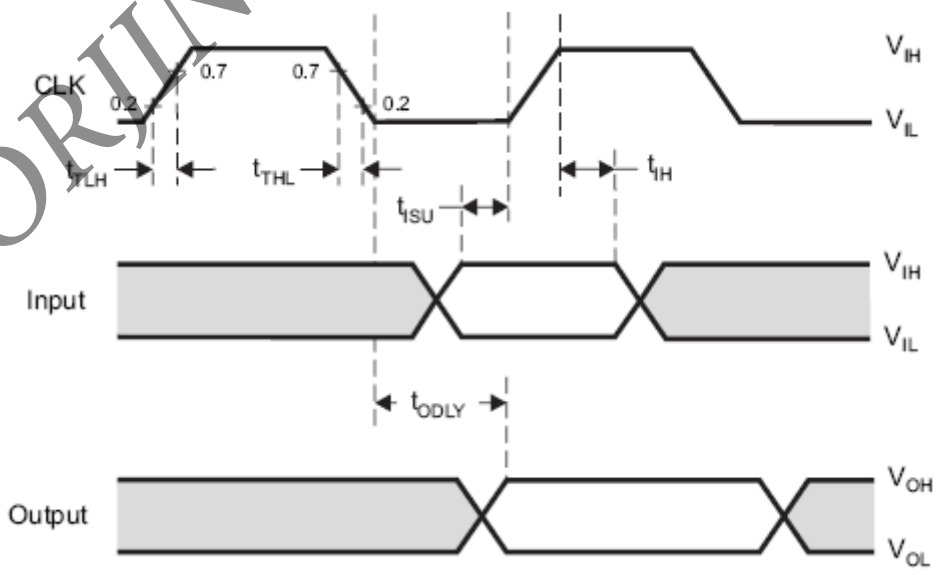
(1) CRC status and busy waveforms are only for data line 0. Data lines 1-3 are N/A. The busy waveform is optional and may not be present.

SDIO Single Block Write

Table 4. SDIO Write Switching characteristics

Parameter		Min.	Max.	Unit
t_{d1}	Delay time, CMD card response invalid to SD3-SD0 write data valid	2	---	Clock Cycles
t_{d2}	Delay time, SD3-SD0 write data invalid end to CRC status valid	2	2	Clock Cycles

6.1.3. SDIO Clock Timing – Default Rate



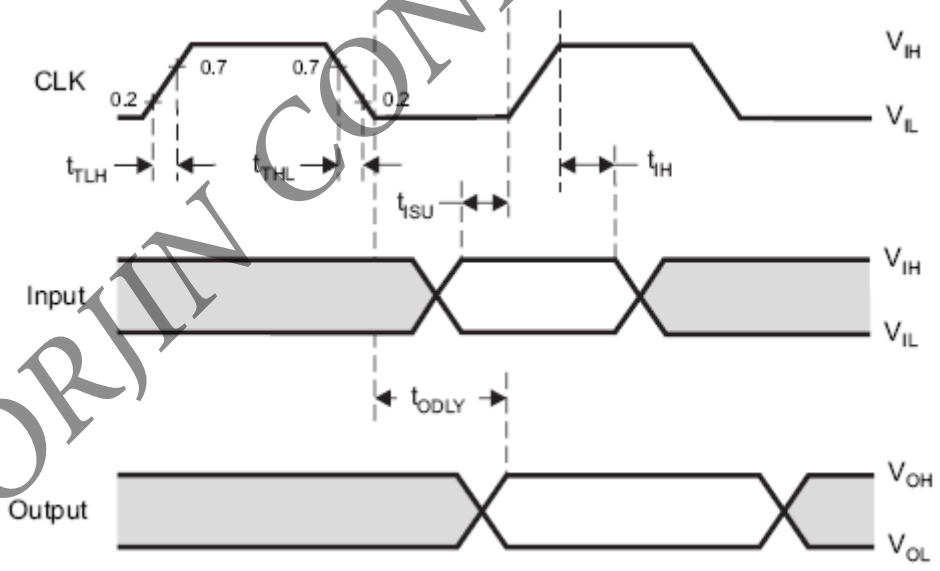
SDIO Clock Timing

Table 5. SDIO Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	26	MHZ
DC	Low/high duty cycle	40	60	%
t_{TLH}	Rise time, CLK	1	3	ns
t_{THL}	Fall time, CLK	1	3	ns
t_{ISU}	Setup time, input valid before CLK↑	2		ns
t_{1H}	Hold time, input valid after CLK↑	2		ns
t_{ODLY}	Delay time, CLK↓ to output valid	2.5	14.8	ns
CI	Capacitive load on outputs		15	pF

Note: Option to change data out clock edge from falling edge (default) to rising edge, by setting configuration bit.

6.1.4. SDIO Clock Timing – High Rate

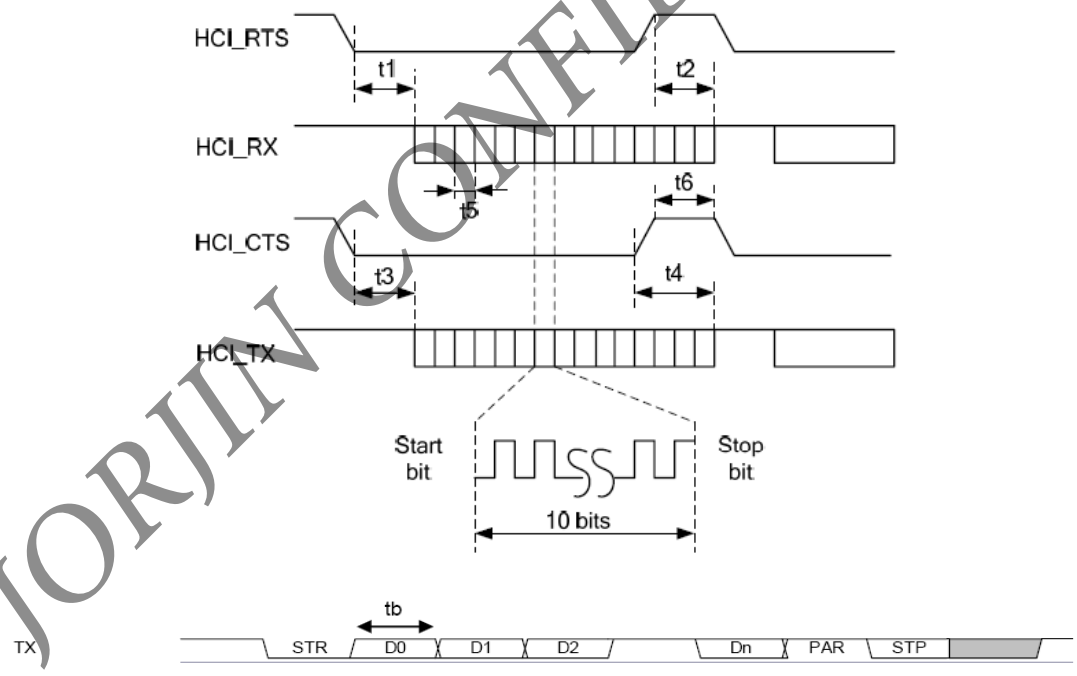


SDIO Clock Timing

Table 6. SDIO Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	52	MHZ
DC	Low/high duty cycle	40	60	%
t_{TLH}	Rise time, CLK	1	3	ns
t_{THL}	Fall time, CLK	1	3	ns
t_{ISU}	Setup time, input valid before CLK↑	2		ns
t_{1H}	Hold time, input valid after CLK↑	2		ns
t_{ODLY}	Delay time, CLK↓ to output valid	2.5	14.8	ns
Cl	Capacitive load on outputs		15	pF

6.2. Bluetooth HCI Interface



* STR: Start bit; D0…Dn: Data bits (LSB first); PAR: Parity bit (if parity is used); STP: Stop bit

Table 7. BT HCI Timing characteristics

Characteristics	Condition	Symbol	Min	Typ.	Max	Unit
Baud rate			37.5	115.2	4000	kbps
Baud rate accuracy	Receive/Transmit				-2.5to+1.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS high pulse width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes

6.3. Bluetooth PCM Interface

Bluetooth can be setting as master or slave mode. For more stable voice performance, slave mode is recommended.

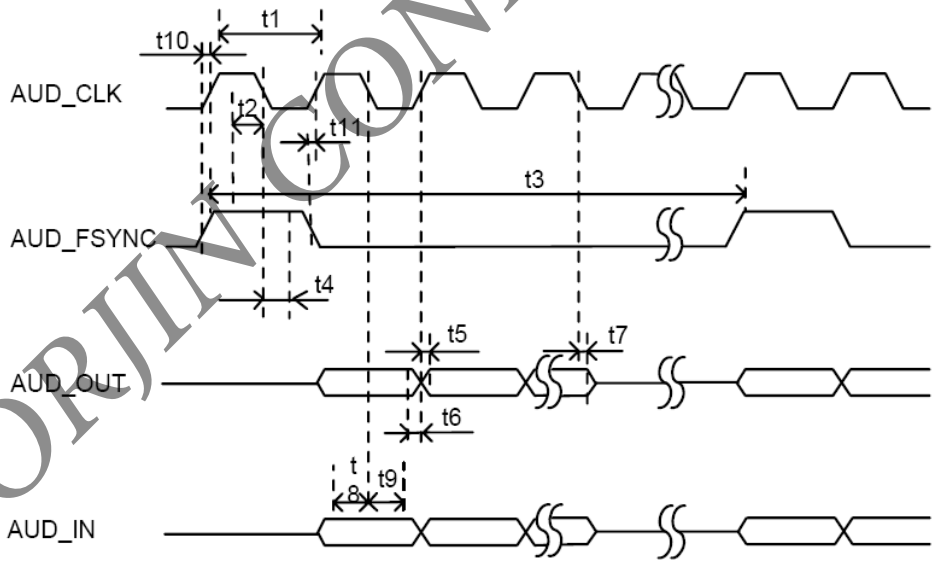
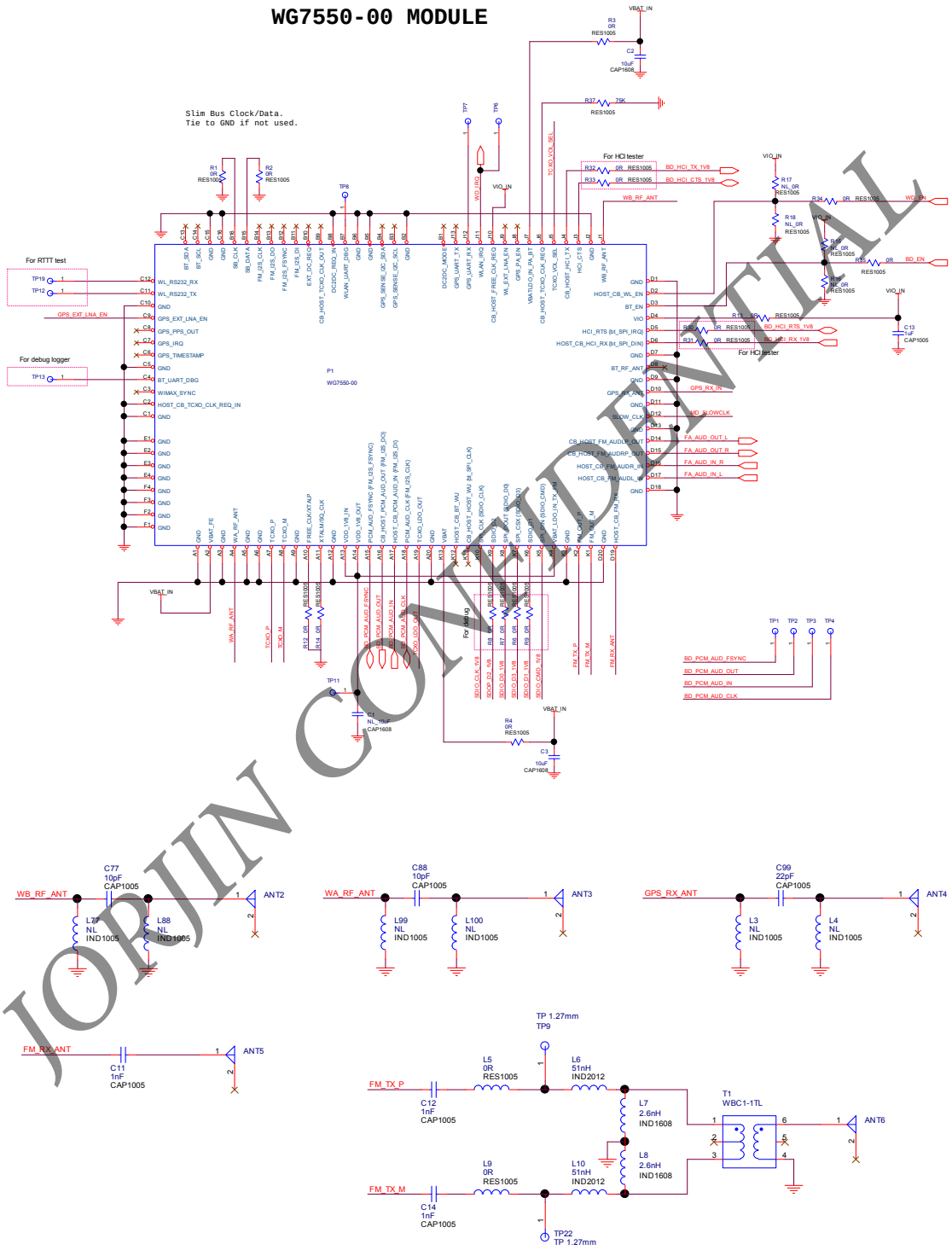


Table 8. BT PCM Slave mode Timing characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit
Master clock frequency	1/t1	64		16000	KHz
Clock duty cycle		40	50	60	%
Synchronization clock frequency	1/t3	1/(8xt1)		1/(65535xt1)	KHz
Synchronization signal width		t1		165545xt1	
Setup time for AUD_FSYNC high to AUD_CLK low	t2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t7			20	ns

7. REFERENCE SCHEMATIC

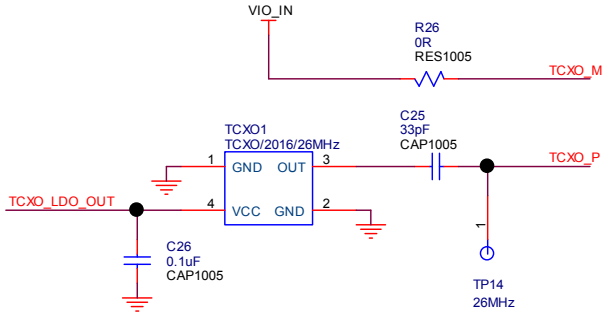


TCXO 26MHz

TCXO Mode	TCXO_M(A8)	TCXO_P(A7)
AC coupled	VIO	0.8v-1.195v
DC coupled	0v-1.92v	GND

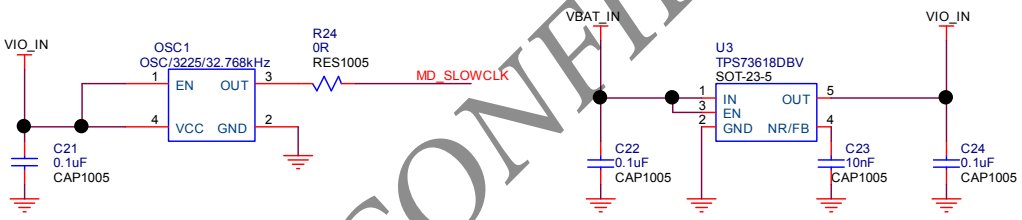
TCXO LDO Output Voltage Select

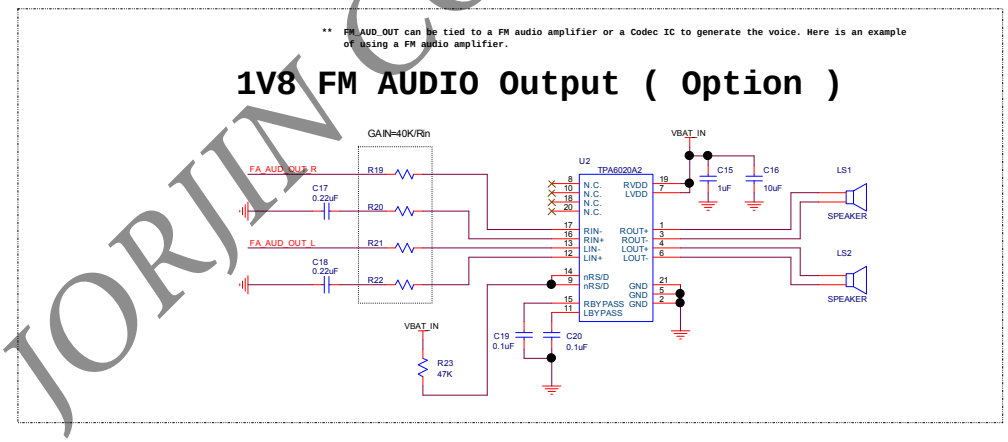
TCXO_LDO_OUT(A19)	TCXO_VOL_SEL(J5)
1.83V	GND (default)
2.5V	Floating
2.87V	VIO



32.768K XOSC

1.8V LDO





Scheme Brief

WiFi Interface: SDIO

BT Interface: UART, PCM

FM Interface: UART (with BT together), Audio IN/OUT

GPS Interface: UART

Fast Clock: TCXO 26MHz from outside

Slow Clock: 32.768KHz from outside

** Boot Conditions

VBAT_IN: 2.7~4.8V => 3.3V TYP

VIO_IN: 1.62~1.92V => 1.8V TYP

Slow Clock: 32.768KHz for module boot and deep sleep

***** WiFi SDIO/SPI Matching Curcuit

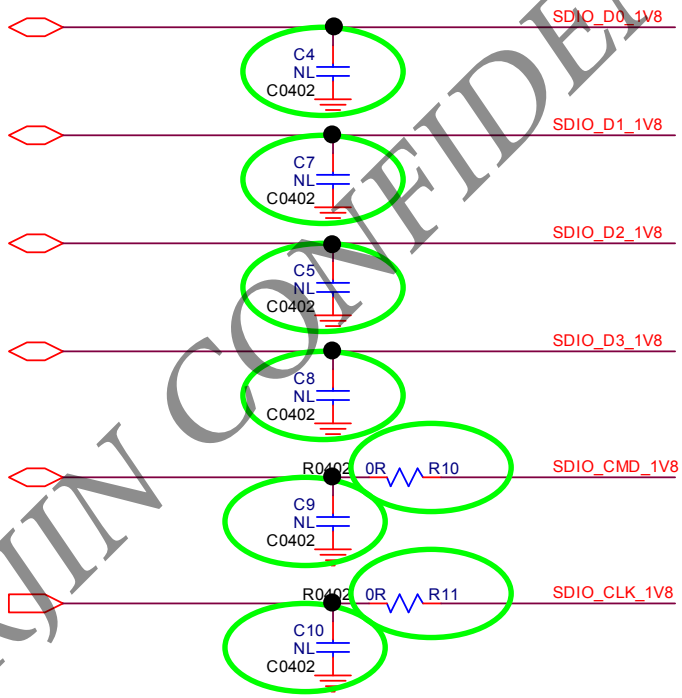
In green circle is a necessary part

** It's recommended to reserve SDID matching circuits and keep them close to WG7550-00 module for signal optimization

** The six traces from U1 (module) to Host must be treated like a bus. The bus length shall be as short as possible and every trace length must be the same as the others. Enough space above 2 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Besides, please remember to keep them away from the other digital or analog signal traces. To add ground shielding to around the buses will be helpful.

** SDIO lines should be held high by the host

** All test point must reserved for test

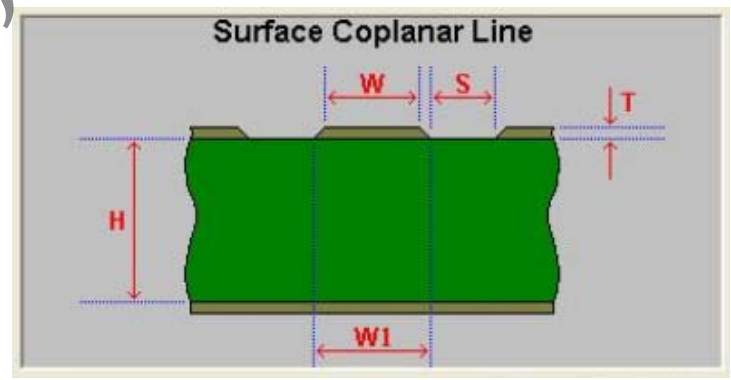


8. LAYOUT RECOMMENDATION

8.1. Recommended Trace Layout

- **Digital Signals Layout**
  - SDIO signals traces (CLK, CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible **(less than 12cm)**.
    Besides, every trace length must be the same as the others.
    Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Remember to keep them away from the other digital or analog signal traces. Adding ground shielding around these bus is recommended.
  - SDIO Clock, PCM clock, Audio Clock… these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.

- **RF Trace & Antenna**
  - 50 ohm trace impedance match on the trace to the antenna.
  - Recommended 50ohm trace design for PCB layout



Height Between L1 and L2 **(H):**	10.0 mil
Trace **(W):**	15.35 mil
(W1):	15.35 mil
Thickness **(T):**	2.1 mil
Separation **(S):**	10.0 mil
Dielectric **(Er):**	4.3

- Move all the high-speed traces and components far away from the antenna.
- Check ANT vendor for the layout guideline and clearance.
- Matching circuit layout should be as following figure.

- **Power Trace**
  - Power trace for VBAT should be 40mil wide. 1.8V trace should be 18mil wide.

- **Ground**
  - Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation as following figure.
  - Have a complete Ground pour in layer 2 for thermal dissipation.
  - Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
  - Move GND vias close to the pad.

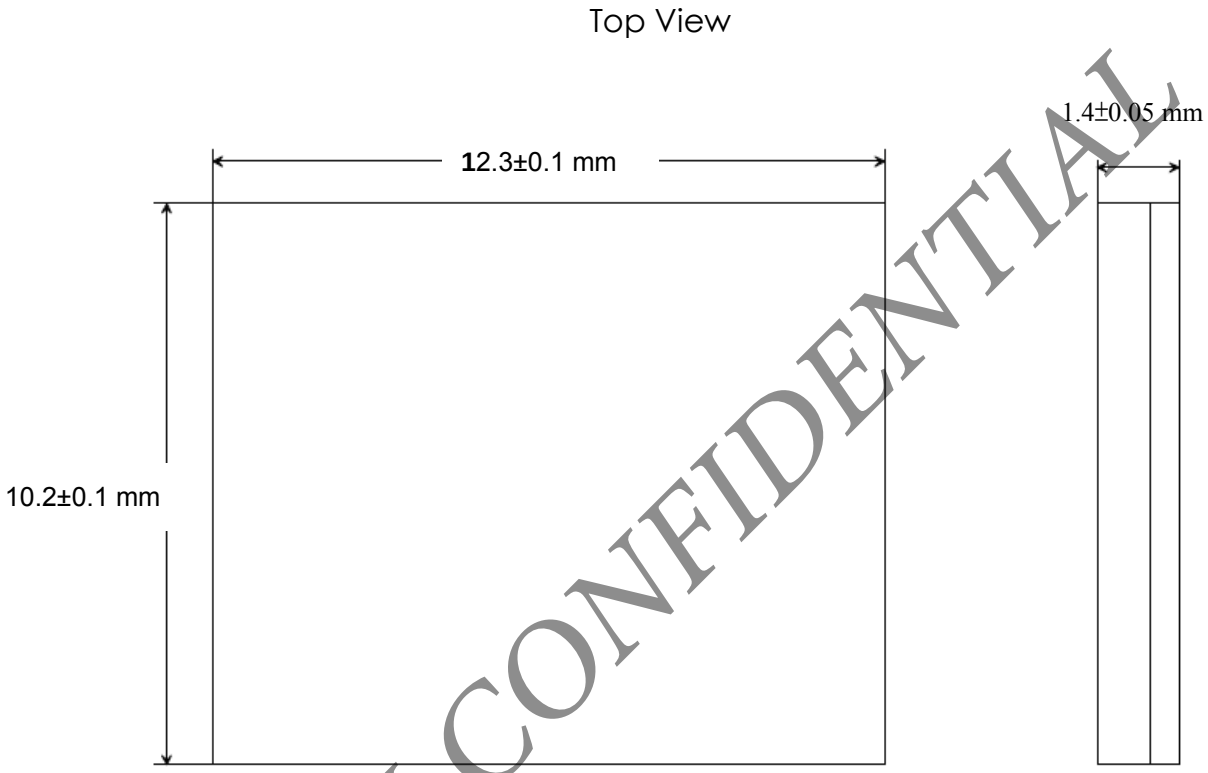
- **Slow Clock**
  - FM RF module uses the 32-kHz clock, it is extremely important that the slow-clock trace not be routed next to any digital signals.

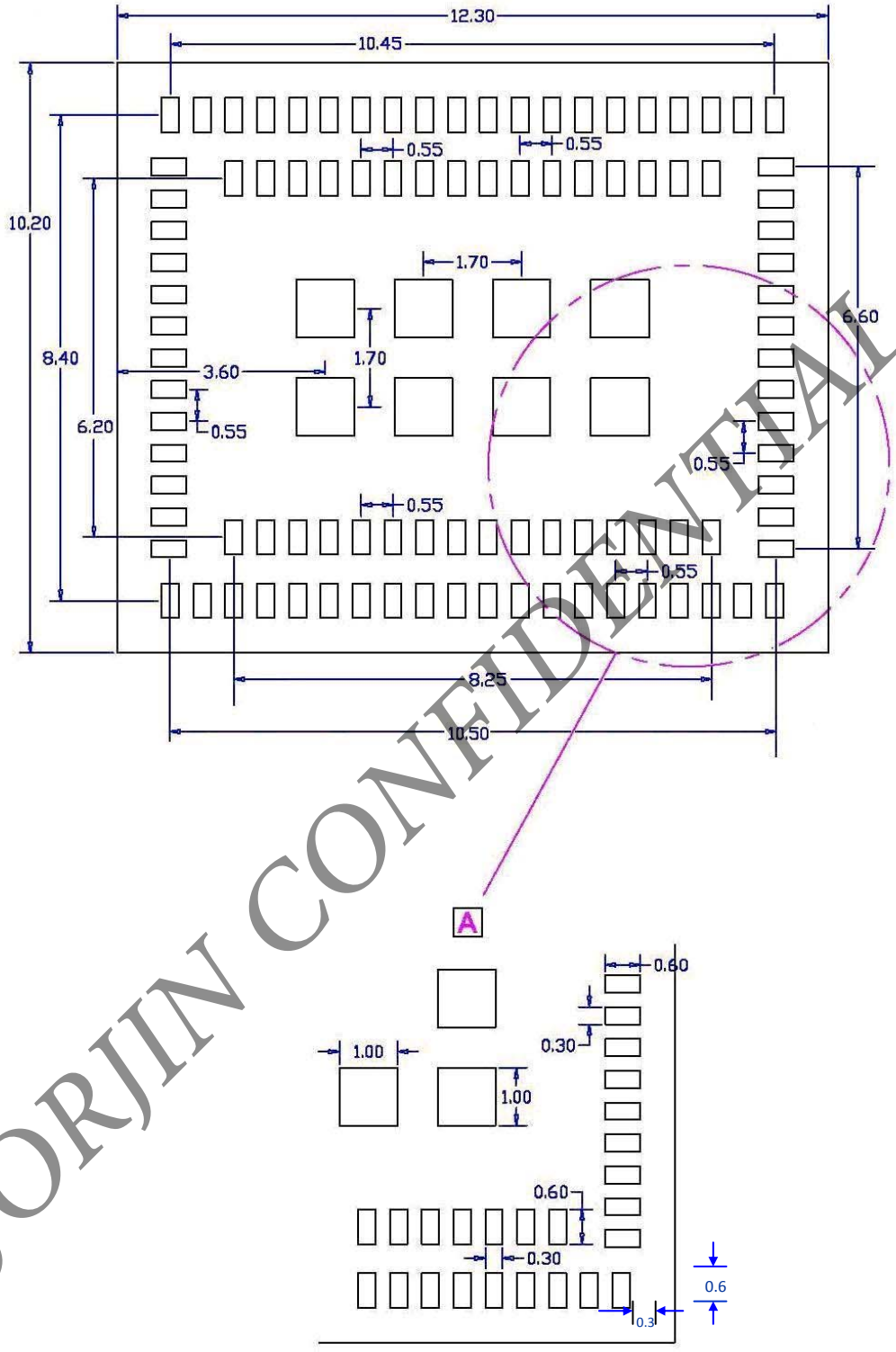
- The slow clock trace should not be routed above or below digital signals on other layers.

- **TCXO**
  - Do not route any high-speed digital lines, such as UART, SPI, or other clocks, under the TCXO.
  - Connect the TCXO to ground using multiple vias to ensure a strong grounding.
  - Place the decoupling capacitor as close as possible to the TCXO and route the supply line to the TCXO using wide traces (200 um or more) to keep the inductance to a minimum.
  - The output line from the TCXO is very small compared to the TCXO output wavelength (or rise time); therefore, there is no requirement to use controlled impedance for this line.
  - Although a continuous ground plane can be used under the TCXO, having a small slot between the TCXO ground and the WG7550 ground connections can help reduce the heat transfer between the devices. A rapid heating of the TCXO because of a WG7550 device power-up can cause frequency perturbations at the TCXO output and as well as impact GPS acquisition performance.

9. PACKAGE INFORMATION

9.1. Module Mechanical Outline





Top View (Perspective view)

Unit: mm

Dimension tolerance: +/- 0.05

9.2. Ordering Information

Part number:	WG7550-00

9.3. Package Marking

Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2008=08

WW = Week (01~53)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = 1 for Taiwan

10. SMT AND BAKING RECOMMENDATION

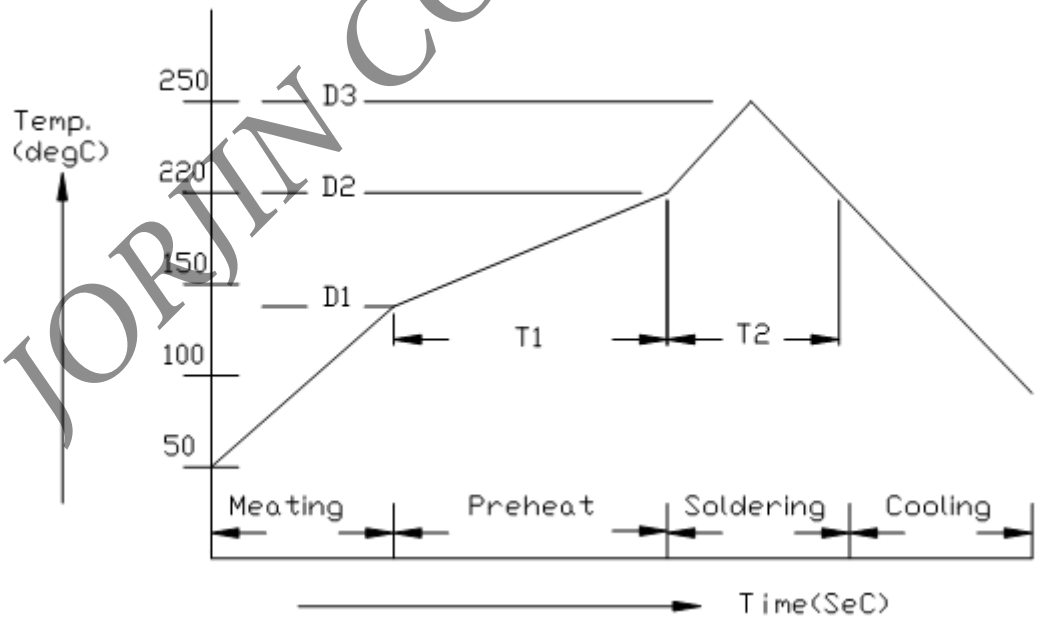
10.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs at 125 °C.

10.2. SMT Recommendation

- **Recommended Reflow profile：**



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

11. HISTORY CHANGE

Revision	Date	Description
D 0.1	2010/11/05	Draft 0.1
D 0.2	2010/12/01	Update module dimension & package information
D 0.3	2010/12/20	Update layout recommendation
D 0.4	2010/12/21	Update index of pin description on P19
D 0.5	2010/12/31	Update Reference Schematic on P30
D 0.6	2011/01/20	Modify module pin 1 location
D 0.7	2011/01/26	Modify P4 block diagram &module mechanical outline on P37
D 0.8	2011/02/08	Modify section12.1 module mechanical outline
D 0.9	2011/02/15	Modify Page 38 module mechanical outline
D 1.0	2011/02/18	Modify Page 38 module mechanical outline
R 0.1	2011/08/18	Release R 0.1
R 0.2	2011/10/06	Update Page 40 module mechanical outline
R 0.3	2012/02/15	Insert external Slow clock & TCXO clock input specification
R 0.4	2012/07/05	Add High Rate SDIO clock timing.