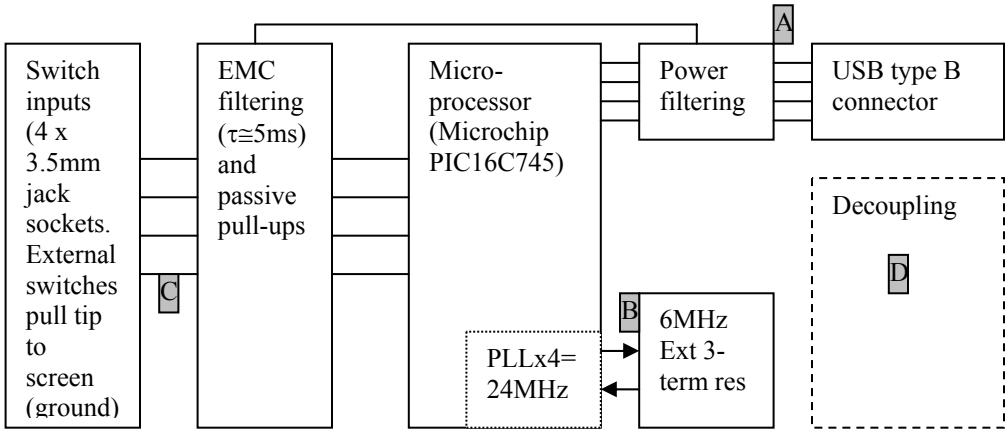
Block Diagram

An overview of the major sections of the interface follows:



Notes:

A. The device is a low speed USB peripheral. USB is a differential bus. Slew rates and external cable specifications are available in the USB specifications. Power is supplied by the USB bus, and is filtered in order to reduce transients to and from the bus.

B. The CPU has an external 6MHz 3-terminal resonator fitted close to the oscillator pins, which is multiplied to the required 24MHz clock using a PLL internal to the CPU. Outputs from the internal inverter are slew-rate-limited, and ground path from the resonator network is to a pin adjacent to the CPU's oscillator pins.

C. "Tip" connection of 3.5mm sockets are pulled high weakly (on CPU side of filtering), closing an external switch connects "tip" to "screen". Current via closed switch is 0.5mA. RC filtering protects CPU from transients, and reduces radiation of power noise.

D. Decoupling close to active components.